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Failure analysis and solutions to overcome latchup failure event of a power controller IC in bulk CMOS technology

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Abstract

Latchup failure which occurred at only one output pin of a power controller IC product is investigated in this work. The special design requirement of the internal circuits causes the parasitic diode that is inherent between the n-well and p-substrate to be a triggering source of the latchup occurrence in this IC. The parasitic diode of the internal PMOS was easily turned on by an anomalous external signal to trigger the neighbor parasitic Silicon Controlled Rectifier (SCR) path which causes latchup event in the CMOS IC product. Some solutions to overcome this latchup failure have been also proposed in this paper.
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1. Introduction

In CMOS integrated circuits, latchup is formed by the parasitic SCR path between VDD and VSS. This parasitic path is inherent in the bulk CMOS ICs. When the SCR path is triggered on to conduct a huge current from VDD to VSS, the chip is often burned out. The first-order equivalent circuit of the SCR path is shown in Fig. 1(a), and the cross-sectional view of this path in a bulk CMOS technology is illustrated in Fig. 1(b) [1]. In order to prevent latchup issue in bulk CMOS ICs, the guard ring structures and substrate/well pickups are often added to the I/O cells and internal circuits, respectively [2–4]. Guard ring structures are often applied to the I/O cell to prevent the latchup in the bulk CMOS ICs. There are two types of guard rings, minority-carrier guard ring and majority-carrier guard ring, to block latchup path in CMOS technology. Minority-carrier guard ring is used to collect injected minority carriers by a reverse-biased well/substrate junction. Due to the n-well with a deeper junction depth into p-substrate, the n-well guard rings are more effective than n+ diffusions for realization of minority-carrier guard rings in p-substrate bulk CMOS process. On the other hand, majority-carrier guard ring can de-couple the parasitic BJT action by reducing the voltage drop across the emitter/base junction. The majority-carrier guard rings

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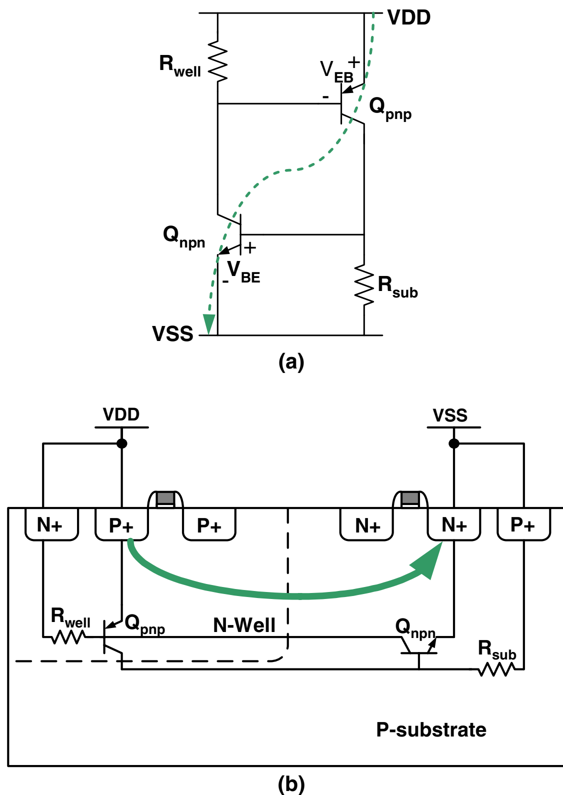


Fig. 1. (a) The first order equivalent circuit, and (b) the cross-sectional view, of the latchup structure in p-substrate bulk CMOS technology.

locally reduce the well/substrate resistance by forming the ohmic contact to reduce the voltage drop for a given trigger current. The guard ring structures are rarely applied to internal circuits due to the silicon area concerns. But, the substrate/well pickups are used in the internal circuits to reduce latchup susceptibility instead. The substrate/well pickups in internal circuits can decrease the voltage across the emitter/base junctions of the parasitic BJTs to efficiently improve latchup immunity. However, the wider double guard rings in I/O cells and more pickups in the internal circuits often occupy more layout area in the bulk CMOS ICs [5,6].

Although the guard rings and substrate/well pickups could efficiently overcome the latchup failure in CMOS ICs, the latchup failure phenomenon are still existed in many special application circuits. The "signal latchup" occurrence in voltage tolerant I/O circuits had been reported [7], where the parasitic SCR path existed between I/O pad and VSS. In addition, the power-on latchup phenomenon on DRAM modules was also investigated when the power supply is initially turned on [8]. The "anomalous latchup" failure in ESD protection circuits had also been studied [9,10], where the latchup failure was induced by the large N-well resistor associated with the RC-triggered active clamp circuit for on-chip ESD protection between VDD and VSS.

In this paper, the latchup failure phenomenon of a power controller IC is presented. Only one output pin showed latchup failure under negative current-mode latchup test. In order to find out the latchup failure spots, some failure analysis (FA) procedures, including de-cap of the IC package, EMission MIcroscope (EMMI), and Focused Ion Beam (FIB) were applied to this power controller IC. The reasons of latchup failure are analyzed and discussed by comparing with the results of failure analyses, layout patterns, and equivalent circuits.

2. Latchup test

2.1. Trigger current on the I/O pin

To verify the latchup immunity of a CMOS IC, the overshooting (positive) and undershooting (negative) currents are applied to each I/O pin of a CMOS IC to investigate whether the latchup occurs or not. The detailed latchup test procedure and specifications have been clearly specified in the EIA/JEDEC Standard No. 78 [11]. The schematic diagram to show a latchup trigger current applied to an output pin is illustrated in Fig. 2(a). The overshooting/undershooting trigger current on the pad is applied into the drain regions of output devices, as shown in Fig. 2(a). While the overshooting (undershooting) current is applied to I/O pin, the P+ drain/n-well (N+ drain/p-substrate) junction of output PMOS (NMOS) is forward biased to further generate the trigger current into the substrate. The injecting substrate current can trigger parasitic SCR paths in the I/O cell or in the internal circuits. If the device under test (DUT) is triggered into latchup state by the trigger current applied on an I/O pin, the current flowing from VDD to VSS has an obvious increase. To avoid latchup induced by the trigger current on the I/O pins, the double guard rings are often used to block the latchup path between PMOS and NMOS in I/O cells. To avoid the latchup occurrence in the internal circuits induced by the trigger current on the I/O pins, the additional guard rings have been suggested to be added between the I/O cells and the internal circuits [5,6].

2.2. Over-voltage on the power pin

The latchup in CMOS ICs is also sensitive to voltage transition on VDD supply [8,12]. In order to verify latchup immunity of CMOS ICs under a power-transient trigger, the test circuits is configured in Fig. 2(b). The trigger voltage is applied on the VDD pin, and the VDD-to-VSS current is monitored to judge if latchup occur. The power-transition trigger voltage often

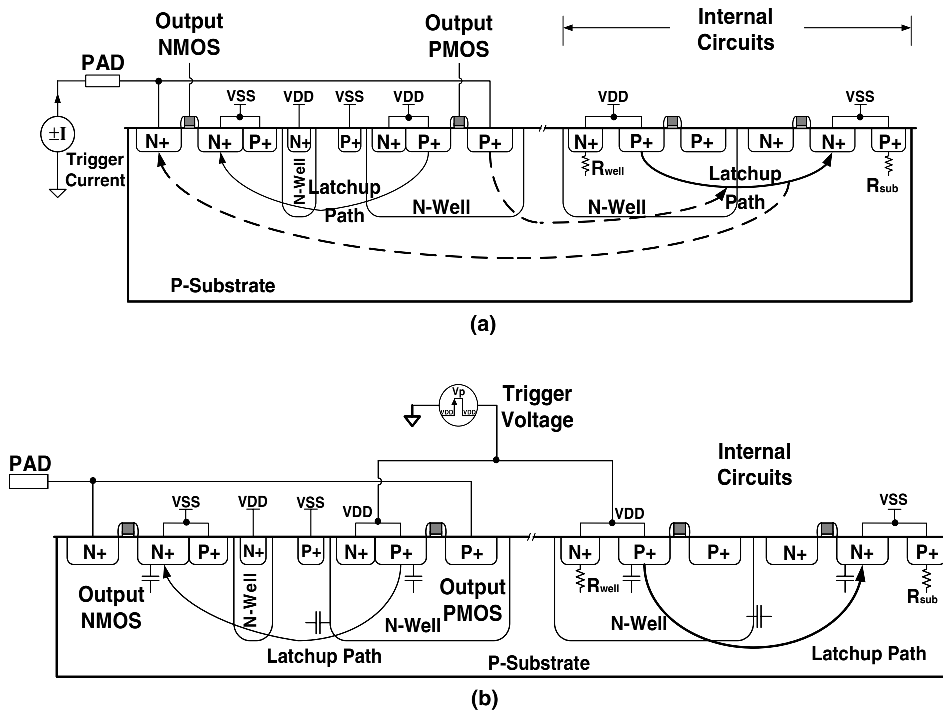


Fig. 2. Latchup test for a CMOS IC with (a) the overshooting or undershooting trigger current at each I/O pin and (b) the voltage-transient trigger at the VDD pin.

generates transient current through the parasitic junction capacitance into the n-well or p-substrate to initiate latchup path in CMOS ICs. In general, the consumer CMOS ICs should not be triggered into latchup by a trigger current of ±100 mA on the I/O pins or a trigger voltage of 1.5 × VDD on the VDD pin [11].

3. Latchup failure in a power controller IC

3.1. Latchup phenomenon and failure analysis

Table 1 gives the latchup testing results for input/output pins and power pins under current trigger test and over-voltage trigger test, respectively. This power controller IC shows a lower latchup immunity level under negative current trigger test. In Fig. 3, the *I–V* characteristic of the inherent parasitic SCR in this chip shows a higher immunity level against the over-voltage trigger test. The trigger-on voltage (V_{t1}) is about 10 V which is higher than the over-voltage test requirement of 1.5 × VDD (7.5 V). However, this chip still has the latchup risk because the inherent parasitic SCR shows a holding voltage (V_h, ~1.5 V) lower than normal oper-

Table 1
The latchup immunity levels of this IC product

I-Test applied to I/O pins: >200 mA/−50 mA
V_{supply} Over-voltage test applied to power pin: >7.5 V

The latchup immunity level is only −50 mA under negative current trigger test.

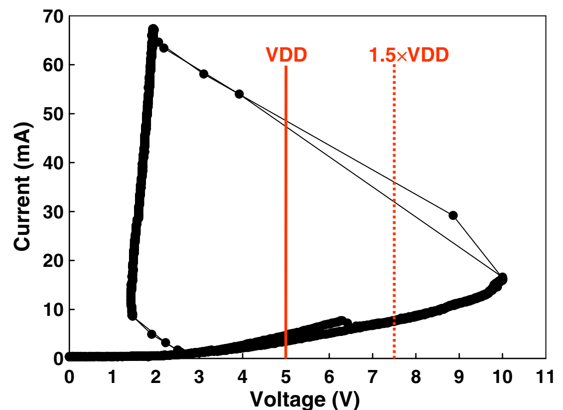


Fig. 3. The *I–V* curve of the parasitic SCR device in this IC chip. Due to the holding voltage of the parasitic SCR device is lower than normal operation voltage (VDD), the IC chip has a latchup risk during anomalous trigger status.

ation supply voltage of 5 V. The parasitic SCR path could be induced into latchup state by the external trigger source during current-mode latchup test.

According to the test results in Table 1, an output pin (Pin A) presents a lowest latchup immunity level throughout the entire test pins. The chip failed under the negative current trigger test when Pin A was triggered by a negative current pulse of 100 mA. The measured voltage waveforms between VDD and VSS are shown in Fig. 4, when the Pin A was triggered by different negative trigger current pulses. The power pin VDD was applied with a normal operation voltage of 5 V with respect to VSS. In addition, the negative trigger current was applied on Pin A as a trigger source of latchup event. The voltage waveforms between VDD and VSS were measured and used to judge if latchup occur or not during the current mode latchup test. When a negative trigger current of 60 mA was applied on Pin A, the VDD voltage is dropped down to 4 V but it returns to 5 V again after the current trigger. But, it was held on 2.3 V and the chip entered latchup state after a negative trigger current of 80 mA is applied to the Pin A. Nevertheless, the other input and output pins in the same chip can sustain the positive and negative current trigger test up to a level over 200 mA. However, all the input and output cells have the same ESD protection structure, including a gate-grounded NMOS (GGNMOS) and a gate-VDD PMOS (GDPMOS) as shown in Fig. 5(a). The corresponding layout view of such ESD protection structure for I/O cell is shown in Fig. 5(b). The GGNMOS and GDPMOS devices were enclosed with double guard rings to prevent latchup in the I/O cells.

To investigate the latchup phenomena between Pin A and the other output pins, different parameters (such as the rise time and the pulse width) of the negative trigger current sources were applied to the Pin A, Pin B, and Pin C which have the same I/O cell in the chip. The latchup

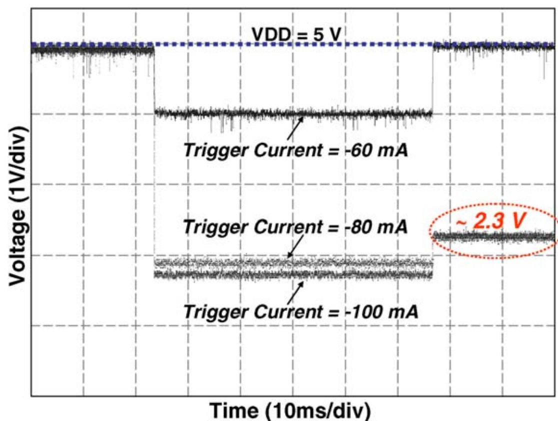
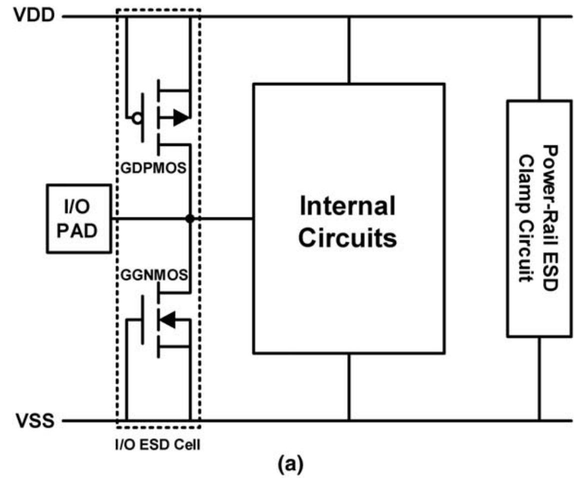


Fig. 4. The measured voltage waveforms on VDD node under different trigger currents applied on the Pin A.



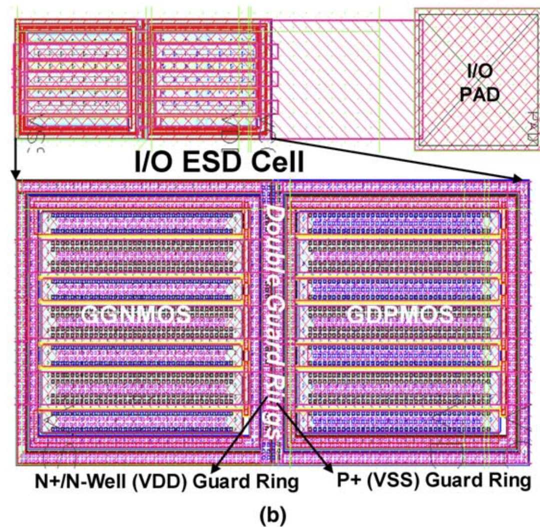


Fig. 5. (a) The schematic circuit diagram, and (b) the layout top view, of the I/O cell with ESD protection devices. The double guard rings are used to block the latchup path in the I/O cell.

immunity levels in Pin A, Pin B, and Pin C under different test conditions are listed in Table 2. In Pin A, the latchup immunity level was found to be related the rise time and pulse width of the triggering current. The latchup immunity level is degraded by decreasing the rise time or increasing the pulse width of the triggering current source. On the contrary, the phenomena were not observed in the Pin B and the Pin C. The results of the latchup immunity levels among these pins with the same I/O cell have identified that the latchup occurrence was not related to the I/O cell with ESD protection devices (GGNMOS and GDPMOS).

In order to find out the root cause of latchup, EMission MIcroscope (EMMI) is used to locate the hot spots

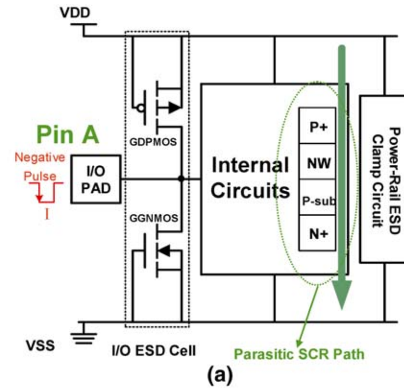
Table 2
The latchup immunity levels at Pin A, Pin B, and Pin C of a power controller IC under different pulse widths and rise times of the triggered sources

Pulse width	Rise time			
	5 μs	50 μs	500 μs	5 ms
Pin A				
10 μs	>±200 mA	>±200 mA	>±200 mA	>±200 mA
1 ms	−50 mA	−50 mA	−50 mA	>±200 mA
1 s	−50 mA	−50 mA	−50 mA	−50 mA
Pin B				
10 μs	>±200 mA	>±200 mA	>±200 mA	>±200 mA
1 ms	>±200 mA	>±200 mA	>±200 mA	>±200 mA
1 s	>±200 mA	>±200 mA	>±200 mA	>±200 mA
Pin C				
10 μs	>±200 mA	>±200 mA	>±200 mA	>±200 mA
1 ms	>±200 mA	>±200 mA	>±200 mA	>±200 mA
1 s	>±200 mA	>±200 mA	>±200 mA	>±200 mA

and the latchup occurrence path. The measurement setup is illustrated in Fig. 6(a). The latchup condition is presented by a negative triggered current pulse of −100 mA applied to Pin A, and the chip is powered with 5-V VDD. The parasitic SCR path at internal core circuits was obviously observed by the Emission Microscopic photograph as shown in Fig. 6(b). The metal line that connects to internal circuits of Pin A was cut off by Focused Ion Beam (FIB) to prove the latchup occurrence at the internal circuits. After FIB treatment, the results of current trigger latchup test on Pin A can pass the level of over −200 mA. This has verified that the latchup occurrence is located at the internal circuits, not the I/O cell.

3.2. Latchup failure mechanism

As comparing with the layout patterns and the hot-spot image of the EMMI photograph, Pin A was found to be directly connected to a PMOS transistor close to the internal latchup location. The equivalent circuit and the device cross-sectional view of the PMOS device in the internal circuits are shown in Fig. 7(a) and (b), respectively. According to the schematics and layout patterns, the root cause of this anomalous latchup is identified to the n-well pickups of the PMOS. The n-well of this PMOS is directly connected to the output pad (Pin A), therefore the potential of n-well was related to the signal presenting on the pad. During the current-mode latchup test, a negative triggering current pulse drops down the potential of n-well. Consequently, the parasitic diode between the p-substrate and n-well turns on by a forward bias. The parasitic diode injects the substrate current to trigger the neighbor parasitic SCR path in the internal circuits, as illustrated in Fig. 8. The locations of the latchup path and the triggering source in the



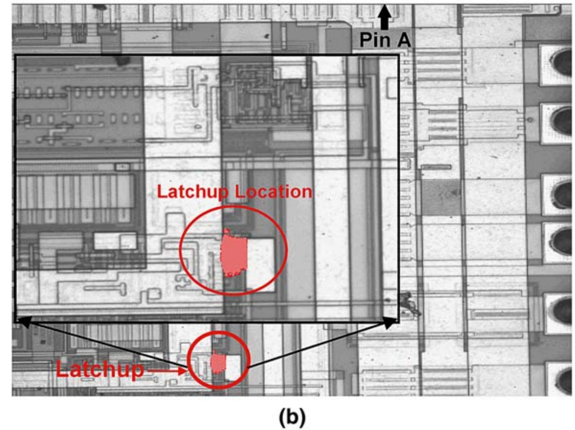


Fig. 6. (a) The measurement setup of latchup test. (b) The latchup path in the internal circuits was identified by the EMMI photograph.

layout patterns are shown in Fig. 9(a). The zoomed-in layout to show the relationship between the PMOS and latchup location is illustrated in Fig. 9(b). The parasitic diode between the n-well and p-substrate will be turned on by the negative I/V injection source on the pad (Pin A). Then, this forward biased diode will inject a huge substrate current to trigger on the parasitic SCR path in its neighborhood. Even if there are some guard rings to surround the PMOS (triggering source), the injecting substrate current is still large enough to induce latchup occurrence in the neighbor circuits to cause this latchup failure event.

3.3. Solutions and discussions to overcome latchup failure

According to the measurement results in Figs. 3 and 4, the latchup failure would not occur in the lack of enough substrate trigger current. Therefore, the latchup failure can be solved by eliminating or reducing the substrate trigger current which initiates the latchup occurrence during current trigger latchup test. Several solutions were proposed to improve the latchup immu-

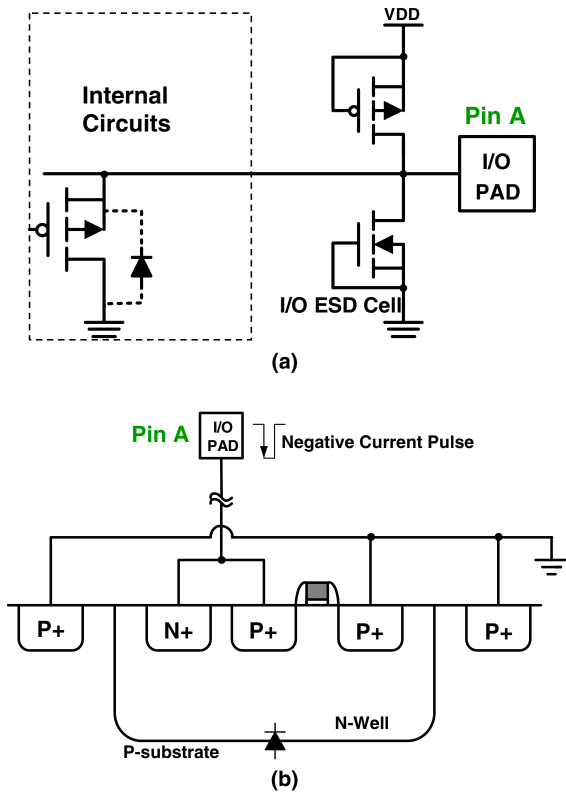


Fig. 7. (a) The equivalent circuit, and (b) the cross-sectional view, of the PMOS in the internal circuits that is directly connected to the pad of Pin A.

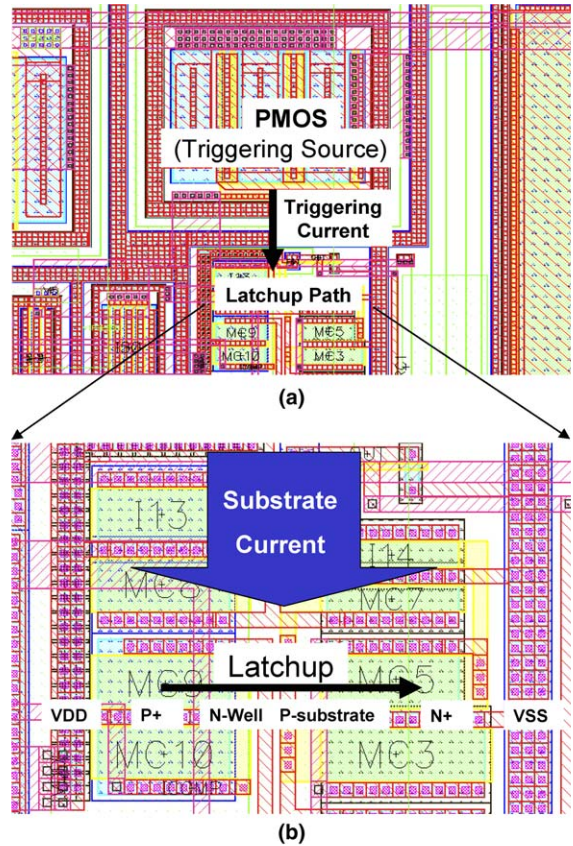


Fig. 9. (a) The relationship between the PMOS and latchup path in the layout pattern. (b) The zoomed-in layout pattern to show the latchup location at the neighbor circuits.

nity level in this chip. Firstly, the parasitic diode can be held on reverse status to thoroughly eliminate the substrate current injection during the negative current trigger latchup test. The potential of n-well (N+ guard ring) of the PMOS should be connected to VDD or held on a high potential level, where only a few mask layers need to be modified for achieving high latchup immunity level in this IC product. When the n-well pickup is connected to a high potential level to keep the parasitic diode in reverse biased, there is no substrate current injecting to trigger the latchup path in this CMOS IC product. However, the original design for the n-well pickup of the PMOS tied to pad is used to reduce the threshold voltage (V_{th}) of the PMOS in this application. If the n-well

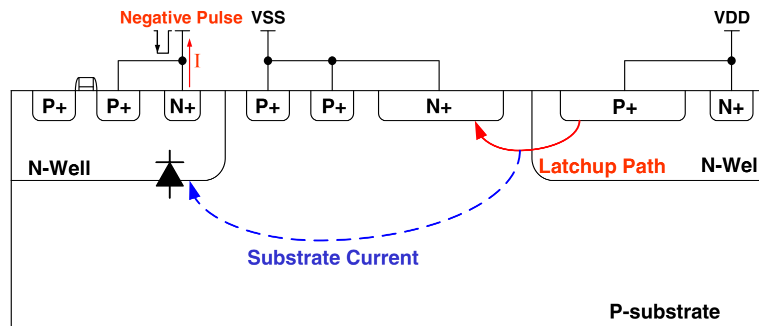


Fig. 8. The parasitic SCR path was triggered by the substrate current that is induced from the forward diode of n-well/p-substrate in the PMOS.

pickup was tied to VDD, the threshold voltage of the PMOS will be increased due to the body effect. Then, the performance of this IC could be slightly degraded by the n-well pickup being tied to VDD.

Secondly, the distributions of the trigger currents between the parasitic N+/p-well junction diode of the GGNMOS in I/O ESD cell and the n-well/p-substrate junction diode of the PMOS in the internal circuits under the negative trigger current stress are shown in Fig. 10(a). These two forward-biased diodes conduct the latchup trigger current, I_1 and I_2, during the negative current trigger latchup test. The I_1 current is supported by the guard ring of GGNMOS in the I/O ESD cell, and the I/O ESD cell is far away from the internal circuits. So, the I_1 current did not cause latchup event in this Pin A. But, the transient current I_2 induces a large enough substrate current to initiate the latchup failure in the neighboring SCR path. If a resistor R with a resistance of several ohms is added between the pad and the output PMOS of Pin A, the transient current I_2 under the negative current trigger latchup test can be significantly reduced. While the turned-on resistance of the N+/p-well diode is about 4 Ω, the transient current I_2 could be decreased about 33–60% to reduce the substrate current injecting to the internal circuits by adding a resistor of 4–12 Ω, as shown in Fig. 10(b). The latchup immunity level of this IC can be significantly improved by reducing the trigger current injecting into internal circuits. However, the inserted resistor would induce the voltage drop to degrade the circuit performance. Therefore, the inserted resistance should be suitably chosen to achieve the optimal value for effectively improving the latchup immunity level without seriously degrading circuit performance.

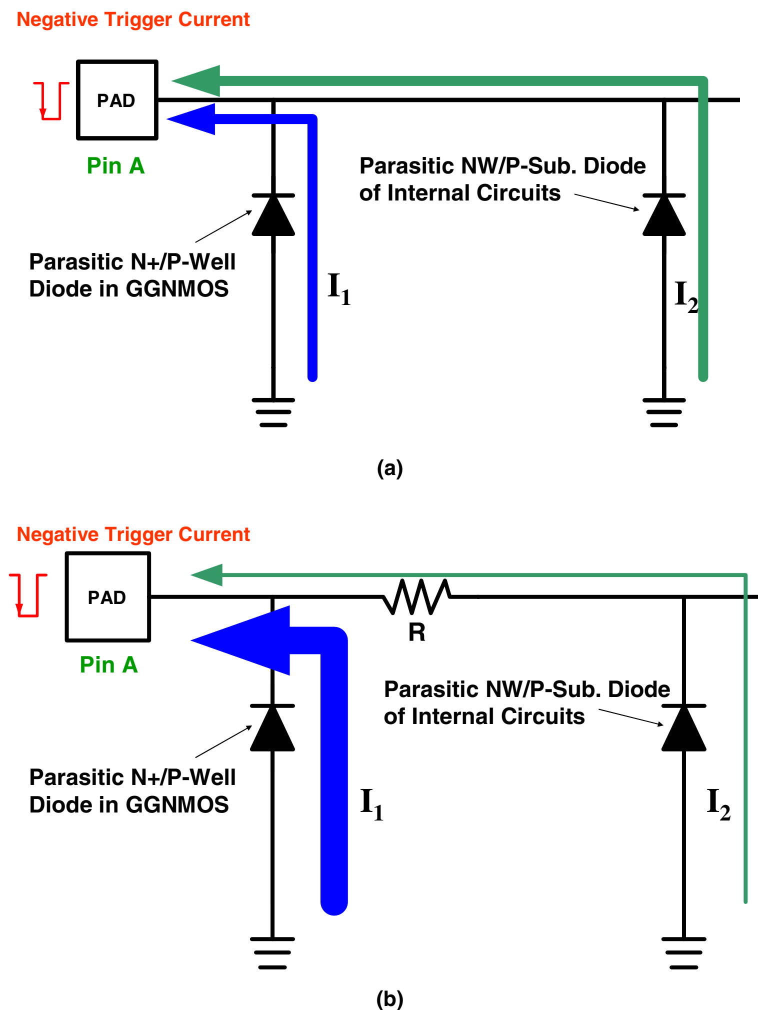


Fig. 10. The distributions of the major trigger currents (a) without adding the resistor, (b) with adding the resistor, between the I/O cell and the internal circuits.

Thirdly, a wider guard ring to surround the special PMOS is recommended to increase the latchup immunity of this IC product. The wider grounded P+ guard ring can efficiently capture the major carriers (holes) to reduce the trigger substrate current injecting towards the internal circuits. In addition, the minority carrier (electrons) would also be caught by the N+/n-well guard ring to further eliminate the substrate current to prevent the latchup occurrence. The latchup would not occur under the lack of trigger current, therefore the wider double rings which surround the floating n-well of PMOS can efficiently eliminate the trigger current to improve latchup immunity of the IC products.

4. Conclusion

From the detailed analyses, the latchup failure was attributed to the potential of n-well pickup in the PMOS of the internal circuits in CMOS IC. Due to the special design concern in the PMOS, the parasitic diode between the n-well and p-substrate was turned on to induce a substrate current to trigger the neighbor SCR path, when a negative latchup voltage/current trigger source is applied to the pad. To solve this latchup occurrence, the potential of n-well in the PMOS should be connected to a higher potential. However, the performance will be slightly degraded when the n-well pickup is tied to VDD. On the other hand, the trigger current can be significantly restrained by adding a resistor between the I/O cell and the output PMOS in internal circuits. To re-draw the chip layout with a wider spacing from the PMOS and its neighborhood, as well as a wider P+ guard ring to surround the PMOS, is suggested to overcome such latchup failure in this IC product.

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