Pergamon

0038-1101(95)00410-6

Solid-State Electronics Vol. 39, No. 7, pp. 1015–1020, 1996
Copyright © 1996 Elsevier Science Ltd
Printed in Great Britain. All rights reserved
0038-1101/96 $15.00 + 0.00

NUMERICAL ANALYSIS OF THE TRANSIENT BEHAVIOR OF THE SIDEGATING EFFECT IN GaAs MESFETs

SHWU-JING CHANG and CHIEN-PING LEE

Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 30050, Taiwan, Republic of China

(Received 17 July 1995; in revised form 25 October 1995)

Abstract—Transient responses of sidegating effects in GaAs MESFETs are analysed using two-dimensional numerical simulations. Substrates with different trap conditions are considered to clarify the dominant processes in the sidegating transients. Particularly for the electron trap rich substrate (the commonly used undoped semi-insulating GaAs), transient sidegating responses under different bias conditions and the effect of sidegating on the active loads are analyzed to evaluate the effect of sidegating on circuits in operation. Copyright © 1996 Elsevier Science Ltd

INTRODUCTION

The sidegating effect is a serious problem in integrated circuits of GaAs MESFETs[1,2]. Steady-state analyses[3–5] have shown that, for hole trap rich substrates, the negative voltage applied to an adjacent electrode appears at the vicinity of the FET's channel/substrate interface and causes the reduction of the channel current. For electron trap rich substrates, the sidegating effect occurs when the negative sidegate voltage is over a certain threshold. The presence of some hole traps and the injection of holes (from a Schottky contact on the semi-insulating substrate) have been shown to be essential to the sidegating effect in this case[5]. Since the sidegating effect involves filling and detrapping of deep traps in the substrate, it is not an instantaneous effect. According to Birrittella *et al.*[6], the time constants associated with changing the width of the backside depletion layer or the magnitude of backgating are in the range of 10 μs–100 ms. Therefore, the static effect analyzed previously sometimes can not apply when the circuits are in operation. In this work, the transient phenomena of the sidegating effect in FETs on different substrates are analyzed to identify the dominant processes. The influence of sidegating transients on circuit operation is then discussed.

NUMERICAL METHODS, MODELS AND DEVICE STRUCTURES

A two-dimensional, two-carrier, transient device simulator was developed. This simulator was based on the drift-diffusion model for the transports of electrons and holes. The Shockley–Read–Hall (SRH) model was adopted for the emission/capture of carriers through deep traps. The Schottky barrier height was assumed to be 0.8 V. The current transport across the Schottky-barrier junction was described by the thermionic emission–diffusion theory. Surface states were not considered and the Neumann boundary condition was used for the free surface. The finite difference method, Scharfetter–Gummel scheme and fully implicit backward Euler method[7] were adopted. Poisson's equation, electron and hole continuity equations were solved self-consistantly together with the rate equations of deep traps by using the decoupled Gummel method[8].

As shown in Fig. 1, the device structure used in the simulations had a realistic sidegate configuration. Both the FET and the sidegate were placed on the top surface of the semi-insulating (SI) substrate. The FET had a 1 μm gate and a 3 μm source-to-drain spacing. The FET's channel was 0.12 μm deep and uniformly doped to $10^{17}\,cm^{-3}$. The sidegate was 4.35 μm away from the FET. This spacing was chosen to be close to that used in real circuits. A 0.2 μm wide Schottky contact was placed between the FET and the sidegate, simulating a portion of the gate contact which extrudes out of the active region and contacts the SI substrate. The SI substrate was assumed to contain deep donors which compensate for the residual shallow acceptors of about $10^{15}\,cm^{-3}$. For comparison with the steady-state results reported in Ref.[5], substrates with different trapping conditions of the deep donors were considered, namely, the electron trap rich (ETR) substrate, and substrates which contain electron traps only (ET) or hole traps only (HT). Detailed trap conditions of the substrates were listed in Table 1. The capture cross-sections and energy levels of these traps were chosen for the convenience of simulations and analyses. To be specific, they were chosen not only to emphasize the relation between the trap types and the sidegating responses, but also to save the computation time.

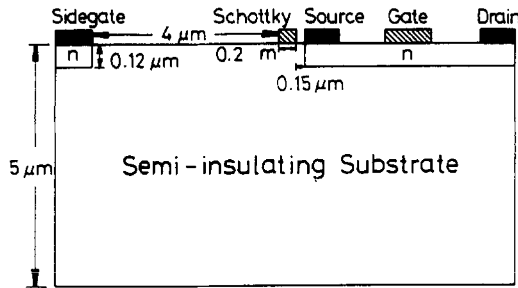


Fig. 1. Device structure used in the simulations.

Under these assumptions, quantitative agreement between the simulated results and the experimental ones[6,9,10], especially in the time scale, may not be acquired. Nevertheless, dominant processes in the sidegating transients as well as the qualitative trends of the responses can be clearly identified.

RESULTS AND DISCUSSIONS

Dependence on substrate conditions

Transient sidegating behaviors for GaAs MESFETs on substrates with different trap conditions (ETR, ET and HT) were investigated. In the simulations, the sidegate bias was changed from 0 V to -2 V in 1 ns, while the source, gate and the Schottky contact were grounded, and the drain was biased at 1 V. The 0– -2 V sidegate voltage swing was chosen to be similar to that used in a real circuit environment. It should be pointed out that for the device arrangement shown in Fig. 1 and the biased condition used, the threshold for the steady-state sidegating effect is around 0.4 V for the ET and ETR substrates and 0 V for the HT substrate. So the FET is d.c. sidegated with the voltage range used. Figure 2(a) and (b) shows the responding drain current (I_D) with linear time scale and log time scale, respectively. The corresponding sidegate current (I_{SG}), the Schottky contact current (I_{SB}), and the hole injection current from the Schottky contact (I_{hSB}) as functions of time are plotted in Fig. 2(c) (in log–log scale).

The responses shown in Fig. 2(b,c) can be divided into four stages (A–D) and described as follows. For up to 1 ns (stage A), as the sidegate voltage is changed

Table 1. Substrate conditions

Category	Electron capture cross-section (cm^2)		Hole capture cross-section (cm^2)
Electron trap	1×10^{-13}		3×10^{-16}
Hole trap	3×10^{-16}		1×10^{-13}
Substrates	E_c-E_T (eV)	N_T (cm^{-3})	Trap type
ETR	0.715	10^{16}	Electron trap
	0.745	10^{15}	Hole trap
ET	0.715	10^{16}	Electron trap
	0.745	10^{15}	Electron trap
HT	0.715	10^{16}	Hole trap
	0.745	10^{15}	Hole trap

to -2 V, the currents I_{SG}, I_{SB}, I_{hSB} increase with the negative sidegate voltage, while I_D decreases about 12%. Responses up to this stage are qualitatively the same for all three substrates. This is because the deep traps can not respond to such fast changes in 1 ns. After stage A, when the sidegate voltage was kept at -2 V, currents in the HT substrate start to behave differently from those in the ET and ETR substrates. For the HT substrate, the currents I_{SG}, I_{SB}, I_{hSB} and I_D remain at constant values during stage B (from 1 ns to about 0.3 μs) and decrease again in stage C (from 0.3 μs up to 10 ms). For both ET and ETR substrates, on the other hand, all these currents continue decreasing throughout stages B and C. At the end of stage C, the reduction in drain current becomes more than 25% for all these three substrates. During stage D (since about 10 ms), the drain current for ETR and HT substrates decreases, while that for the ET substrate increases, all towards their respective steady-state values[see Fig. 2(a)]. By the way, in this final stage, the apparent increase in the sidegate current and the electron current through the Schottky contact can be observed only in the case of ETR substrates.

Dominant processes in the sidegating transients can be further identified through the investigation of the corresponding changes in the potential, carrier concentrations and carrier occupancies of deep traps. These dominant processes for three types of substrates (ET, ETR and HT) are described in the following. Only some profiles for the ETR substrate at 1 ns and 10 ms are shown for illustration. Figure 3 shows profiles of the potential, the electron concentration and the ionization ratio of deep donors at 1 ns for the ETR substrate. The potential is linearly graded. The electron concentration in the *i*-region is increased to about 10^{12} cm^{-3} (the initial thermal equilibrium concentration is about 10^6 cm^{-3}). The concentration of ionized deep donors remains equal to the concentration of shallow acceptors (i.e. the ionization ratio of deep donors, N_{dd}^+/N_{dd}, is close to 9%) in the *i*-substrate. This is because: immediately after the application of the voltage step, the *n-i* barrier of the sidegate is lowered, electrons are injected from the sidegate to the Schottky contact and the FET side, and holes are injected from the Schottky contact to the sidegate. Both the sidegate current and the Schottky current (mostly electron current) increase rapidly before the deep traps can respond. Therefore, in this stage (A) regardless of the trap types in the substrate, the drain current decreases due to a field effect of the sidegate voltage through the substrate with injected electrons.

In stages B and C for ETR and ET substrates, as excess electrons are getting captured by electron traps, the *n-i* barrier of the sidegate is recovered. Therefore, the electron injection current from the sidegate decreases, and the electron concentration in the substrate returns to about 10^7 to 10^8 cm^{-3}. On the other hand, injected holes continue to accumulate

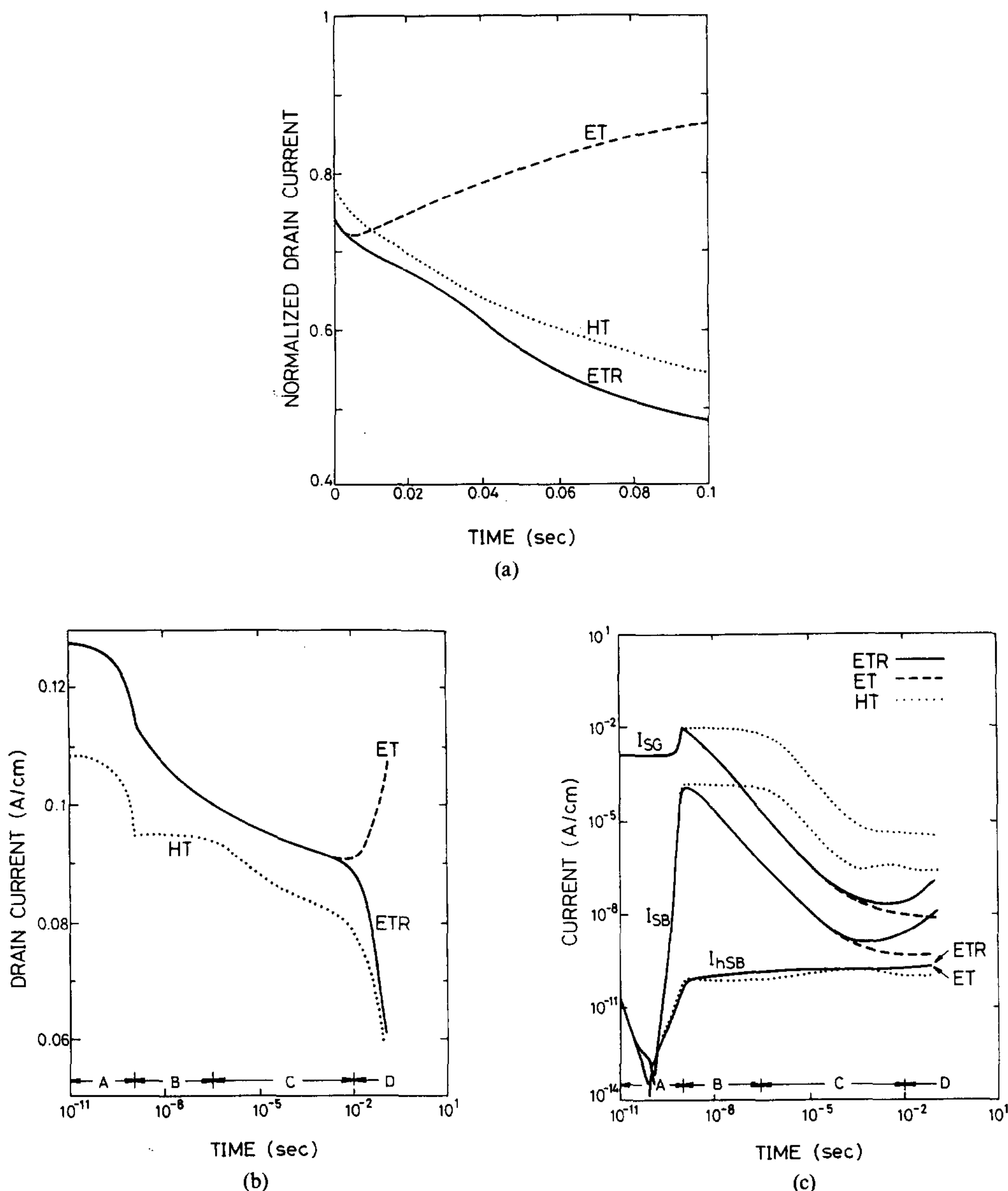


Fig. 2. Calculated (a) drain current with linear time scale, (b) drain current with log time scale, and (c) the corresponding sidegate current (I_{SG}), the Schottky contact current (I_{SB}), and the hole injection current from the Schottky contact (I_{hSB}) as functions of time.

and form a nearly flat potential region around the sidegate. This increases the field strength near the FET and decreases the drain current. The profiles of the potential, the hole concentration, and the ionization ratio of deep donors at the end of stage C (about 10 ms) for the ETR substrate are shown in Fig. 4. The substrate regions where N_{dd}^{+}/N_{dd} approaches 0 or less than 9% are negatively charged due to the shallow acceptors and the electron occupancy in deep donors. Please note the hole accumulation and flat potential region at the sidegate side of the substrate. Note also that the region between the sidegate and the FET becomes negatively charged, especially in the region near the surface close to the FET side.

In the final stage (D), for the ET substrate, the drain current gradually increases, as the channel/substrate interface potential barrier is lowered due to the re-emission of electrons from electron traps, until the steady-state is reached, while for the ETR substrate, the drain current asymptotically decreases to the steady-state value. This results from the extension of the hole accumulation and thus nearly flat potential region as well as the emission of holes from hole traps in the vicinity of the channel/substrate interface[5]. In this way, the sidegate voltage is propagated to the FET side and a negatively charged region is formed under the FET's channel.

In Ref.[11], where the backgate is placed at the bottom side of the substrate, the decrease in drain current for the electron trap rich substrate beyond 50 ms is said to be too fast to be explained by simple trapping and detrapping effects in deep levels. It was attributed to the positive feed back between the extension of the hole accumulation region with flat potential and the increase of the hole injection current. On the contrary, we found that the hole injection current through the Schottky contact, I_{hSB} [see Fig. 2(c)] increases only slightly after stage A for all substrates. From another steady-state analysis, we found that, as the sidegate voltage exceeds the negative sidegating threshold, the electron current through the Schottky contact increases with the sidegate voltage or the field between the Schottky contact and the sidegate, whereas the hole current becomes limited by the thermionic emission of holes over the barrier to the SI substrate.

As for the HT substrate after stage A, holes are drifted towards the sidegate, blocked by the n-i barrier, and become captured by hole traps around the sidegate. In the meantime, hole traps near the channel/substrate interface emit holes in response to the hole depletion, and a negatively charged region forms there. Finally, as the steady-state is approached, the potential profile becomes nearly flat in the SI substrate and the sidegate voltage drops entirely across the channel/substrate interface.

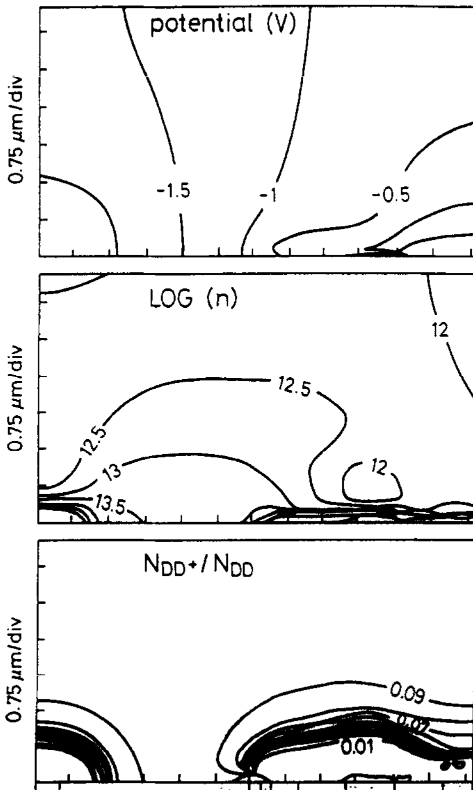


Fig. 3. Profiles of the potential, the electron concentration and the ionization ratio of deep donors at 1 ns for the ETR substrate.

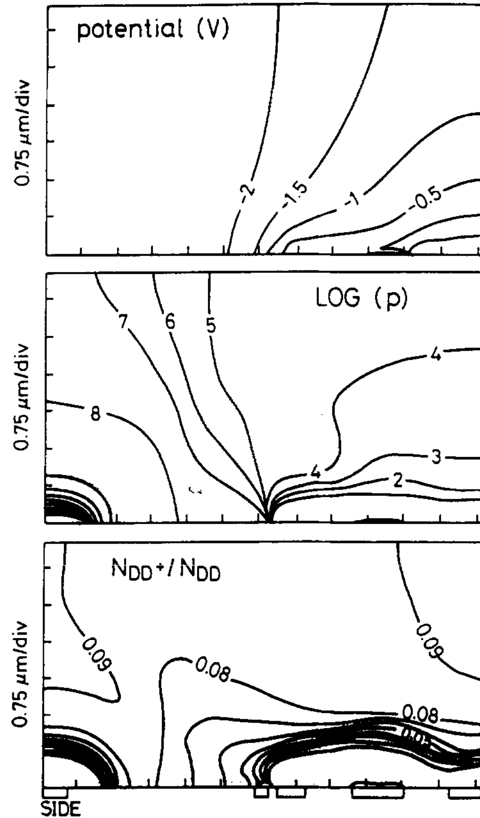


Fig. 4. Profiles of the potential, the hole concentration and the ionization ratio of deep donors at the end of stage C (about 10 ms) for the ETR substrate.

Dependence on the pulse voltage and the scan rate of the sidegate voltage

In order to see the dependence of the sidegating transient on the peak sidegate voltage and the scan

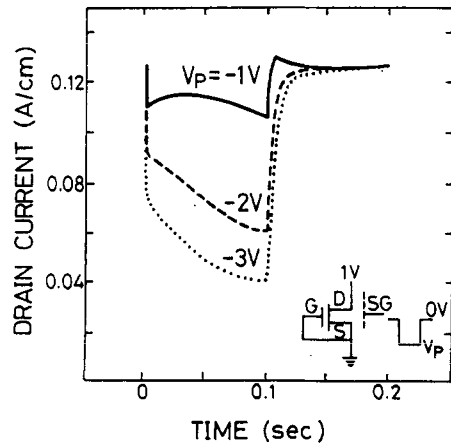


Fig. 5. The calculated drain currents in response to negative sidegate voltage pulses for the ETR substrate. The source, gate, and the Schottky contact were grounded, and the drain was biased at 1 V.

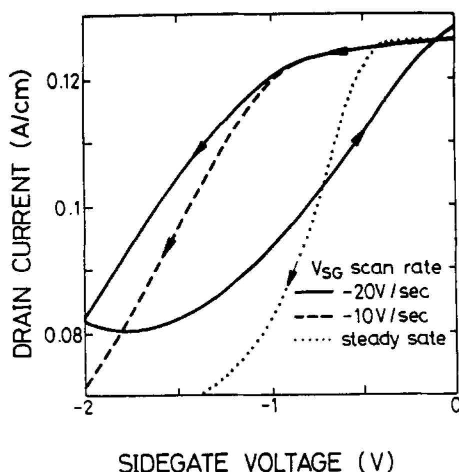


Fig. 6. The calculated drain currents as functions of negative sidegate voltage with different scanning rates.

rate, we performed calculations for FETs on a ETR substrate, which corresponds to the commonly used undoped EL-2 rich semi-insulating GaAs substrate. Pulses of 0.1 s duration with peak voltages (V_P) of -1, -2 and -3 V were applied to the sidegate. The source, gate and the Schottky contact were grounded, and the drain was biased at 1 V. Figure 5 shows the responding drain currents. The reductions in drain current at the falling edge (at 1 ns) and just before the rising edge (at 0.1 s) of the pulse increase with the peak voltage. The former is simply due to the increase in the electric field across the SI substrate, while the latter results from the sidegating effect which causes the sidegate voltage to drop across the channel/substrate interface. For $V_P = -1$ V, there is a slow increase (before about 25 ms) following the steep decrease of drain current. This is due to the re-emission of electrons from electron traps.

Next, negative sidegate voltage scans from 0 to -2 V with -10 and -20 V s^{-1} were performed on the ETR substrate with the FET biased as above. A round trip scan was simulated in the case of -20 V s^{-1}. Figure 6 shows the resulting drain currents. The steady-state result is also included in the figure for comparison. It can be seen from Fig. 6 that, the faster the scan rate of negative sidegate voltage, the larger the apparent sidegating threshold and the less steep the decrease of drain current. Note also that the round trip scan of the negative sidegate voltage results in a big loop in the drain current. These features are commonly observed in experimental measurements and can be easily explained by the long response time of the deep traps, which are responsible for the sidegating effect.

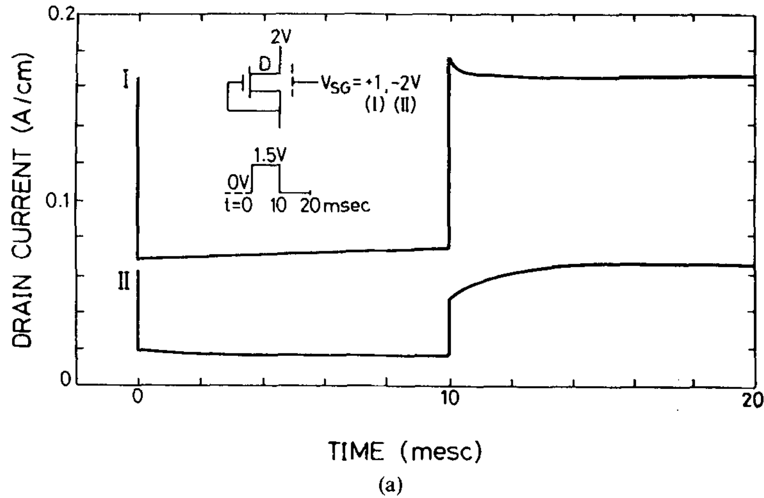
The effect of sidegating on the active loads

In real circuit operation, the voltage of the source node of an active load, which is one of the most sidegated FETs in the circuit, switches back and forth very fast. The deep traps at the channel/substrate interface usually fail to respond to such fast changes. In this simulation, the FET was connected as an active load, with the gate (thus the Schottky contact) tied to the source and the drain biased at 2 V. The voltage of the source node was switched from 0 V to 1.5 V in 100 ps, kept at 1.5 V for 10 ms, then switched back to 0 V in 100 ps. To investigate the influences of sidegating on the responding drain currents, the sidegate was biased at 1 V and -2 V. These correspond to the cases when the maximum voltage differences are below and over the sidegating threshold, respectively. As can be seen from Fig. 7(a), the transient behavior at the rising edge of the drain current (in response to the falling edge of the source voltage) is most affected by the sidegating effect. There is a slight undershoot and a prominent overshoot in the drain current when the sidegate is biased at 1 V. In this case, only the electrons, electron traps and the channel/substrate interface potential barrier are involved. On the other hand, when the sidegating threshold is exceeded, both the absolute magnitude and the relative change of the drain current are reduced. The falling edge and especially the rising edge of the drain current become damped. This is because the steady-state potential in the substrate is essentially kept at the sidegate bias voltage due to the sidegating effect[see Fig. 7(b)]. In this case, holes, hole traps under the channel, and the resulting channel/substrate interface potential barrier play important roles.

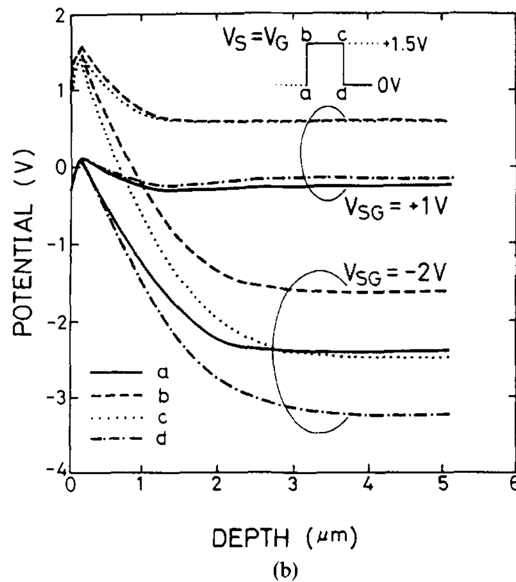
It can also be seen from Fig. 7(a) that the sidegating effect is more serious when the voltage difference between the drain and the source, V_{DS}, is smaller. To be specific, when V_{DS} equals 2 V, the drain current at sidegate voltage $V_{SG} = -2$ V is about 41% that at $V_{SG} = 1$ V, while it is only about 24% when V_{DS} is reduced to 0.5 V. The reason that the sidegating effect is stronger when the drain voltage is lower is because that potential beneath the FET's channel is more negative compared to the situation when the drain voltage is biased higher. This phenomenon is the same as that in the steady-state backgating effect[1].

CONCLUSIONS

Based on the results given above, several conclusions or suggestions can be drawn as given in the following. First, substrate conditions and circuit operation conditions such as the biases and switching speed can all affect the transient characteristics of the sidegating effect and the resulting circuit performance. These factors should be taken into account in the modeling and evaluation of the sidegating problem in circuits. Secondly, minimization of the hole traps in the SI substrate can eliminate the sidegating effect in the steady-state. However, even without the hole traps, the electric field between the sidegate and the FET can still cause some transient reduction in the channel current. Thirdly, sidegating



(a)



(b)

Fig. 7. (a) The calculated drain currents as functions of time, (b) the potential profile under the middle of the gate contact. The FET was connected as an active load with the drain biased at 2 V. A positive pulse voltage of 1.5 V was applied to the source node when the sidegate was biased at 1 V and −2 V.

characteristics should be measured with a very slow scanning rate. If the scanning rate of the sidegate voltage is too fast, the results will not be realistic. Finally, static sidegating characterization should include a measurement at small V_{DS}, because this is the condition when the sidegating effect is the worst. Otherwise the sidegating problem might be underestimated.

Acknowledgements—This work is supported by the National Science Council of the Republic of China under contract no. NSC84-2215-E009-033.

REFERENCES

1. C. P. Lee, S. J. Lee and B. M. Welch, *IEEE Electron Device Lett.* **EDL-3**, 97 (1982).
2. C. P. Lee, R. Vahrenkamp, S. J. Lee, V. D. Shen and B. M. Welch, in *Proc. GaAs IC Symp. Tech. Dig.* p. 169 (1982).
3. N. Goto, Y. Ohno and H. Yano, *IEEE Trans. Electron Devices* **ED-37**, 1821 (1990).
4. Y. Ohno and N. Goto, *J. Appl. Phys.* **66**, 1217 (1989).
5. S. J. Chang and C. P. Lee, *IEEE Trans. Electron Devices* **40**, 698 (1993).
6. M. S. Birrittella, W. C. Seelback and H. Goronkin, *IEEE Trans. Electron Devices* **29**, 1135 (1982).
7. S. Selberherr, *Analysis and Simulation of Semiconductor Devices*. Springer, Wein (1984).
8. E. M. Buturla and P. E. Cottrell, *Solid-St. Electron.* **23**, 331 (1980).
9. L. G. Salmon, in *Proc. GaAs IC Symp. Tech. Dig.*, p. 289 (1991).
10. C. Kocot and C. A. Stolte, *IEEE Trans. Electron Devices* **ED-29**, 1059 (1984).
11. H. Yano, S. Kumashiro, N. Goto and Y. Ohno, *Tech. Dig. IEDM*, 151 (1989).