High-Performance TFTs With Si Nanowire Channels Enhanced by Metal-Induced Lateral Crystallization

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***Abstract*—Thin-film transistors with poly-Si nanowire (NW) channels enhanced by metal-induced lateral crystallization (MILC) are reported. The new device features a side-gate with self-aligned NW channels abutting the sidewalls of the gate structure. By adopting the MILC technique, the crystallinity of the NW channels is greatly enhanced, compared to those formed by solid-phase crystallization. As a result, the electrical performance of the devices could be significantly enhanced in terms of reduced subthreshold swing and threshold voltage as well as improved field-effect mobility.**

***Index Terms*—Metal-induced lateral crystallization (MILC), nanowires (NWs), thin-film transistors (TFTs).**

I. Introduction

POLYCRYSTALLINE silicon (poly-Si) thin-film transistors (TFT) are very attractive for applications to liquid-crystal display (LCD) drivers and three-dimensional electronics [1]. Several techniques, including excimer laser annealing (ELA) [2] and metal-induced lateral crystallization (MILC) [3], have been developed to form high-quality poly-Si layer with high carrier mobility, large grain size, and low defect density. Among these techniques, MILC seeded by nickel is particularly attractive for yielding superior poly-Si layers with good electrical characteristics that meet device application requirements.

On the other hand, FETs with nanowire (NW) channels have recently drawn a lot of attention for a number of applications, such as NW TFTs [4], memory devices [5], and biosensors [6]. By taking advantage of the high surface-to-volume ratio inherent in the structure, NWs can provide high surface sensitivity for sensing device applications [6], [7]. The preparation of NWs could be categorized into two types, namely: 1) top-down [7], [8] and 2) bottom-up [5], [6]. However, there remain certain distressing issues for either approach. For example, the top-down methods usually require costly equipment and cutting edge techniques, whereas the bottom-up methods may suffer from the uncontrollability of structural parameters, such as the length and diameter of NWs. Precise positioning of the NWs represents another major obstacle for reliable device fabrication. These issues may hinder practical applications and manufacturing of NW devices. Recently, Lin *et al.* [9] have proposed a simple and inexpensive approach to implement TFTs with poly-Si NW channels. The proposed structure overcomes all the major drawbacks previously mentioned. However, the new device was demonstrated on NWs formed by solid-phase crystallization (SPC) and was therefore susceptible to considerable grain boundaries and microstructural defects in the NW, which would unavoidably degrade device performance.

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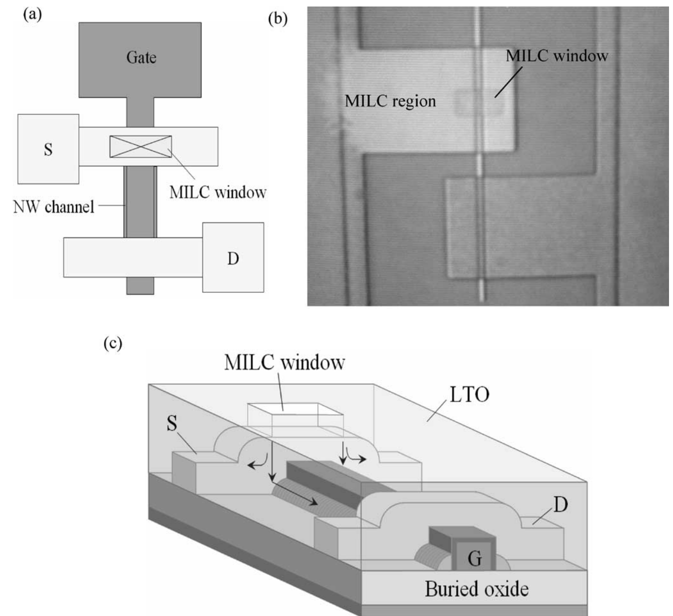

Fig. 1. (a) Top view of the layout, (b) optical microscopy image of MILC at 550 °C for 16 h, and (c) the schematic of poly-Si NW TFTs enhanced by MILC. The arrows indicate the MILC directions.

In this letter, we employ the MILC technique to the fabrication of the novel NW devices to further improve device performance. Because the grains formed by MILC are large and could be deliberately formed parallel to the channel direction, it becomes feasible to form Si NWs with nearly monocrystalline structures [10]. The experimental results indeed reveal much improved performance over SPC devices.

II. Device Fabrication

Basically, the fabrication flow follows that described in the previous report [10], with the addition of the implementation of the MILC process. The top and side views of the device structure are depicted in Fig. 1(a) and (c), respectively. In addition, Fig. 1(b) shows an optical micrograph of a fabricated device. As shown, a window is opened in the oxide layer overlying the source region. Before the MILC treatment, a 5-nm-thick Ni layer was deposited in the window area to serve

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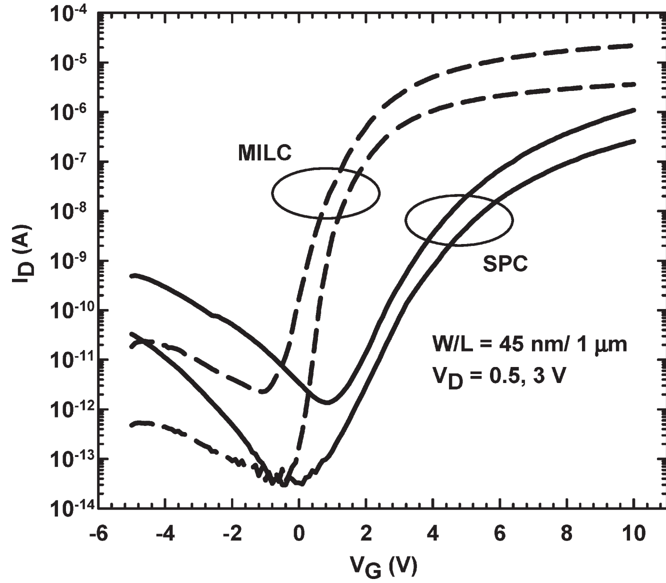

Fig. 2. Comparison of transfer characteristics between SPC and MILC TFTs with NW channels.

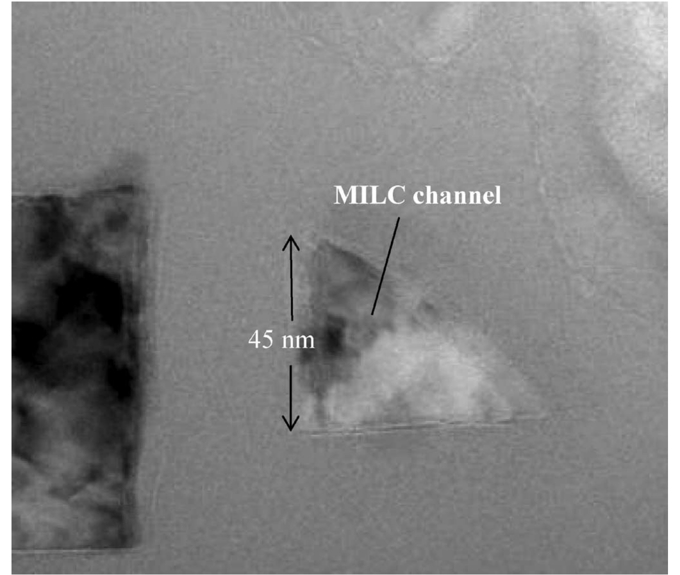

Fig. 3. TEM image of an MILC-crystallized transistor.

TABLE I
COMPARISONS OF DEVICE PARAMETERS BETWEEN SPC AND MILC TFTs

Parameters*	SPC TFT	MILC TFT
V_{th} (V)	8.2	2.0
S.S. (V/dec)	1.09	0.26
μ_{FE} (cm^2/V.s)	31	201
I_{off} (A)	1.37×10^{-12}	2.26×10^{-12}
I_{on}/I_{off}	7.9×10^{5}	9.7×10^{6}
N_t (cm^{-2})	2.35×10^{12}	5.01×10^{11}

*All parameters were extracted at V_D = 0.5 V except fot the off-state, I_{off}, and ON/OFF ratio, I_{on}/I_{off}, which were extracted at V_D = 3 V. I_{off} is defined as the minimum drain current for convenience.

as the seeding layer. Lateral crystallization was carried out at 550 °C for 16 h in an N_2 ambient, which also served the purpose of dopant activation. The unreacted Ni was then removed by an H_2SO_4/H_2O_2 solution. As shown, the portion surrounding the window with different colors indicates the region that has been crystallized. For comparison, control samples that were crystallized by SPC at 600 °C for 24 h were also fabricated.

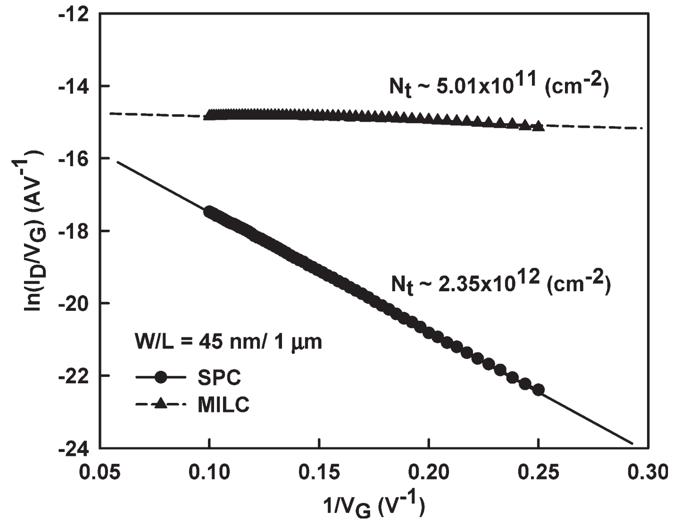

Fig. 4. Plot of $\ln(I_D/V_G)$ versus $(1/V_G)$ and the extracted effective trap density of SPC and MILC TFTs. I_D was measured at $V_D = 0.5$ V.

III. RESULTS AND DISCUSSION

Transfer characteristics of SPC and MILC poly-Si TFTs with NW channels are compared in Fig. 2. The devices have a nominal channel length L of 1 μm and a channel width W of 45 nm. The gate oxide is 40 nm thick. Detailed device characteristics are summarized in Table I. The field-effect mobility extracted from maximum transconductance is 201 $\text{cm}^2/\text{V} \cdot \text{s}$ for the MILC device, which is much higher than the 31 $\text{cm}^2/\text{V} \cdot \text{s}$ of the SPC counterpart. In addition, the MILC TFT has better subthreshold swing (SS, about 0.26 V/dec) and higher on/off current ratio (about 10^7). These results clearly indicate that NW channels formed by MILC are suitable for high-performance device applications. We believe this is because the grain is large, needlelike, and parallel to the channel for the MILC device. Fig. 3 shows the cross-sectional transmission electron microscopy (TEM) image of a fabricated device with MILC channels. As compared with the SPC sample characterized in our previous work [9], the film crystallinity is significantly improved, demonstrating the effectiveness of the MILC process in NW structures. When the size of the NW channel is shrunk to a dimension comparable to the grain size, a quasi-single-crystalline Si NW could be obtained [10].

Fig. 4 shows the trap densities (N_t) extracted from the slope of $\ln(I_D/V_G)$ versus $(1/V_G)$ according to the grain-boundary trap model [11], [12]. It can be found that the N_t of the MILC TFT is about four times smaller than that of the SPC TFT. This result further confirms that the MILC technique results in much fewer grain boundaries and microstructural

defects in the NW channel. It should also be noted that the MILC NW devices with high mobility and on/off ratio could provide favorable conductivity and switching characteristics suitable for high-sensitivity chemical and biological sensor applications.

Though the aforementioned enhancement in device performance is magnificent, the OFF-state leakage of the devices remains high despite the MILC treatment. This is likely to be due to potential Ni contamination. The formation of silicide at the grain boundaries during the MILC process has been reported previously [13], which would aggravate the leakage. This drawback could be alleviated by adoption of a long Ni-offset structure [14] or by proper annealing conditions [13]. Through further posttreatment (e.g., hydrogenation or high-temperature annealing), further improvement in electrical performance is expected.

IV. Conclusion

In summary, by adopting the MILC process to the newly proposed TFTs with Si NW channels, excellent device performance could be obtained. The fabricated devices exhibit large on current, high on/off ratio, low ss, and favorable output characteristics. The extracted effective trap density and mobility further confirm that fewer defects and good crystallinity in the NW channels are indeed achieved by MILC. The MILC-enhanced NW devices with good electrical characteristics and low-cost processes could be highly promising for future practical manufacturing and applications.

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