Influence of Bias-Temperature Stressing on the Electrical Characteristics of SiOC:H Film with Cu/TaN/Ta-Gated Capacitor

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Experiments on bias-temperature stressing, capacitance-voltage measurements, current-voltage characteristics, and time-dependent dielectric breakdown were performed to evaluate the reliability of Cu and low-k SiOC:H integration. A high leakage current of $\sim 8 \times 10^{-10}$ to 2×10^{-8} A/cm^2 at 1 MV/cm in SiOC:H dielectrics in a Cu-gated capacitor, and a lower 2×10^{-10} to 5×10^{-10} A/cm^2 at 1 MV/cm in a Cu/TaN/Ta-gated capacitor, were observed at evaluated temperatures. The drift mobility of the Cu^+ ions in the Cu/TaN/Ta-gated capacitor was lower than that in a Cu-gated capacitor. A physical model was developed to explain the observed kinetics of Cu^+ ions that drift in Cu-gated and Cu/TaN/Ta-gated capacitors. The electric field in the Cu-gated MIS capacitor in the cathode region is believed to be increased by the accumulation of positive Cu^+ ions, which determines the breakdown acceleration. Good Cu^+ ions drift barrier layers are required as reliable interconnects using thin TaN and Ta layers. Additionally, Schottky emission dominates at low electric fields, $E < 1.25$ MV/cm, and Poole-Frenkel emission dominates at high fields, $E > 1.5$ MV/cm.

Key words: Bias-temperature stressing, capacitance-voltage, time-dependent dielectric breakdown, Cu^+ ions, ion drift, SiOC:H

INTRODUCTION

As devices in integrated circuits continue to be reduced in size, the resistance-capacitance (RC) delay of the interconnection increases.[1,2] In practice, aluminum or aluminum alloys are employed as interconnect metals, and plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 has been used to form the intermetallic dielectric material in integrated circuits (ICs). Yet, the resistivity (ρ) of aluminum ($\rho \approx 2.7\ \mu\Omega$ cm) and the dielectric constant of PECVD SiO_2 ($k \approx 3.9$) are unsuitable for next-generation interconnections. A low-k ($k < 3.9$) intermetallic dielectric and a metal with a low resistivity, such as copper ($\rho \approx 1.7\ \mu\Omega$ cm), are required in next-generation ICs to ensure that the interconnection system performs well with minimal RC delay.[3,4] Hydrogenated silicon oxycarbide (SiOC:H), formed by high-density plasma chemical vapor deposition (HPDCVD), has become the leading candidate for replacing SiO_2, because of its low dielectric constant ($\sim$2.9) and excellent interlayer features when used in damascene interconnects.[5] Its properties were studied in detail and are presented elsewhere.[5] HDPCVD dielectrics with excellent electric properties outperform those formed by other methods; our recent work described the formation of dielectrics.[6,7]

Meanwhile, Cu interconnections have several disadvantages when used in device process technology. For instance, the Cu film is easily oxidized, and Cu atoms or ions easily diffuse into the low-k interlayer dielectric film by thermal annealing or under the influence of an electric field, causing the interconnection to fail.[8] Hence, a diffusion barrier and an adhesion promoter in the copper interconnect is required. This barrier must be deposited with good step coverage to offer a high aspect ratio and subsequently grow Cu on it. The barrier layer must also be as thin as possible, so as not to degrade the electrical performance of the Cu wiring. Diffusion barriers of refractory metals and their nitrides in copper metallization have been extensively investigated, because of their superior thermal stability

(Received January 3, 2006; accepted January 27, 2006)

and high conductivity, such as those of Ti-N,[9] Ta-N,[10] and W-N.[11] Tantalum and its nitrides have been used in the current fabrication of devices because they have better thermal stability and chemical inertness than other transition-metal nitrides when in contact with copper. Although Cu diffusion and drift in various dielectric materials have been extensively examined,[12–15] a few studies have addressed electrical behavior and reliability of SiOC:H with a diffusion barrier. In this study, very thin TaN/Ta films and low-k SiOC:H films in metal-insulator-semiconductor (MIS) capacitors are investigated and leakage current conduction mechanisms proposed. The reliability is examined in terms of bias-temperature-stress (BTS) and time-dependent dielectric breakdown (TDDB). Furthermore, the barrier effectiveness of Ta and TaN films is studied using the capacitance-voltage method.

EXPERIMENTAL PROCEDURES

Phosphorus-doped n-type silicon (100) wafers were utilized as substrates. The wafers were degreased in organic baths and chemically etched with dilute HF solution to remove native oxide. A 20-nm-thick thermal SiO_2 layer was initially grown on Si to produce a high-quality dielectric–semiconductor interface. The SiOC:H film, 200 nm thick, was fabricated using an inductively coupled plasma (ICP) HDPCVD system, with trimethysilane [$Si(CH_3)_3H$, 3MS] and nitrous oxide (N_2O) as precursors at 10 and 90 sccm, respectively. Radiofrequency (rf) power and substrate temperature were 500 W and 300°C, respectively. Electrodes were sputtered on top of the SiOC:H dielectrics using a shadow mask, which was used to yield a circular metal gate with an area of about 3.14×10^{-2} mm^2. Ta and TaN layers, 20 nm thick, were deposited by sputtering from a Ta metal (99.95% purity) target at a dc power of 500 W. The atmospheres in which Ta and TaN were sputtered were 20 sccm pure Ar and a 20/5 sccm Ar/N_2 mixture, respectively. Finally, a 300-nm-thick copper film was prepared by sputtering a pure Cu metal target, at a dc power of 1500 W, and then reactively sputter-depositing a 50-nm-thick TaN layer on the Cu surface to prevent oxidation of the Cu electrode during the subsequent thermal process. Figure 1 presents the structures of Cu-gated and Cu/TaN/Ta-gated MIS capacitors in SiOC:H dielectrics. A 200-nm-thick Al backside sputtering produces an electrical contact during the measurement.

The probe station with a 6-in. water-cooled chuck was situated in a hot chuck system, which was a hermetically sealed aluminum enclosure designed specifically for Cu drift studies. The room temperature capacitance-voltage (C-V) characteristics at 1 MHz were obtained using a Keithley package (Cleveland, OH) 82 system at a voltage sweep rate of 0.25 V/s. Current density-electric field (J-E) and current-time (I-t) characteristics were measured using a Hewlett-Packard (HP4156A) semiconductor parameter analyzer and a Keithley package 82 system to supply bias during the BTS experiments. After the test samples were loaded, the hot chuck was purged with N_2 for at least 1 h before high-temperature tests were conducted. These precautions minimize oxidation of Cu electrodes during high-temperature testing and prevent the dielectrics from absorbing ambient moisture during testing. BTS tests were performed at 175–250°C in electric fields of up to 1.5 MV/cm. In high-temperature testing, samples were initially heated to the target temperatures, and then the bias was applied for particular periods, ranging from a few minutes to several hours. After the period of stress or the samples had broken down, the hot chuck was cooled to room temperature. The voltage sweeping direction was set such that a MIS capacitor starts from the inversion region and ends in the accumulation region to prevent the deep depletion of capacitors.

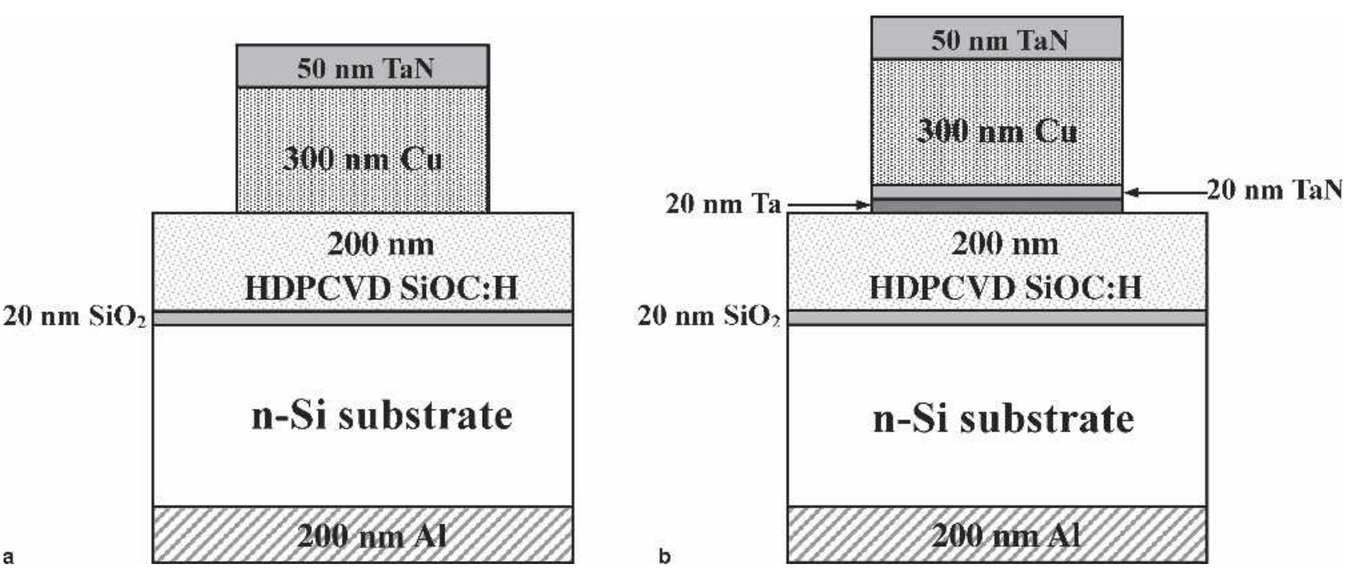

Fig. 1. Structures of (a) Cu-gated and (b) Cu/TaN/Ta-gated MIS capacitors in SiOC:H dielectrics.

RESULTS AND DISCUSSION

The drift diffusion of Cu^+ ions is studied by determining the shift in the flat-band voltage (V_{FB}) in the C-V curve for processed Cu gate capacitors before and after BTS. V_{FB} is determined by the number of charges in the dielectric and at the dielectric/Si interface.[16] The contribution of the flat band voltage shift of Cu^+ ions ($\Delta V_{FB[Cu^+]}$) after positive bias BTS is applied can be extracted by subtracting the flat-band voltage shift of a Cu/TaN/Ta-gated capacitor ($\Delta V_{FB[Cu/TaN/Ta]}$) from that of a Cu-gated capacitor ($\Delta V_{FB[Cu]}$), using Eq. 1, to demonstrate the effectiveness of the barrier layers and the Cu injection mechanism.

$$\Delta V_{FB[Cu^+]} = \Delta V_{FB[Cu]} - \Delta V_{FB[Cu/TaN/Ta]} \quad (1)$$

Therefore, a positive flat-band voltage shift reveals an increase in the positive charge (Cu^+) in the SiOC:H film. Figure 2 shows the flat-band voltage shift of the Cu^+ ions ($\Delta V_{FB[Cu^+]}$) vs. stressing time at various temperatures in the electric field of 1.5 MV/cm, using Eq. 1. Every data point is a mean of results from 10 tested capacitors. MIS gate capacitors stressed at 175 and 200°C exhibit minor changes of $\Delta V_{FB[Cu^+]}$ as the stressing time changes, while capacitors stressed at 225 and 250°C have a higher $\Delta V_{FB[Cu^+]}$ of Cu^+ ions. The general trend clearly suggests the continuous injection of Cu^+ ions and the rapid injection of Cu^+ ions at high temperature.

The drift rate of Cu^+ ions is determined from the gradients of the lines fitted using Eq. 2, to quantify the diffusion.[17]

$$\frac{d[Cu^+]}{dt} = -\frac{C_{ox}}{q}\frac{d\left(\Delta V_{FB[Cu^+]}\right)}{dt} \quad (2)$$

where $[Cu^+]$ is the Cu^+ ion concentration per unit area; C_{ox} is the dielectric stack capacitor per unit area, and q is the magnitude of the charge on an electron (1.6×10^{-19} C). This equation assumes that the Cu^+ ions drifted to the SiO_2/Si interface. The initial drift rate is determined by the change in the electric field in the dielectric with time, due to the accumulation of Cu^+ ions. Figure 3 displays Arrhenius plots of the drift rates in the different MIS capacitors. Increasing the temperature increases the drift rate of Cu^+ ions in the material. Moreover, the drift rates of Cu^+ ions in HDPCVD SiOC:H layers are markedly lower than those in PECVD SiOC:H layers.[18] These characteristics—the low hydrogen (low defect sites) and the high oxygen concentration (enhanced porous densities)—of SiOC:H films deposited on the HDPCVD system reduce the number of carrier-trapping sites and, therefore, slightly reduce the drift rate of Cu^+ ions.[5]

The drift of Cu^+ ions into the SiOC:H film was examined using J-E analysis. The J-E characteristics of Cu-gated and Cu/TaN/Ta-gated MIS capacitors were measured at 175°C, 200°C, 225°C, and 250°C and are plotted in Fig. 4a and b, respectively. The Cu-gated MIS capacitor exhibits consistently higher leakage current (8×10^{-10}–2×10^{-8} A/cm^2 at 1 MV/cm) than a Cu/TaN/Ta-gated MIS capacitor (2×10^{-10}–5×10^{-10}A/cm^2 at 1 MV/cm) at the same temperature. The higher leakage current of a Cu-gated MIS capacitor is probably related to the ionization and injection of Cu^+ ions into dielectrics. According to a physical model introduced elsewhere,[18,19] Cu atoms are ionized into Cu^+ ions at gate interface under positive gate bias, and these Cu^+ ions are then injected into the dielectrics, leaving behind electrons collected using an external instrument. In an external electric field, the flux of Cu^+ ions from the gate to the SiO_2/Si interface and the electrons collected by an external instrument tend to increase the leakage current. The difference between the leakage current densities of the Cu-gated and Cu/TaN/Ta-gated MIS capacitors (J_{diff}) were measured and are given in Fig. 5. J_{diff} increases with electric field and temperature, indicating that Cu^+ ion drift into the HDPCVD SiOC:H is the probable cause of larger J_{diff}. Based on the

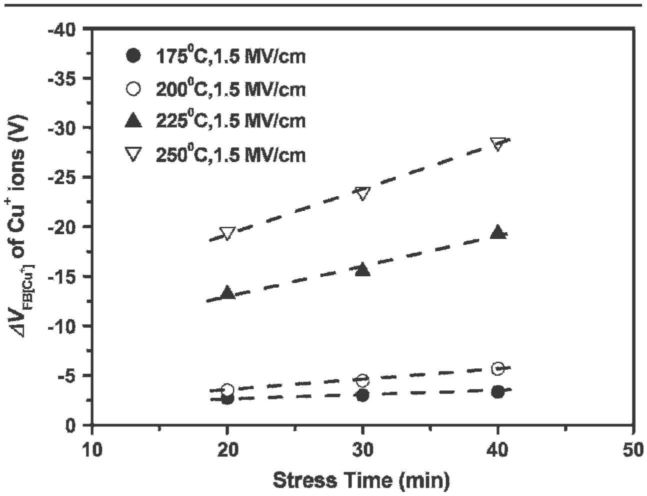

Fig. 2. Flat-band voltage shift $\Delta V_{FB[Cu^+]}$ of Cu^+ ions vs. BTS temperature under various stress time at 1.5 MV/cm.

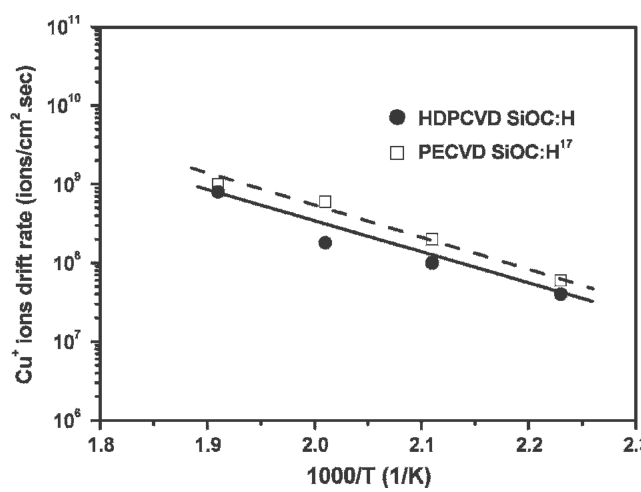

Fig. 3. Arrhenius plot of estimated drift mobility of Cu^+ ions in the SiOC:H dielectrics vs. 1000/T.

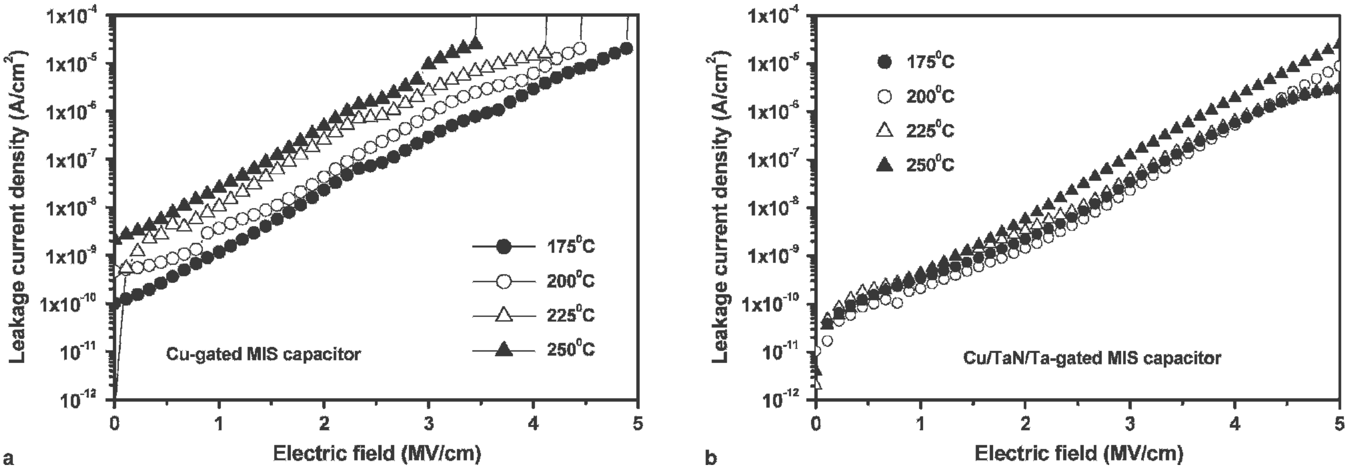

Fig. 4. Leakage current density-electric field characteristics of (a) Cu-gated and (b) Cu/TaN/Ta-gated MIS capacitors at various temperatures.

assumption that the drifting of Cu^+ ions into SiOC:H determines $\Delta V_{FB[Cu^+]}$ in BTS/C-V analysis and J_{diff} in J-E analysis, $\Delta V_{FB[Cu^+]}$ should be linearly correlated with J_{diff} according to

$$\Delta V_{FB[Cu^+]}[t] = \frac{Q_{Cu}[t]}{C_{ox}} \propto \frac{1}{C_{ox}}\int_0^t J_{diff}(\tau)dt \qquad (3)$$

where C_{ox} is the capacitance per unit area, and $Q_{Cu}(t)$ is the accumulated Cu^+ ions charge density. Figure 6 compares J_{diff} at 1.5 MV/cm (30 V), which is the voltage used in the BTS/C-V test, to $\Delta V_{FB[Cu^+]}$ after 40 min. of BTS. A good linear correlation is found between $\Delta V_{FB[Cu^+]}$ and J_{diff}, revealing that J_{diff} is related to the number of injected Cu^+ ions.

Several mechanisms may govern the conduction of the leakage current in the Cu/TaN/Ta-gated MIS capacitor, including Schottky emission, the Poole-Frenkel effect, electronic hopping conduction and tunneling.[15,20–22] Schottky emission is modeled as[22]

$$J = AT^2 \exp\left(-\frac{q\phi_0}{kT}\right) \exp\left(\frac{\beta}{kT}E^{1/2}\right) \qquad (4)$$

where A is a constant, T represents the absolute temperature, q is the electronic charge, ϕ_0 is the barrier height, k is the Boltzmann constant, and β is given by

$$\beta = \left(\frac{q^3}{4\pi\varepsilon_0\varepsilon}\right)^{1/2} \qquad (5)$$

where ε_0 is the permittivity of free space and ε is the high-frequency dielectric constant. Figure 7a plots ln(J) as a function of $E^{1/2}$. The figure demonstrates that different conduction mechanisms dominate in different electric-field regimes. Two linear regions are observed, and the slope yields the corresponding effective dielectric constant in the electric field $E < 1.25$ MV/cm. The figure demonstrates that the dominant conduction mechanism in the Cu/TaN/Ta-gated MIS capacitor is Schottky emission in the electric field $E < 1.25$ MV/cm, at which electrons from the cathode overcome the Ta/SiOC:H energy barrier before they are emitted. Figure 7b presents Richardson plots of $\ln(J/T^2)$ vs. (1000/T) associated with a close examination of Schottky emission transport, for electric fields between 0.5 and 1.25

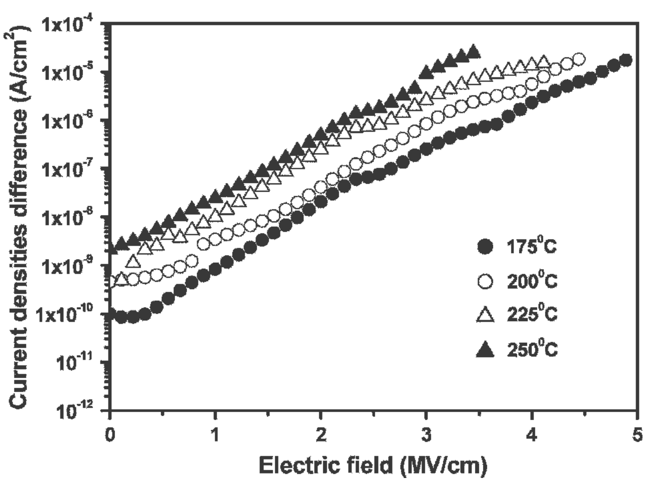

Fig. 5. Leakage current densities difference J_{diff} of Cu-gated and Cu/TaN/Ta-gated MIS capacitors at various temperatures.

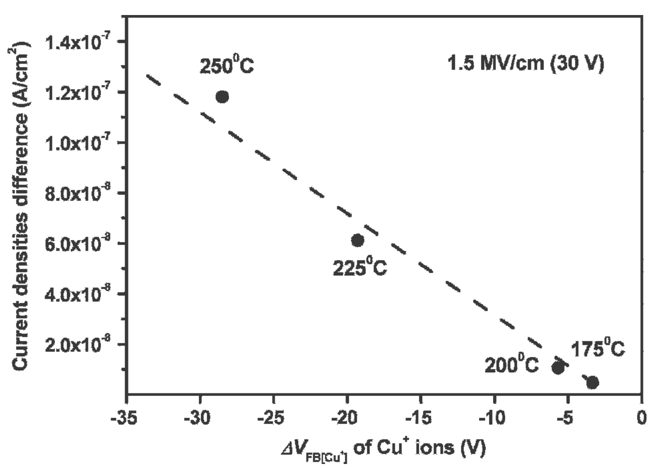

Fig. 6. Leakage current densities difference J_{diff} of Cu-gated and Cu/TaN/Ta-gated MIS capacitors at 1.5 MV/cm (30 V) vs. $\Delta V_{FB[Cu^+]}$ of Cu^+ ions after 40 min. at 30V BTS at various temperatures.

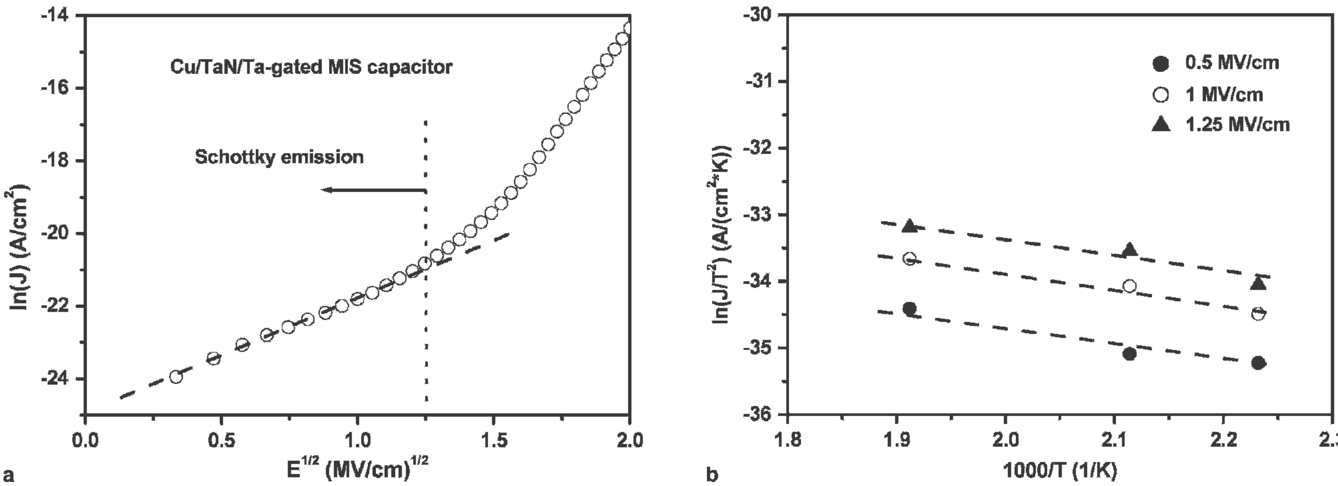

Fig. 7. (a) ln(J) vs. $E^{1/2}$ and (b) ln(J/T^2) vs. 1000/T for Cu/TaN/Ta-gated MIS capacitors at various measured temperatures in electric field E < 1.25 MV/cm.

MV/cm. The straight lines fitted to the data points are quite consistent with Schottky emission. The leakage current density increases with the measured temperature and the electric field because when an electron enters the SiOC:H, it generates an image field that adds to and subtracts from the barrier field, thus reducing barrier height and increasing current.

When electric field E > 1.5 MV/cm, electrical conduction is governed by Poole-Frenkel emission, which is described by[22]

$$J = CE\exp\left(-\frac{q\phi_0}{kT}\right)\exp\left(\frac{\beta_{PF}}{kT}E^{1/2}\right) \quad (6)$$

where C is a constant and β_{PF} is defined by

$$\beta_{PF} = \left(\frac{q^3}{\pi\varepsilon_0\varepsilon}\right)^{1/2} \quad (7)$$

Figure 8a plots ln(J/E) as a function of $E^{1/2}$. The gradient in the linear region yields the corresponding effective dielectric constants in electric field E > 1.5 MV/cm, the value of which is close to that obtained from the C-V measurement. Therefore, Poole-Frenkel emission is deduced to dominate in electric field E > 1.5 MV/cm. The leakage current increases with the temperature, as shown in Fig. 8b. Poole–Frenkel emission results from the field-enhanced excitation of trapped electrons into the conduction band of the dielectric and its existence in Cu/TaN/Ta-gated MIS capacitor indicates the presence of electron traps. In fields of over 1.5 MV/cm, electrons in SiOC:H bulk traps absorb sufficient energy to be excited to the conduction band and Poole-Frenkel emission then dominates conduction.

The impact of Cu^+ ions on breakdown has been examined by comparing the TDDB test results of Cu-gated and Cu/TaN/Ta-gated MIS capacitors in SiOC:H dielectrics. Figure 9 plots the I-t characteristics of the SiOC:H MIS capacitors at 200–250°C and 2.5 MV/cm. At the beginning of the stress test, the leakage current declined. The decrease in the current in the first stage is believed to be caused by electron trapping in the dielectric films.[23,24] After the majority of the electron traps have been filled, the leakage currents decrease during the

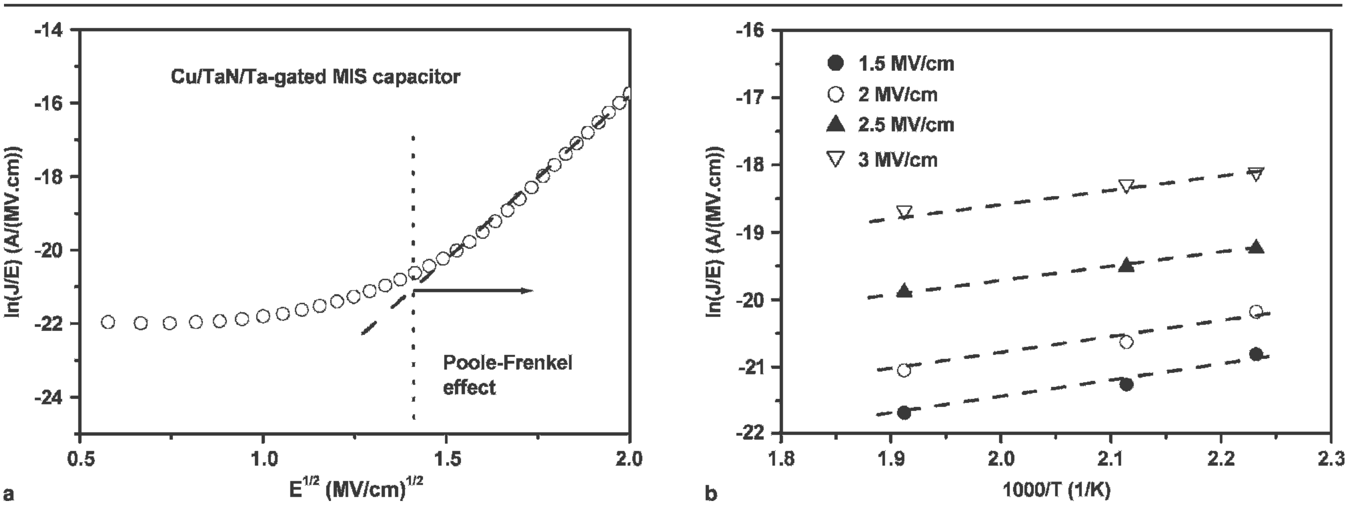

Fig. 8. (a) ln(J/E) vs. $E^{1/2}$ and (b) ln(J/E) vs. 1000/T for Cu/TaN/Ta-gated MIS capacitors at various measurement temperatures in electrical field E > 1.5 MV/cm.

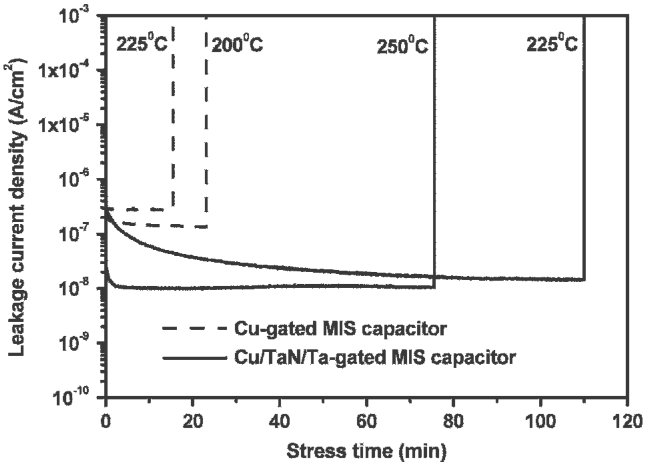

Fig. 9. Current-time characteristics of the Cu-gated and Cu/TaN/Ta-gated MIS capacitors in the electric field of 2.5 MV/cm at various temperatures.

middle stage. However, the leakage current rapidly increased and fatal breakdown occurred after stress was applied for a longer period. The Cu-gated capacitor has a higher leakage current than the Cu/TaN/Ta-gated capacitor under the same test conditions. The Cu/TaN/Ta-gated MIS capacitor was found to exhibit a time-to-breakdown value (t_{BD}) of over 75 min. at 250°C, longer than of the Cu-gated MIS capacitor, which broke down after 25 min. at 200°C. In the Cu-gated capacitor, the data reveals that the leakage curve during TDDB increases greatly just before breakdown due to degradation of the SiOC:H film. Li et al. reported that the leakage curve may not increase before the breakdown even if there are Cu^+ ions.[25] Therefore, the higher leakage current of the Cu-gated capacitor is believed to be caused by defects (such as moisture) in the samples due to process and absence of a passivation layer protecting the SiOC:H film.

Physical models previously presented by other researchers suggest that Cu atoms are thermally ionized at the Cu-dielectric interface, leaving behind free electrons, while the Cu^+ ions drift toward the substrate under the influence of the applied positive bias.[12,26] Figures 10a and b show the injection of Cu^+ ions in Cu-gated and Cu/TaN/Ta-gated MIS capacitors, respectively. The physical model displayed in Fig. 10a describes the drift kinetics of Cu^+ ions. A positive electric field ionizes Cu atoms and then injects the resulting Cu^+ ions into the SiOC:H dielectrics, generating leakage currents. They accumulate at the interface, setting up an uncompensated positive space charge near the Si substrate, as indicated by the shift in C-V analyses. Hence, the dielectric conduction and valence band edges are distorted such that the magnitude of electric field is increased while Cu^+ ions accumulate in the dielectrics. In the absence of Cu^+ ions, however, the electric field of a Cu/TaN/Ta-gated MIS capacitor is distributed uniformly, as presented in Fig. 10b. A lower Cu ionization rate at the Cu-dielectric interface and a lower Cu^+ ions drift rate in the dielectric are desired to slow the rate of accumulation of Cu^+ ions in the dielectric and thus increase t_{BD}.

CONCLUSIONS

The drift of copper Cu^+ ions into a SiOC:H film, which is a promising low-k material for use in interlayer dielectrics in ultra-large-scale integrated circuit interconnects, was examined using BTS/C-V and J-E plots at elevated temperatures and in TDDB tests. The physical model demonstrates that Cu^+ ions significantly accelerate the breakdown of SiOC:H films, and the buildup of positively charged Cu^+ ions in the dielectric cathode region is believed to enhance the local electric field and accelerate thermochemical breakdown process, distorting the dielectric conduction and valence band edges, and increasing the magnitude of the electric field. Integrating Cu in low-k SiOC:H with poor Cu resistance involves thin TaN and Ta diffusion barrier layers, which effectively provide a low leakage current density of around 2×10^{-10} A/cm^2 at 1 MV/cm, a high breakdown field at $E > 4$ MV/cm of over 1.0×10^{-6}

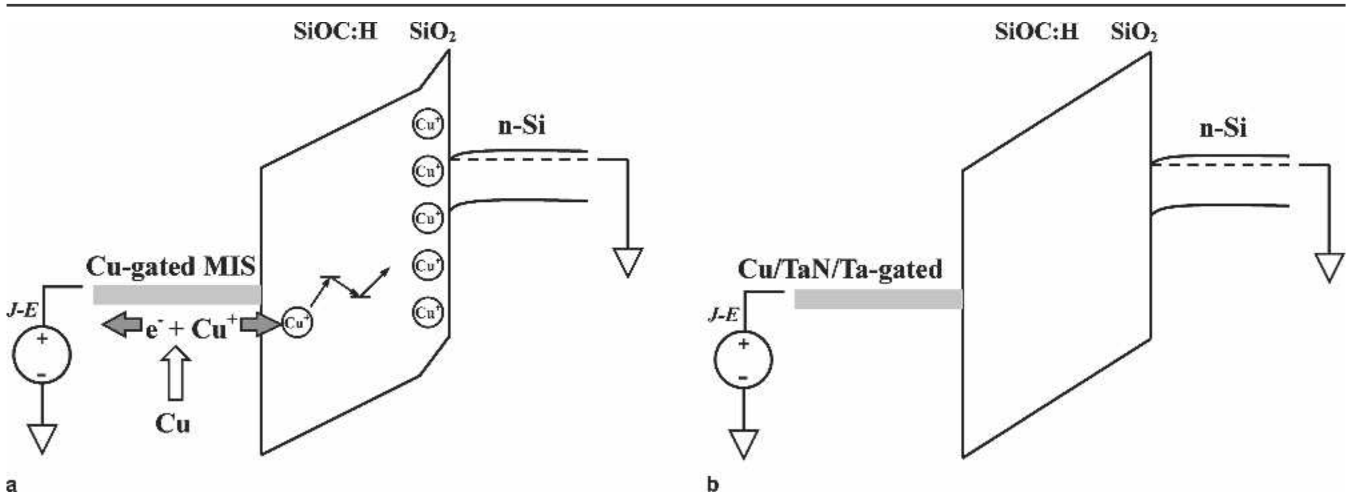

Fig. 10. Schematic band diagram of injection of Cu^+ ions in (a) Cu-gated and (b) Cu/TaN/Ta-gated MIS capacitors under positive gate bias.

A/cm^2, and a low Cu^+ ion drift rate at various temperatures in the Cu/TaN/Ta-gated MIS capacitor.

ACKNOWLEDGEMENTS

The work was financially supported by the National Science Council of the Republic of China under Contract No. NSC 94-2215-E-492-009 and in part by the Ministry of Economic Affairs of the Republic of China under Contract No. 93-EC-17-A-08-S1-0003. Technical support from the National Nano Device Laboratories is greatly acknowledged.

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