CMOS Dual-Wideband Low-Noise Amplifier in 3.1GHz-4.9GHz and 6.0GHz-10.3GHz for Ultra-Wideband Wireless Receiver

Zhe-Yang Huang[1], Che-Cheng Huang[2], Chun-Chieh Chen[3] and Chung-Chih Hung[1]

[1] Dept. of Communication Engineering, National Chiao Tung University, Hsin-Chu, Taiwan
[2] Instrument Technology Research Center, NARL, Hsin-Chu, Taiwan
[3] Dept. of Electronic Engineering, Chung Yuan Christian University, Chung-Li, Taiwan

Abstract - **In this paper a CMOS dual-wideband low-noise amplifier (LNA) is designed for ultra-wideband (UWB) wireless receiver radio system. The design consists of a wideband input impedance matching network, two stage cascode amplifiers with shunt-peaked load, a notch filter and an output buffer for measurement purpose. It is simulated in TSMC 0.18um standard RF CMOS process. The LNA gives 13.66dB maximum power gain between 3.0GHz-4.9GHz and 10.34dB maximum power gain between 6.0GHz-10.3GHz while consuming 24.07mW through a 1.8V supply. Over the 3.1GHz-4.9GHz frequency band and the 6.0GHz-10.3GHz, a minimum noise figure is 2.6dB and 3.8dB. Input return loss lower than -8.31dB in all bandwidth have been achieved.**

Index Term – **RFIC, Ultra-Wideband, UWB, Notch Filter, LNA and Low-Noise Amplifier.**

I. INTRODUCTION

Since the approval of the ultra-wideband (UWB) radio technology for low power wireless communication application in February, 2002, [1] UWB systems has become an increasingly popular technology which is capable of transmitting data over a wide spectrum of frequency with very low power and high data rate. Although the IEEE UWB standard (IEEE 802.15.3a [2]) has not been completely defined, two major proposed solutions, MB-OFDM and DS-UWB, are all allowed to transmit in a band between 3.1GHz-10.5GHz and 3.1GHz-9.6GHz. The 1st generation device in commercial applications for ultra-wideband radio systems which shows in Fig.1(a) and Fig.1(b). The band definition of MB-OFDM is illustrated in Fig.1 (a) which extended from 3168MHz to 10296MHz and the band definition of DS-UWB are from 3100MHz to 4900MHz and 6000MHz to 9700MHz. The bandwidth of MB-OFDM is containing Group-A, Group-C and Group-D. The Group-B is not considered in current UWB system which caused by the U-NII band and WLAN (IEEE 802.11a). The bandwidth of DS-UWB is with Low-Band and High-Band which is in Fig.1 (b).

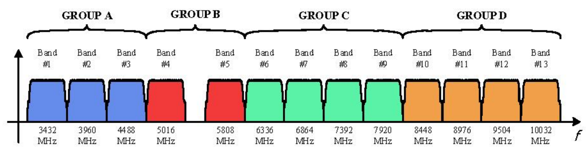

Fig.1 (a) Groups of MB-OFDM

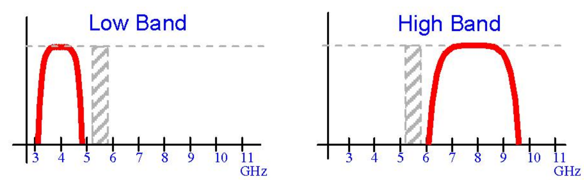

Fig.1 (b) Low Band and High Band of DS-UWB

This paper is focused on the design and implementation of dual-wideband systems which avoids the U-NII band and coexists with MB-OFDM and DS-UWB radio systems. The dual-wideband low–noise amplifier for ultra-wideband receiver is implemented in a 0.18um Standard RF CMOS Process.

II. DESIGN OF ULTRA-WIDEBAND LNA

The proposed low-noise amplifier is shown in Fig.2 which consists of wideband input impedance matching networks, two stages cascode amplifier with shunt-peaked load, a notch filter and an output buffer. The constituent of wideband matching networks are inductors L_1, L_2 and L_s and transistor M_1. First stage cascoded amplifier are transistors M_1 and M_2 with shunt-peaked load consists of inductors L_{load1}, R_{load1}, and the second stage cascoded amplifier are transistors M_3 and M_4 with shunt-peaked load consists of inductor L_{load2} and R_{load2}. The notch filter is between first stage and second stage amplifier. A common-drain amplifier is a good choice of wideband output impedance matching for measurement purpose.

1-4244-0797-4/07/$20.00 © 2007 IEEE

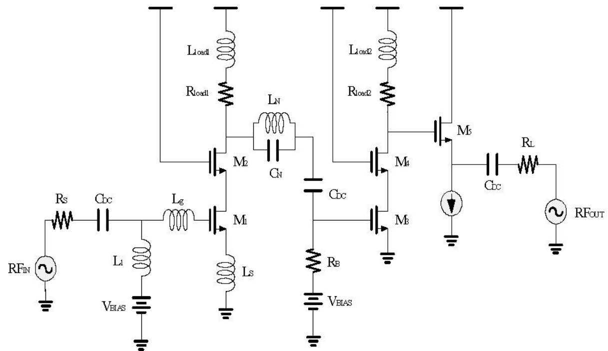

Fig.2 Proposed Low-Noise Amplifier for UWB System

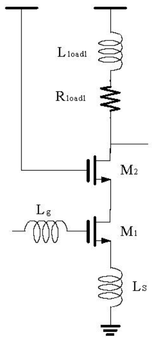

Fig. 3 Cascode Amplifier with Shunt-Peaked Load

A. Wideband Input Impedance Matching

Wideband input impedance matching is a tough design challenge in ultra-wideband system. Some excellent wideband input impedance matching solutions are proposed in [3]. Equation (1) is the parallel LC-tank in RF signals input path which resonates a centred frequency f_{r1} shows in equation (2) where L_1 is the inductor at bias and C_{L1} is the parasitic capacitors. Inductive source degeneration also resonate a centred frequency f_{r2} which are equations (3) and (4) where L_g is the gate inductor, L_s is the source inductor and the C_{gs1} is the gate-source parasitic capacitor in transistor M_1. The wideband input impedance matching is composed of these two centred frequencies f_{r1} and f_{r2}.

$$Z_1 = sL_1 \,||\, \frac{1}{sC_{L1}} = \frac{sL_1}{1+s^2L_1C_{L1}} \quad (1)$$

$$f_{r1} = \frac{1}{2\pi\sqrt{L_1C_{L1}}} \quad (2)$$

$$Z_2 = sL_g + \frac{1}{sC_{gs1}} + \frac{g_m}{C_{gs1}}L_S \approx sL_g + \frac{1}{sC_{gs1}} + \omega_T L_S \quad (3)$$

$$f_{r2} = \frac{1}{2\pi\sqrt{L_gC_{gs1}}} \quad (4)$$

B. Shunt-Peaked Amplifier

The cascoded shunt-peaked amplifier is easy to reach wide bandwidth which shown in Fig. 3. Cascoded amplifier eliminates the Miller effect on input transistor to achieve high-frequency performance. Voltage gain A_{L1} is a band-pass filter type which is expressed in equation (5).

$$A_{L1} \approx g_{m1} \cdot \frac{R_{L1} + sL_{L1}}{s^2C_{L1}L_{L1} + sC_{L1}L_{L1} + 1} \quad (5)$$

Amplifier with shunt-peaking load, the power gain and the bandwidth is determined by the resistance of load, where the resistance is small then the quality factor (Q) is high and on the contrary the quality factor is low. The higher quality factor makes higher power gain but narrower bandwidth, the lower quality factor makes lower power gain but wider bandwidth which shows in Fig. 4.

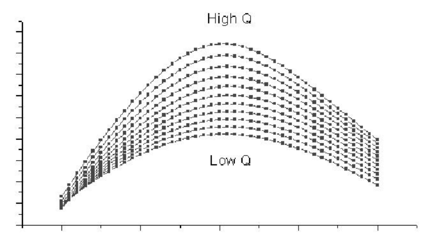

Fig. 4 Power Gain and Bandwidth V.S Quality Factor

C. Wideband Amplifier Design

Wide bandwidth amplifier is shown in Fig. 5 which consists of two stages of shunt-peaked amplifiers. The power gain is not good enough when the bandwidth is wide to reach whole bandwidth of the single stage shunt-peaked amplifier. Therefore, two stages of shunt-peaked amplifiers could achieve higher power gain and wider bandwidth.

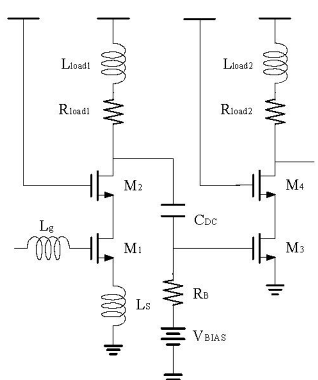

Fig. 5 Wide Bandwidth Amplifier

The first stage shunt-peaked amplifier is providing the power gain of lower frequency, and the second stage shunt-peaked amplifier is providing the power gain of the higher frequency, which are the blue lines in Fig. 6. And final power gain of the low-noise amplifier is the red line in Fig. 6 which is the result of two stage shun-peaked amplifiers in gain compensated.

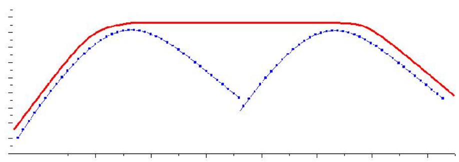

Fig. 6 Gain Compensated of Two Stages Amplifiers

D. Notch Filter Design

There are some signals which are larger than UWB signals in U-NII band, such as WLAN (IEEE 802.11a), and dodging these large interferences is very indispensable. A notch filter is proposed in dual-wideband low-noise amplifier which is located among first stage amplifier and second stage amplifier shown in Fig. 7. This is a LC-tank series in RF signal path, the impedance is declared in equation (6) and the centred frequency f_N is expressed in equation (7). The centred frequency f_N is design at 5.5GHz to reject the interference from 5.1GHz to 5.9GHz, and the final power gain is shown in Fig.8. The green line is the final power which rejects 5.1GHz to 5.9GHz.

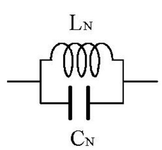

Fig. 7 Notch Filter among First and Second Stage Amplifier

$$Z_N = sL_N \,||\, \frac{1}{sC_N} = \frac{sL_N}{1+s^2 L_N C_N} \quad (6)$$

$$f_N = \frac{1}{2\pi\sqrt{L_N C_N}} \quad (7)$$

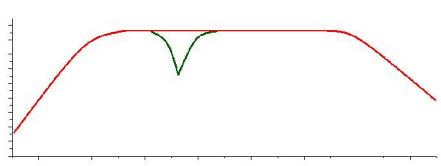

Fig. 8 Power Gain Caused by Notch Filter

III. SIMULATION RESULTS

The simulation results of the proposed dual-wideband UWB LNA using Agilent ADS 2005A simulator are given in Figure 9 to Figure 12. In Figure 9 that can be seen that the input/output return loss (S11/S22) are lower than -8.31dB/-11.47dB between 3.1GHz to 4.9GHz, respectively. The power gain whose peak value is 15.65dB at 4.8GHz which covers the Group-A for MB-OFDM and Low-Band for DS-UWB, and is shown in Figure 10. In Fig. 11, it can be seen that the noise figure is below 3.3dB between 3.1GHz to 4.9GHz and the minimum noise figure is 3.30dB at 4.2GHz through 1.8V supply voltage. In Fig. 12, the input-referred 1dB compression point (IP1dB) is -27dBm at 4.0GHz. In Figure 9 that can be seen that the input/output return loss (S11/S22) are lower than -9.50dB/-9.95dB between 6.0GHz to 10.3GHz, respectively. The power gain whose peak value is 11.55dB at 9.0GHz which covers the Group-C and Group-D for MB-OFDM and High-Band for DS-UWB, and the power gain are shown in Figure 10. In Fig. 11, it can be seen that the noise figure is below 6.1dB between 6.0GHz to 10.3GHz and the minimum noise figure is 3.80dB at 6.8GHz through 1.8V supply voltage. In Fig. 12, the input-referred 1dB compression point (IP1dB) is -22dBm at 8.5GHz. The IIP3 performance is not presented in this paper because the UWB system uses a very wide bandwidth and there is no specified fundamental frequency. Therefore, it does not have meaning to discuss carrier interference with its harmonic frequency. The power consumption is 24.07mW through 1.8V supply voltage which neglects the power of output buffer.

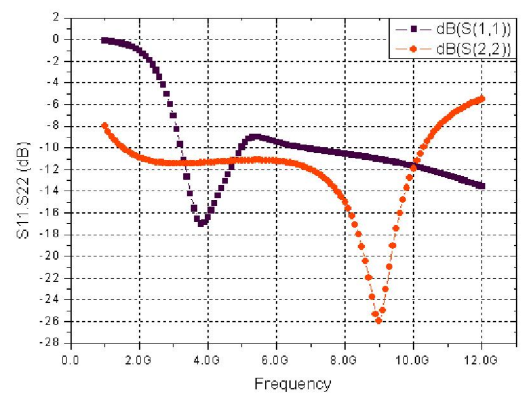

Fig. 9 Input Return Loss (S11) & Output Return Loss (S22)

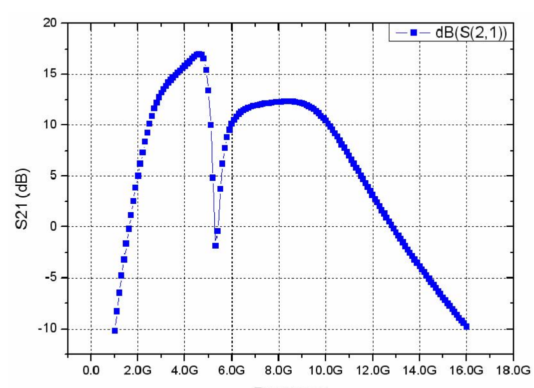

Fig. 10 Power Gain (S21)

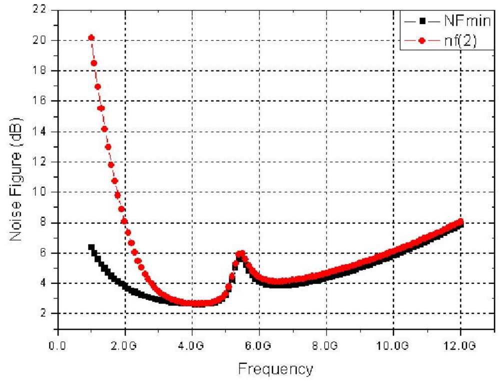

Fig. 11 Noise Figure & Noise Minimum

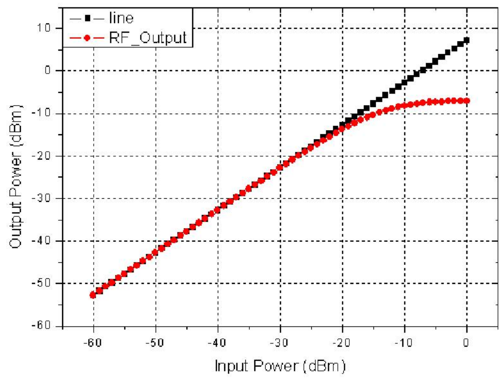

Fig. 12 Input-Referred 1dB Compression Point

	3.1-4.9GHz	6.0-10.3GHz
S11 (dB)	< -8.31	< -9.50
S22 (dB)	< -11.47	< -9.95
S21 (dB)	12.15 ~ 15.65	8.95 ~ 11.55
S21 Max. (dB)	15.65	11.55
Working Bandwidth (GHz)	3.1 ~ 4.9	6.0 ~ 10.3
3dB Bandwidth (GHz)	2.9 ~ 5.1	6.0 ~ 10.5
NF (dB)	2.6 ~ 3.3	3.8 ~ 6.1
IP1dB (dBm)	-27	-22
IIP3 (dBm) [10MHz]	-18	-12
Power Consumption (mW)	24.07	

Table.1 Performance Comparisons

IV. Conclusions

A CMOS UWB LNA is designed with dual-wideband system for 3.1-4.9GHz and 6.0GHz-10.3GHz. The simulation results show that the proposed LNA gives 13.66dB power gain for 3.1-4.9GHz and gives 10.34dB power gain for 6.0-10.3GHz. 2.4GHz 3dB bandwidth (2.9 – 5.1GHz) and 4.5GHz 3dB bandwidth (6.0 – 10.5 GHz) while consuming 24.07mW through 1.8V power supply.

Acknowledgment

The authors would like to thank the chip implementation center (CIC) for technical support.

References

[1] FCC, "Final Rule of the Federal Communications Commission, 47 CFR Part 15,Sec. 503", Federal Register, vol. 67,no. 95,May 2002.

[2] http://www.ieee802.org/15/pub/TG3a.html

[3] Andrea Bevilacqua, and Ali M. Niknejad, " An Ultrawideband CMOS Low-Noise Amplifier for 3.1–10.6-GHz Wireless Receivers",*IEEE JOURNAL OF SOLID-STATE CIRCUITS*, Vol. 39, No. 12,pp.2259-2268,Dec 2004.

[4] Chang-Wan Kim, Min-Suk Kang, Phan Tuan Anh, Hoon-Tae Kim, and Sang-Gug Lee, "An Ultra-Wideband CMOS Low Noise Amplifier for 3–5-GHz UWB System", *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, Vol. 40, No. 2,pp.544-547, Feb. 2005.

[5] Chang, C.-P.; Chuang, H.-R., "0.18 um 3-6 GHz CMOS broadband LNA for UWB radio", *Electronics Letters*, Volume 41, Issue 12, June 2005 Page(s):33 – 34.

[6] Yang-Chaun Chen; Chien-Nan Kuo, "A 6-10-GHz ultra-wideband tunable LNA", *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, 23-26 May 2005 Page(s):5099 - 5102 Vol. 5.

[7] Chih-Fan Liao; Shen-Iuan Liu, "A broadband noise-canceling CMOS LNA for 3.1-10.6-GHz UWB receiver", *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*, 18-21 Sept. 2005 Page(s):161 – 164.

Paper	Circuit Topology	Technology	S11(dB)	S22(dB)	S21(dB)	BW(GHz)	Gmax(dB)	NF(dB)	NFmin(dB)	Pdiss(mW)
[4]	resistive feedback	0.18um CMOS	< -9	< -10	6.8-9.8	2.0-4.6	9.8	2.3-5.2	2.3	12.6
[5]	3-stages comm.-source	0.18um CMOS	<-12.2	< -10.1	13.5-15.8	3.0-6.0	15.76	4.7-6.7	4.7	59.4
[6]	Tunable LC-tank	0.18um CMOS	< -9	< -12	10.0-11.6	6.0-10.0	11.6	4.2-5.3	4.2	11.6
[7]	3-stages shunt-peaked	0.18um CMOS	< -7	< -12	6.7-9.7	1.2-11.9	9.7	4.5-5.1	4.5	20.0
3-4.9GHz (This work)	2-stages shunt-peaked with notch filter	0.18um CMOS	< -8.3	< -11.5	12.2-15.7	2.9-5.1	13.66	2.6-3.3	2.6	24.1
6-10.3GHz			<-9.5	<-9.9	9.0-11.6	6.0-10.5	10.34	3.8-6.1	3	

Table.2 Comparison of the Proposed UWB LNA with Other Reported Wideband LNA