Spatially Resolving the Hot Carrier Degradations of Poly-Si Thin-Film Transistors Using a Novel Test Structure

Horng-Chih Lin, *Senior Member, IEEE*, Ming-Hsien Lee, and Kai-Hsiang Chang

***Abstract*—A novel thin-film transistor test structure is proposed for monitoring the device hot-carrier (HC) degradations. The new test structure consists of several source/drain electrode pairs arranged in the direction perpendicular to the normal (i.e., lateral) channel of the test transistor. This unique feature allows, for the first time, the study of spatial resolution of HC degradations along the channel of the test transistor after stressing. The extent of degradation as well as the major degradation mechanisms along the channel of the test transistor can be clearly identified.**

***Index Terms*—Grain boundary, hot-carrier (HC) effects, poly-Si, test structure, thin-film transistor (TFT).**

I. Introduction

POLY-Si THIN-FILM transistors (TFTs) fabricated on insulating substrates are important for the manufacturing and applications of large-area microelectronics [1]. The device performance degradation caused by hot carrier (HC) effects during normal device operation is one of the major reliability concerns [2], [3]. Hot carriers are generated during normal device operation by the high-electric field existing near the drain junction. Charge trapping in the oxide and creation of interface states would occur, which in turn cause device degradation [4]. As compared with the bulk CMOS counterpart, the situation becomes even more complicated for poly-Si TFTs owing to the lack of substrate contact in typical device configuration, as well as the large amount of potential defect sites existing at the grain boundaries [5]. Since the damage associated with the HC effect is nonuniform along the channel of the stressed transistor after HC stressing, it is desirable to resolve and understand the detailed mechanisms responsible at different portions of the stressed channel. In this letter, a novel test structure that serves this purpose is proposed and demonstrated.

II. Device Structures and Stress Conditions

The top view of the test structure is shown in Fig. 1. The test structure is configured with four pairs of n^+ electrodes at the edge of the channel. One pair of n^+ electrodes is placed along the x (horizontal) direction to form the source and drain (S/D) of the normal (lateral) test transistor that will be subjected to HC stressing, while the other three pairs are arranged along the y (vertical) direction to form three separate monitor transistors (MTs) to allow spatial characterization of the HC degradations along the channel of the test transistor after stressing. A common gate electrode shared by the test transistor as well as all three MTs is lying over the entire channel. Since each pair of n^+ electrodes could be configured as the S/D of the respective MT, the current–voltage $(I$–$V)$ characteristics of the corresponding MT could be characterized.

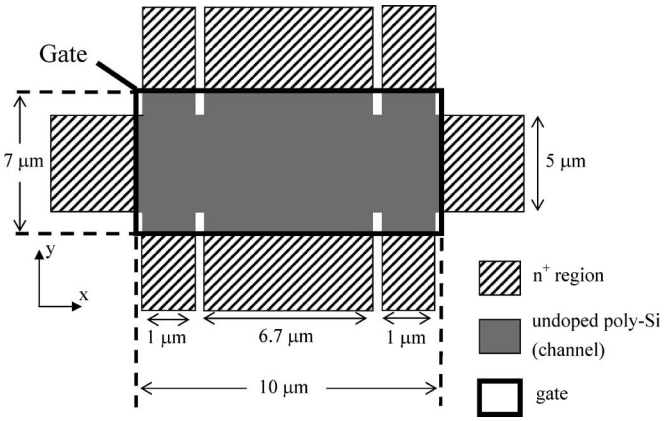

Fig. 1. Top view of the test structure. Structural parameters of the test structure characterized in this letter are detailed in the figure.

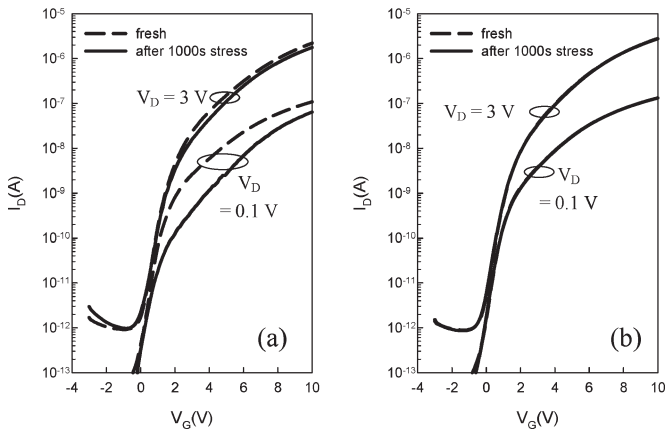

Fig. 2. Subthreshold characteristics of the test transistor before and after the HC stressing at V_D/V_G of (a) 20 V/10 V and (b) 12 V/6 V for 1000 s. Channel length and width are 10 and 5 μm, respectively.

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H.-C. Lin is with the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C., and also with the National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C.

M.-H. Lee and K.-H. Chang are with the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

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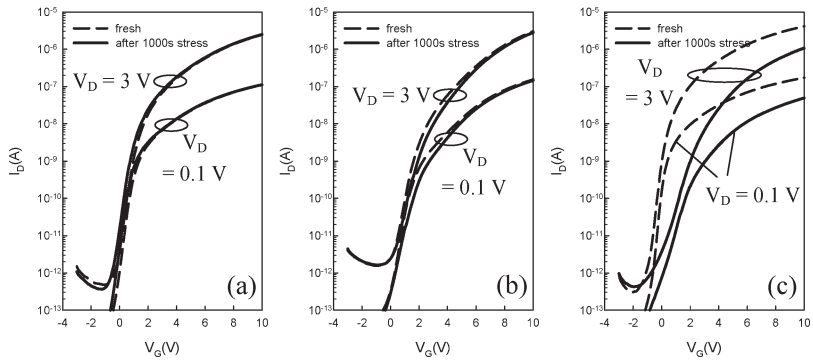

Fig. 3. Subthreshold characteristics of (a) S-MT, (b) C-MT, and (c) D-MT transistors in the same test structure characterized in Fig. 2(a) before and after the HC stressing at V_D/V_G of 20 V/10 V for 1000 s.

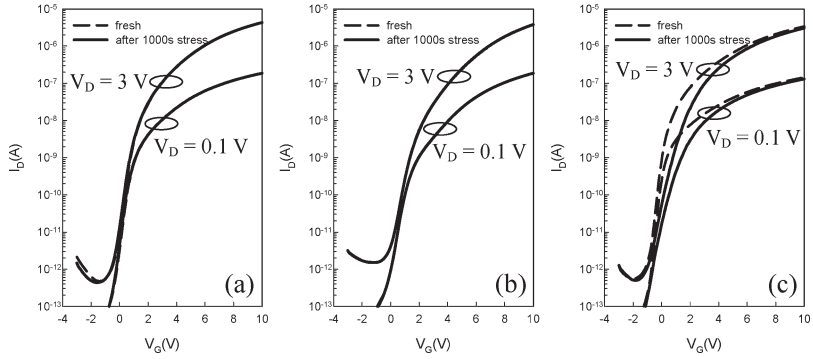

Fig. 4. Subthreshold characteristics of (a) S-MT, (b) C-MT, and (c) D-MT transistors in the same test structure characterized in Fig. 2(b) before and after the HC stressing at a milder V_D/V_G of 12 V/6 V for 1000 s.

The pair of S/D placed along the x-direction that serves to form the test transistor is subjected to HC stressing by applying a high voltage to its drain for inducing the HC degradations in the test transistor. According to their respective location relative to the channel of the test transistor, the three MTs are denoted as the source-side MT (S-MT), central MT (C-MT), and drain-side MT (D-MT), respectively. This unique configuration allows us to resolve the damage and identify the associated mechanisms at different locations along the channel of the test transistor after stressing. Important planar structural dimensions for the test structure characterized in this letter are detailed in Fig. 1.

In this letter, an as-deposited poly-Si layer of 50 nm was employed as the channel, which was deposited by a low-pressure chemical vapor deposition (LPCVD) system at 620 °C. The gate dielectric consisted of a CVD oxide layer of 37 nm. An *in situ* doped poly-Si was employed as the gate electrode. S/D doping was formed by implanting phosphorous ions with a dosage of 5×10^{15} cm^{-3} at 45 keV. After the metallization step, the test structure further received a plasma treatment in NH_3 ambient for 1 h.

III. Results and Discussion

Subthreshold characteristics of the test (i.e., lateral) transistor were measured before and after the stress, and the results are shown and compared in Fig. 2. In Fig. 2(a), the test transistor was stressed under high V_D/V_G of 20 V/10 V for 1000 s to induce HC degradations. As can be seen in the figure, the degradation in device characteristics in terms of increased subthreshold swing and reduced on-current are indeed observed after the stress. The poststress I–V shifts are more significant when measured at a low V_D of 0.1 V after stressing. Moreover, an increase in off-current could be detected at V_D of 3 V and V_G of -3 V. These observations are consistent with a well-known belief that most of the damage events occur in the channel near the drain side of the test transistor. A larger drain bias during the measurements of subthreshold I–V characteristics tends to extend the drain depletion region. This would in turn screen out more defects induced in the channel near the drain side, thus relieving the poststress I–V shift. When the stress voltages are reduced, the degradation is reduced correspondingly. This is shown in Fig. 2(b) where the test transistor was stressed under a milder V_D/V_G of 12 V/6 V for 1000 s. The post-stress I–V curve shows only a negligible shift relative to the fresh device under the milder stress condition.

The aforementioned results from the conventional test transistor provide information regarding the major damage location in the stressed channel and the effect of stress voltages, as is well known in the literature. However, detailed degradation mechanisms at different sections of the stressed channel could not be resolved by the conventional test structure. Besides, the conventional test structure is also insensitive in detecting the induced damage when the applied stress voltages are low. To address these shortcomings, the MTs in the test structure were characterized and the results are shown in Figs. 3 and 4. It is worth noting that the characteristics of the MTs shown in Fig. 3 were measured using the same test structure with its test transistor HC-stressed and measured in Fig. 2(a). It can

be seen that among the three MTs, the D-MT shows the worst degradation. Note that the poststress I–V shift is very significant even measured at a high V_D bias (e.g., 3 V), indicating that the induced traps are uniformly distributed along the entire channel of the D-MT. This observation confirms the inference made above in analyzing the results of Fig. 2(a). However, the remaining two MTs exhibit some interesting results that are not explicitly revealed in Fig. 2(a). First, the C-MT shows degraded subthreshold swing, albeit the on-current does not seem to be affected. This implies that the generation of interface states at the oxide/channel interface is mainly responsible for the degradation. Second, the S-MT shows negative parallel shift in subthreshold characteristics, indicating that positive hole trapping is preponderant in the oxide near the source side of the test transistor after stressing. These holes are generated by the impact ionization during the HC stressing of the test transistor. Since no substrate contact is present in the TFT structure, these holes tend to drift toward the grounded source, and some of them with sufficient energy may surmount the barrier and be injected into the oxide. Based on the results shown in Fig. 3, major degradation mechanisms occurred at different channel sections could be clearly distinguished and identified by the proposed novel test structure.

Fig. 4 shows the subthreshold characteristics of the MTs for the same test structure measured in Fig. 2(b), i.e., after stressing the test transistor at a milder V_D/V_G of 12 V/6 V for 1000 s. It can be seen that both S-MT and C-MT exhibit negligible shift in I–V curves after the stress, similar to the result of the test transistor [Fig. 2(b)]. By contrast, the D-MT shows obvious performance degradation after the stress. This demonstrates the high sensitivity of the test structure in detecting the hot carrier effects.

By increasing the number of MTs, it will be possible to increase the spatial resolution along the channel in detecting the HC induced degradation. In this way, it will be possible to detect experimentally the uniformity of degradation near the drain region, instead of simply using numerical analysis of specific models to predict the poststress performance of the device [6], [7]. Nevertheless, this methodology is limited when the device dimensions become small, since the current level of the monitor current is decreased. Further work is needed to verify the limitation.

IV. Conclusion

In this letter, we have proposed and successfully demonstrated a new test structure suitable for monitoring the spatial HC degradation in poly-Si TFTs not previously possible. Our results indicate that the new structure is capable of resolving the spatial damage induced at different sections of the stressed channel and, based on the observations, major mechanisms responsible for the resultant degradation could be identified. The new test structure is also shown to be highly sensitive for detecting degradations in even slightly damaged devices.

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References

[1] A. G. Lewis, I.-W. Wu, T. Y. Huang, A. Chiang, and R. H. Bruce, "Active matrix liquid crystal display design using low and high temperature processed polysilicon TFTs," in *IEDM Tech. Dig.*, 1990, pp. 843–846.

[2] Y. Uraoka, T. Hatayama, T. Fuyuki, T. Kawamura, and Y. Tsuchihashi, "Reliability of low temperature Poly-Silicon TFTs under inverter operation," *IEEE Trans. Electron Devices*, vol. 48, no. 10, pp. 2370–2374, Oct. 2001.

[3] I. W. Wu, W. B. Jackson, T. Y. Huang, A. G. Lewis, and A. Chiang, "Mechanism of device degradation in n-channel and p-channel polysilicon TFTs by electrical stressing," *IEEE Electron Device Lett.*, vol. 11, no. 4, pp. 167–169, Apr. 1990.

[4] B. Doyle, M. Bourcerie, J.-C. Marchetaux, and A. Boudou, "Interface state creation and charging trapping in the medium to high gate voltage range during hot-carrier stressing of n-MOS transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 744–754, Mar. 1990.

[5] N. D. Young, "The formation and annealing of hot-carrier-induced degradation in Poly-Si TFT's, MOSFET's, and SOI devices, and similarities to State-creation in αSi:H," *IEEE Trans. Electron Devices*, vol. 43, no. 3, pp. 450–456, Mar. 1996.

[6] L. Mariucci, G. Fortunato, R. Carluccio, A. Pecora, S. Giovannini, F. Massussi, L. Colalongo, and M. Valdinoci, "Determination of hot-carrier induced interface state density in polycrystalline silicon thin-film transistors," *J. Appl. Phys.*, vol. 84, no. 4, pp. 2341–2438, Aug. 1998.

[7] A. T. Hatzopoulos, D. H. Tassis, N. A. Hastas, C. A. Dimitriadis, and G. Kamarinos, "An analytical hot-carrier induced degradation model in polysilicon TFTs," *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2182–2187, Oct. 2005.