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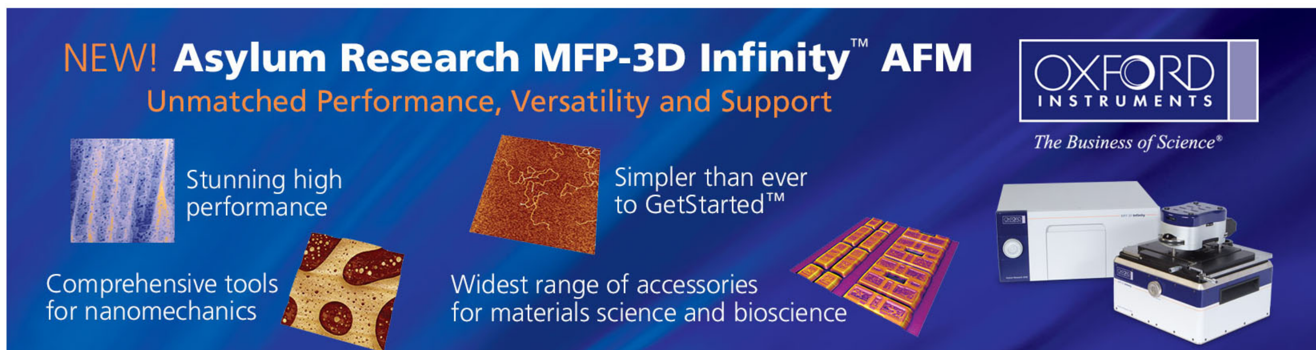

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APPLIED PHYSICS LETTERS **88**, 262909 (2006)

Study on the interface thermal stability of metal-oxide-semiconductor structures by inelastic electron tunneling spectroscopy

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The bias polarity-dependent inelastic electron tunneling spectroscopy is employed to detect the thermal stability of the Ta–Pt/SiO_2/Si and Ta–Pt/HfO_2/Si structures. This work provides a direct evidence that the Fermi-level pinning of metal gates is counted for the generation of extrinsic states due to interface interaction. A Ta_2O_5 layer forms at the Ta–Pt/SiO_2 interface during thermal annealing whereas only an intermittent Ta–O bond is observed at the Ta–Pt/HfO_2 interface. Although the heat of formation of HfO_2 is lower than that of SiO_2, Si presumably diffuses into HfO_2 layer and replaces Hf atoms during the high-temperature annealing. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2219140]

Metal gates are expected to replace polysilicon gates and to integrate with high dielectric constant materials beyond 45 nm technology node.[1] Several kinds of metal gates such as pure metals, binary alloys, metal nitrides, and metal silicides have been proposed.[2–8] One of the most important issues with those gates is that the effective work function ($\phi_{m,\mathrm{eff}}$) is thermally unstable. It is suspected that the thermal instability of $\phi_{m,\mathrm{eff}}$ is caused by the interface reaction between metal electrode and gate dielectric.[4–8] However, no direct evidence has been reported because interface analysis is more difficult than surface analysis. The typical analysis techniques such as Fourier transform infrared spectroscopy, x-ray photoelectron spectroscopy, secondary ion mass spectroscopy, and electron spin resonance spectroscopy may not be suitable for interface analysis on a real device structure.

Recently, a promising interface analysis technique called inelastic tunneling spectroscopy (IETS) was employed to analyze the chemical bonds at the electrode and dielectric interface by detecting the interaction between tunneling electrons and phonons.[9–11] The IETS can further detect the interface bonding near the upper interface or lower interface of a metal-insulator-semiconductor (MIS) or metal-insulator-metal structure by using the bias polarity-dependent characteristic.[11] In this work, the polarity-dependent IETS technique is used to probe the thermal stability of Ta–Pt alloy/SiO_2/Si and Ta–Pt alloy/HfO_2/Si MIS structures.

The MIS capacitors were fabricated on (100)-oriented, *p*-type silicon wafers with a resistivity of lower than 0.001 Ω cm. The metal electrode area was 0.024 cm^2. The capacitors have a shape of two concentric rings isolated by a thick thermally grown field oxide (FOX) in order to keep a uniform electric field as shown in Fig. 1. After field oxide patterning, wafers were cleaned by the standard cleaning process followed by dipping in HF solution for 10 s. For the SiO_2 samples, a 1.5 nm thick SiO_2 layer was thermally grown in a mixture of N_2 and O_2 at 700 °C for 1 min followed by annealing in N_2 ambient at 900 °C for 10 min in the same furnace. For the HfO_2 samples, a 3 nm thick HfO_2 layer was deposited at 300 °C using $HfCl_4$ as precursor and H_2O vapor as oxidant in an atomic layer deposition system. No HfO_2 postdeposition annealing was followed immediately. Metal gates were patterned by lift-off process. The Ta–Pt alloy was deposited in a cosputtering system to a thickness of 55 nm, and the sputtering powers of Ta and Pt targets were set to dc 30 W and rf 30 W, respectively. After the lift-off process, post-metal-annealing was performed at 500 or 800 °C in N_2 ambience for 30 s in the rapid thermal annealing system. This was followed by substrate contact opening using conventional lithography and wet etching processes. Finally, a 500 nm thick aluminum (Al) layer was deposited as local interconnects and probing pads by thermal evaporation. The IETS measurement was performed by a modulation technique using a lock-in amplifier. The details of the system setup can be found elsewhere.[12] Measurement was performed at 15 K and the ac modulation is 2 mV with a frequency of 5 KHz. The dc resolution is 2 mV.

The IETS spectra of 500 and 800 °C annealed Ta–Pt/SiO_2/Si samples are shown in Fig. 2. The asymmet-

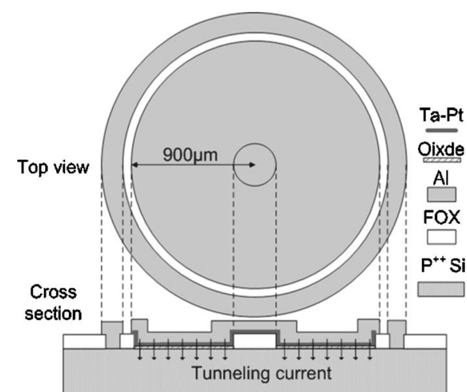

FIG. 1. The schematic top view and cross section of the test structure.

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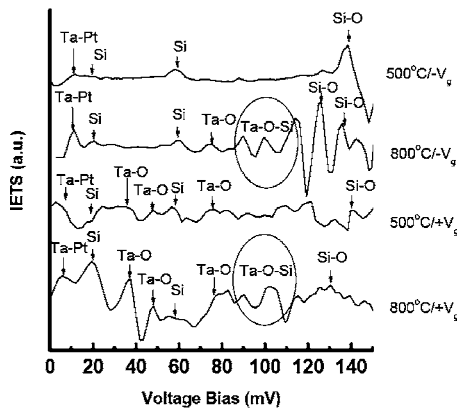

FIG. 2. The inelastic electron tunneling spectra of Ta–Pt/SiO_2/degenerated Si samples annealed at 500 and 800 °C.

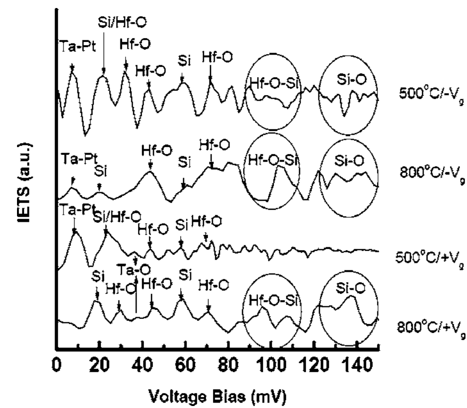

FIG. 4. The inelastic electron tunneling spectra of Ta–Pt/HfO_2/degenerated Si samples annealed at 500 and 800 °C.

ric IETS was caused by different bias polarities. The negative gate bias qualitatively reflects the interaction between electrons and phonons near the bottom interface.[11] The signals of Si substrate and SiO_2 phonon modes have been well identified and analyzed by previous researchers.[11,13] The signals of Si phonons were at 20 and 59 mV and the signals of SiO_2 phonons ranged broadly from 130 to 170 mV.[9,11,14] Several additional peaks occurred on the 800 °C annealed sample (800 °C/$-V_g$ in Fig. 2). The peak at 77 mV (equal to 640 cm^{-1}) was attributed to amorphous Ta_2O_5.[15,16] The observation proved the reaction between Ta of Ta–Pt alloy and SiO_2. The obvious and intense peaks between 90 and 120 mV were qualitatively attributed to deteriorated SiO_2 instead of Ta_2O_5 since the main peak of Ta–O was located only at 77 mV. Those peaks between Ta–O modes and Si–O modes represent Ta–O–Si (metal–O–Si) bonds or imperfect SiO_2 (SiO_x) due to the chemical reaction between Ta–Pt gate and SiO_2.[17,18] The spectra at positive gate bias were more sensitive to the phonon interaction near the Ta–Pt alloy gate. In addition to the Ta–O peak at 77 mV, the other Ta–O peaks at 38 and 49 mV were also observed.[11,12] Both the 500 and 800 °C samples revealed Ta–O bond and the higher and sharper peaks of the 800 °C annealed sample indicated the growth of tantalum oxide.

To investigate the electrical effects of chemical reaction at the interface between Ta–Pt and SiO_2, the work function of Ta–Pt gate was analyzed. In Fig. 3, the barrier height of Ta–Pt electrode extracted by the Fowler-Nordheim tunneling plot increases from 3.18 to 3.65 eV as the annealing temperature increases from 500 to 800 °C. The inset shows that

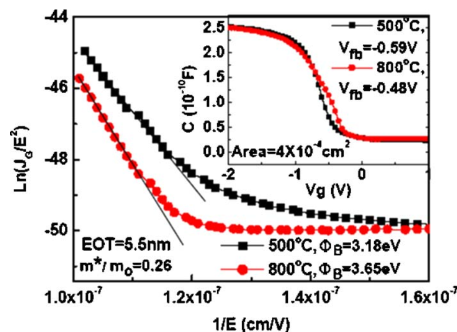

FIG. 3. Fowler-Nordheim plot of the Ta–Pt/SiO_2 (5.5 nm)/Si structure after annealing at 500 and 800 C for 30 °C. The m^*/m_o=0.26 is used to calculate the barrier height (Φ_B) (Ref. 24). The inset shows the relative *C-V* curves.

the equivalent oxide thickness is almost unchanged after 800 °C annealing while the flatband voltage (V_{fb}) changes from the −0.69 to −0.48 V. These observations imply that the effective work function is increased after 800 °C annealing and is consistent with the published data that low work function (near the silicon conduction band) of metal gate tends to the midgap of silicon energy band after high-temperature annealing.[7] It is believed that the Fermi-level pinning (work function offset) originates from the chemical reaction between metal gate and SiO_2 gate dielectric.

Figure 4 shows the IETS spectra of the Ta–Pt/HfO_2/Si samples annealed at 500 and 800 °C. Both the negative and positive biased IETS spectra were measured. The peaks were identified based on the literature values.[12,17,18] The peaks of Si–O and Hf–O–Si vibration modes of the 500 °C annealed sample were weaker than those of the 800 °C annealed sample, and those of the negative-gate-bias IETS spectra were stronger than those of the positive ones. These observations imply the growth of silicon oxide at the lower interface during high-temperature annealing, which has been clearly detected by the transmission electron microscope (TEM) inspection. The shift of the main peak of Hf–O vibration modes after high-temperature annealing was reasonably caused by the crystallization, where the main peak of the 500 °C annealed sample was located at 32 mV and was lower than the main peak of the 800 °C annealed sample located at 43 mV.[18] A special peak of the Hf–O vibration mode at 71 mV observed on both the 500 and 800 °C annealed samples was attributed to the hafnium silicate but not to pure HfO_2.[17,19] This implied that the interfacial layer contained the mixture of Hf–O and O–Si bonds, i.e., Hf silicate. Another special peak at 38 mV was suspected to the Ta–O vibration mode and was only observed on the positive-gate-bias IETS spectra.[20] The peak was small and did not grow even after high-temperature annealing. The Ta–Pt/HfO_2 interface was further inspected by high resolution transmission electron microscopy. An intermittent monolayer material was observed at the interface which corresponded to the weak IETS peaks of both 500 and 800 °C samples. The monolayer Ta–O bond might be formed during the Ta–Pt alloy deposition.

The reaction at the upper interface of HfO_2 is self-limited while the reaction at the lower interface of HfO_2 is continuous during the high-temperature annealing. The reactant, oxygen, surely does not come from the annealing ambient since the Ta–Pt alloy is not oxidized at the upper inter-

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face. Those mean that the oxygen should come from the HfO_2 layer. The existence of Hf silicate sensibly implies that the oxygen comes from the broken Hf–O bond. However, the postulation that HfO_2 releases oxygen atoms during high-temperature annealing while the oxygen only reacts with Si but not Ta is unreasonable since the heat of formations of HfO_2, Ta_2O_5, and SiO_2 are −271, −230, and −210 Kcal/mol, respectively. Besides, the Hf–O, Ta–O, and Si–O bonds are more stable than the Si–Si bond since the bonding energies of Hf–O, Ta–O, Si–O, and Si–Si are 801.7, 799.1, 799.6, and 326.8 KJ/mol, respectively.[21] Therefore, it is presumed that the oxygen is not thermally decomposed from the HfO_2, but it is more reasonable that the Si atom diffuses into the HfO_2 layer from the Si substrate and directly replaces the Hf atom.[21–23] On the other hand, it is difficult for Ta atom to diffuse into the HfO_2 layer, and HfO_2 is more stable than Ta_2O_5 so that only an intermittent Ta–O bond forms at the Ta−Pt/HfO_2 interface. While the Ta–Pt alloy is deposited on the SiO_2, the lower heat of formation of Ta_2O_5 than that of SiO_2 results in a more stable Ta_2O_5.

In summary, IETS spectroscopy provides a direct inspection of thermal instability at the interface of the MIS structure. The analysis of results provides a direct evidence that the Fermi-level pinning of Ta–Pt metal gates on SiO_2 is counted for the generation of extrinsic states due to the formation of the tantalum oxide. The Ta−Pt/HfO_2 interface is more thermally stable than the HfO_2/Si interface. Hf silicate formation during thermal annealing is detected at the latter interface by our IETS analysis.

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