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A novel design of high-speed divide-by-3/4 counter for a dual-modulus prescaler

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Abstract: A novel design for a high-speed divide-by-3/4 counter is presented. The proposed design reduces not only the critical path delay but also the feedback path delay, hence it can increase the operating speed. With this divide-by-3/4 counter, a divide-by-127/128 dual-modulus prescaler (DMP), implemented in 0.18 μm CMOS technology, shows a maximum operating frequency of 7.0 GHz with 2.4 mW power consumption at 1.8 V supply voltage, which has 25% speed improvement and still consumes less power as well compared to the recently-reported one.

Keywords: prescaler, high-speed circuits, synchronous counter
Classification: Integrated circuits

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1 Introduction

A high-moduli DMP presents a crucial challenge to the design of low-power, high-speed, and high performance CMOS PLL-based frequency Synthesizers, which are widely used in modern communication systems. Most high-moduli DMPs usually comprise of a conventional synchronous divide-by-4/5 counter,

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followed by a chain of toggle flip-flops, which forms an asynchronous counter. The operating speed of DMPs is mainly limited by that of the divide-by-4/5 counter. Unlike the conventional divide-by-4/5 counter [1], a new topology for a divide-by-3/4 counter using transmission gates (TGs) in the critical path for mode selection is proposed by R. S. Rana [2]. The author has demonstrated that the TG-based divide-by-3/4 counter provides higher speed compared to the conventional divide-by-4/5 counter. However, an alternative divide-by-3/4 counter using NOR gates in the critical path is also presented and taken into account for further comparison by R. S. Rana [2]. With the help of Hspice simulation, the results show that the NOR-based divide-by-3/4 counter provides higher speed than the TG-based one due to smaller feedback path delay even though the critical path delay is more. For enhancing the speed of the TG-based divide-by-3/4 counter further, the author expects to shorten the D flip-flop (DFF) delay for future improvement.

In this paper, a novel design for a high-speed divide-by-3/4 counter is presented. The design is different from the above-mentioned design by adopting a ratioed-NAND structure in the counter. Based on this design, not only the critical path delay but also the feedback path delay can be reduced due to the mergence of the logic gates used for mode selection into the flip-flop. Thus, our design leads to a higher speed.

2 Circuit Descriptions

Fig. 1 (a) and (b) show the circuit schematics of the TG-based and NOR-based divide-by-3/4 counters, respectively. It can be seen that the speed of divide-by-3/4 counter is limited primarily by two factors: 1) DFF delay and 2) logic gate delay in the critical and feedback paths. Consequently, it is believed that the speed of DMP can be further improved if the logic gate delay and/or DFF delay can be reduced. Fig. 1 (c) shows the circuit topology of a divide-by-3/4 counter using the proposed design. From the figure, the proposed topology uses a 2-to-1 multiplexer in the critical path for mode selection and adopts a ratioed-NAND structure in the counter. The principle of circuit operation can be illustrated as follows.

For the divide-by-4 case: Q1Q2 cycles as 00 to 10 to 11 to 01 to 00 and so on. For the divide-by-3 case: the state "01" is skipped and changes directly from 11 to 00. Here, this can be achieved by generating the signal S from MC using 2-to-1 multiplexer. In turn, NAND-FF2 functions as "Q1 AND S". When TG0 is on (TG1 is off), DFF1 and NAND-FF2 function as divide-by-4 counter else as divide-by-3 one.

When the signal $MC = 1$, TG0 is turned off and TG1 is on. In other words, the path from QB2 to S is disconnected and S is connected to VDD. Thus, NAND-FF2 functions as "Q1 AND 1" and the circuit operates in divide-by-4 mode. Whereas, when the signal $MC = 0$, TG1 is off and TG0 is on. In turn, the path from QB2 to S gets connected. Therefore, NAND-FF2 functions as "Q1 AND QB2" which results in the divide-by-3 mode operation.

It is worth noting here that, in a divide-by-127/128 DMP which consists

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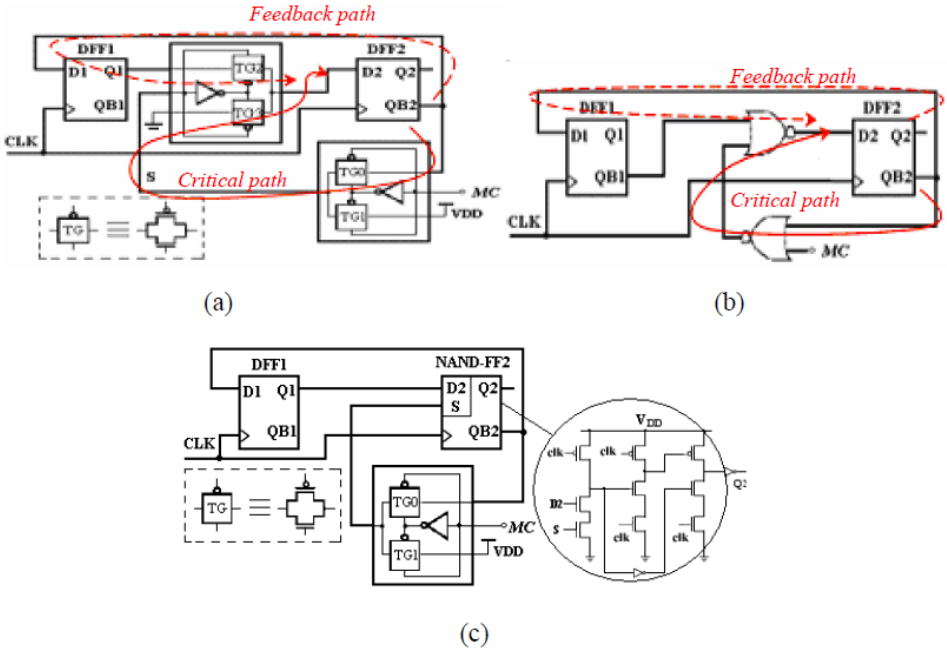

Fig. 1. Circuit schematics (a) TG-based divide-by-3/4 counter (b) NOR-based divide-by-3/4 counter (c) Proposed divide-by-3/4 counter

of a synchronous divide-by-3/4 counter and an asynchronous divide-by-32 counter, the synchronous counter in divide-by-127 mode divides by 3 by connecting QB2 and S through TG0. Thus, the critical path is the path from QB2 to S. Unlike conventional DMPs, rather than using static CMOS logic gates, the critical path delay due to TGs can be lower. For $MC = 0$, when QB2 becomes "0," S must follow QB2 before the next rising edge of the clock resulting in the correct function. This is why the delay from QB2 to S is important.

The proposed topology shows a smaller critical path delay than the TG-based and NOR-based ones. Moreover, the feedback path delay is also reduced based on the optimization method of merging flip-flop with the logic between flip-flops, which has been developed recently [3, 4].

3 Simulation Results

To evaluate the proposed divide-by-3/4 counter, a high-speed divide-by-127/128 dual-modulus prescaler using our design, implemented in TSMC 0.18 μm CMOS technology, is presented with the help of HSPICE simulation. The high-speed True Single Phase Clocking (TSPC) ratioed DFF [3] is used in the synchronous counter. As the asynchronous counter operates at about one-fourth frequency compared to the synchronous counter, the True Single Phase Clocking (TSPC) DFFs [5] are used for low-power consideration. Fig. 2 (a) shows the simulated waveforms of the divide-by-127/128 outputs at 5 GHz. This validates the fact that during the divide-by-127 operation, the state "Q1Q2=01" is skipped and the transition in output occurs early by one clock cycle.

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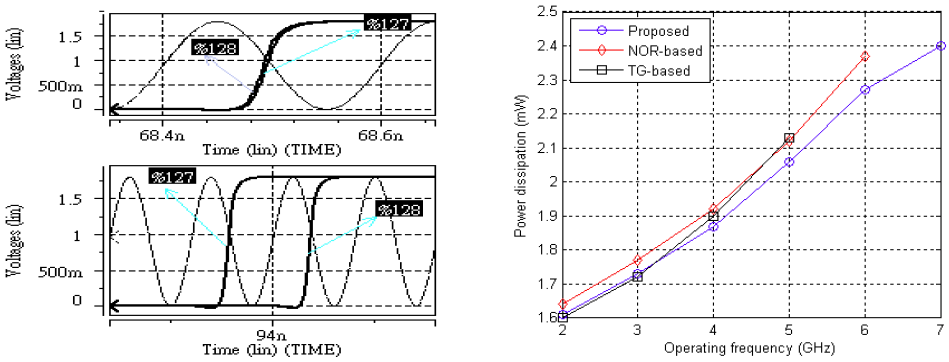

(a) (b)

Fig. 2. (a) Waveforms of the divide-by-127/128 outputs at 5 GHz (b) Power dissipation versus operating frequency at 1.8 V

Table I. Comparison between Rana's and proposed 127/128 DMP

Parameter	NOR-based DMP	TG-based DMP	Proposed DMP
Critical path delay element	2 NOR gates	2 TGs	Only 1 TG
Feedback path delay element	DFF1(QB2 to QB1), 1 NOR gate	DFF1(QB2 to Q1), 1 TG	Only DFF1 (QB2 to Q1)
Critical path delay	99ps	93ps	26ps
f_{max}	6.1 GHz	5.6 GHz	7.0 GHz
Power@f_{max}	2.38 mW	2.2 mW	2.4 mW
Supply voltage	1.8 V	1.8 V	1.8 V
Technology	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS

For comparing the performance comparison, two different divide-by-127/128 DMPs using the NOR-based divide-by-3/4 counter and TG-based one may also be realized using the same DFF and asynchronous counter as mentioned above. Table I provides a summary of the performance comparisons. It indicates that the critical path delay as well as the feedback path delay is further reduced for the proposed divide-by-3/4 counter. This leads to a higher speed. Thus, a maximum operating frequency of 7.0 GHz is obtained at 1.8 V supply voltage with a power consumption of only 2.4 mW for the proposed DMP, which is about 15% and 25% speed improvement over the DMPs using NOR gates and TGs in the critical path, respectively. Fig. 2 (b) shows the comparison of power consumption at different operating frequencies and indicates another benefit of low power consumption.

4 Conclusions

This paper presented a novel and robust design for a high-speed divide-by-3/4 counter. The proposed design is suitable for the high-moduli DMP at high-speed and low-power operation. The use of ratioed-NAND structure helps enhance the speed of the DMP as a result of smaller feedback path delay and critical path delay. The simulation results demonstrate that the high-moduli DMP using the proposed design not only has excellent speed

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improvement but also consumes lower power than that proposed by Rana [2] at a given operating frequency.

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