A CMOS Low Noise Amplifier with RLC-Impedance Feedback for 3-5GHz Ultra-Wideband Wireless System

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Abstract — **In this paper a CMOS low-noise amplifier (LNA) is designed for ultra-wideband (UWB) wireless receiver radio system. The design consists of a wideband input impedance matching network, a cascoded amplifier with shunt-peaked load, a RLC-impedance feedback loop and an output buffer for measurement purpose. It is simulated in TSMC 0.18um standard RF CMOS process. The LNA gives 13.65dB maximum power gain between 3.1GHz-5.0GHz while consuming 12.51mW through a 1.8V supply voltage. Over the 3.1GHz-5.0GHz frequency band, the minimum noise figure (NF) is 3.67dB. Input return loss lower than -10.1 dB in all bandwidth have been achieved.**

Index Terms — **RFIC, Ultra-Wideband, UWB, Feedback, LNA, Low-Noise Amplifier.**

I. INTRODUCTION

Since the approval of the ultra-wideband (UWB) radio technology for low power wireless communication application in February, 2002, [1] UWB systems has become an increasingly popular technology which is capable of transmitting data over a wide spectrum of frequency with very low power and high data rate. Although the IEEE UWB standard (IEEE 802.15.3a [2]) has not been completely defined, two major proposed solutions, MB-OFDM and DS-UWB, are all allowed to transmit in a band between 3.1GHz-4.9GHz and 3.1GHz-4.7GHz. The 1st generation device in commercial applications for ultra-wideband radio systems which are shown in Fig.1(a) and Fig.1(b). The band definition of MB-OFDM is illustrated in Fig.1 (a) which extended from 3168MHz to 4752MHz and the band definition of DS-UWB are from 3100MHz to 4900MHz. The bandwidth of DS-UWB is in Fig.1 (b). The U-NII band located in 5.0GHz-6.0GHz and most popular specification in this band is WLAN (IEEE 802.11a).

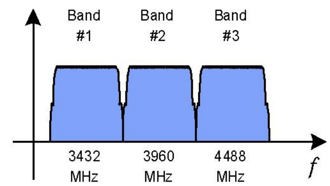

Fig.1 (a) Group A of MB-OFDM

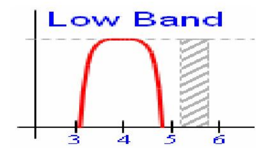

Fig.1 (b) Low Band of DS-UWB

This paper is focused on the design and implementation of low noise amplifier for MB-OFDM and DS-UWB radio systems. It is implemented in a 0.18um Standard RF CMOS Process.

II. DESIGN OF LOW-NOISE AMPLIFIER

The proposed low-noise amplifier is shown in Fig.2 which consists of wideband input impedance matching networks, a cascode amplifier with shunt-peaked load, a RLC-impedance feedback path and an output buffer. The constituents of wideband matching networks are inductors L_1, R_F, L_F, C_F and L_s, capacitor C_1 and transistor M_1. First stage cascoded amplifier are transistors M_1 and M_2 with shunt-peaked load consists of inductor L_{load1}, resistor R_{load1}, and the RLC-impedance feedback path including R_F, L_F and C_F. A common-drain amplifier M_3 is a good choice of wideband output impedance matching for measurement purpose.

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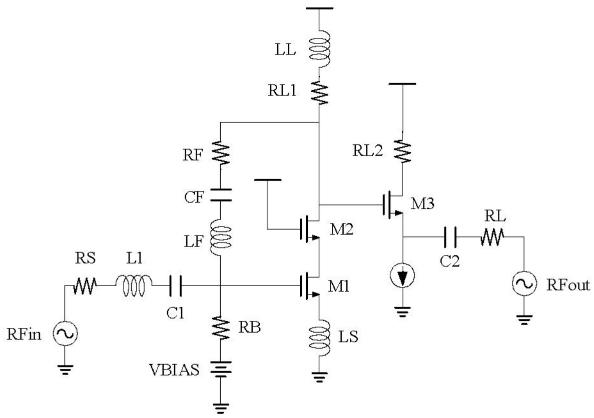


Fig.2 Proposed Low-Noise Amplifier for UWB System

The equivalent impedance Z_L and Y_F are stated in equation (1) and (2). According to the Miller's Theory, the impedance Z_F of the feedback loop could be separated into input impedance Z_1 and output impedance Z_2 which is shown in Fig. 3. The wideband input impedance matching networks including L_1, C_1 and Z_1 which determined two center frequencies in input return loss that is shown in Fig. 4. Furthermore, the loads of the cascoded amplifier, Z_L and Z_2, also determined two resonant frequencies in power gain. The frequency response of the amplifier is composed of two main power gain (blue lines) which are shown in Fig.5, and finally combined into a wide bandwidth power gain (red line).

$$Z_L = R_{L1} + sL_L \tag{1}$$

$$Y_F = \frac{1}{R_F + sL_F + \dfrac{1}{sC_F}} \tag{2}$$

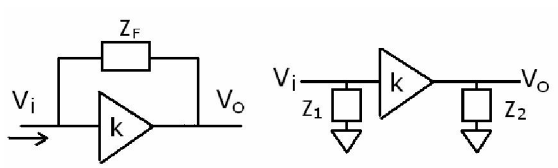


Fig.3 Miller's Theory

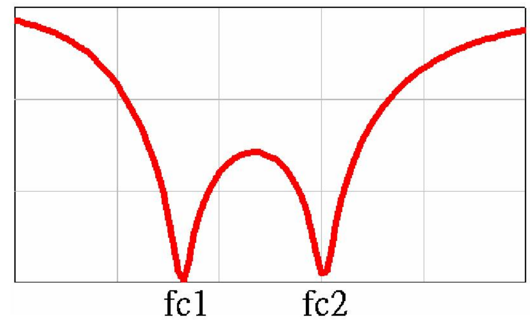
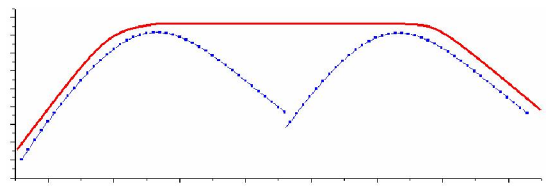


Fig.4 Wideband Input Impedance Matching

Fig.5 Gain Compensated



III. Post-Layout Simulation Results

The post-layout simulation results of the proposed UWB LNA using Agilent ADS 2005A simulator are given in Figure 6 to Figure 10. In Figure 6 and Figure 7, the input/output return losses (S11/S22) are lower than -10.10dB/-9.76dB between 3.1GHz to 5.0GHz, respectively. The power gain whose peak value is 13.65dB at 4.0GHz is shown in Figure 8. It covers the Group-A of MB-OFDM and Low-Band for DS-UWB. In Fig. 9, it can be seen that the noise figure is below 4.05dB between 3.1GHz to 5.0GHz and the minimum noise figure is 3.67dB at 3.7GHz. The power consumption is 12.51mW through a 1.8V power supply. In Fig. 10, the input-referred 1dB compression point (IP1dB) is -19dBm at 4.5GHz and the IIP3 is -5dBm with 3960MHz and 3970MHz which is in Fig. 11.

VI. Conclusion

A CMOS UWB LNA is designed for dual-mode, MB-OFDM and DS-UWB, radio systems. The post-layout simulation results show that the proposed LNA gives 13.65dB maximum power gain between 3.1GHz to 5.0GHz while consuming 12.51mW though a 1.8V power supply.

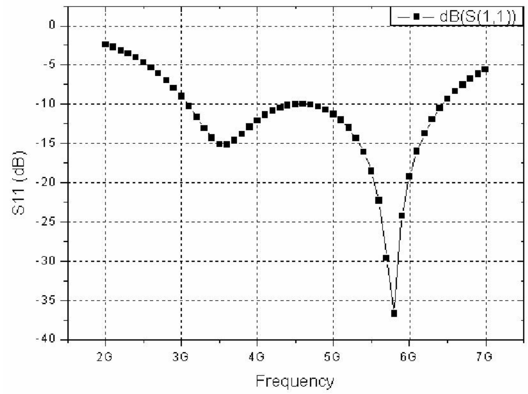


Fig.6 Input Return Loss

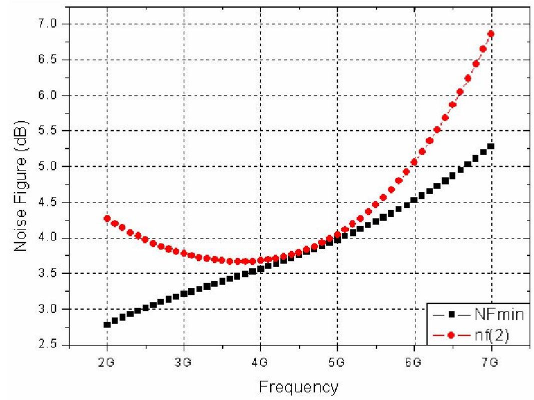


Fig.9 Noise Figure

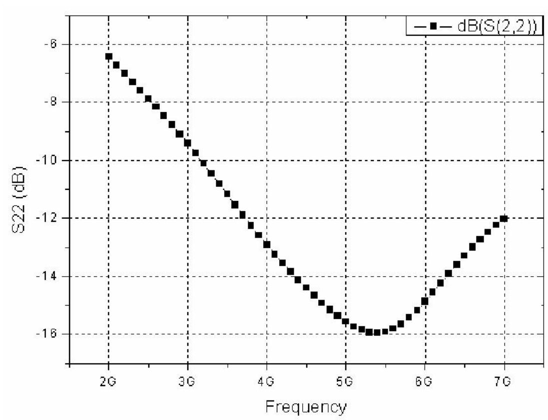


Fig.7 Output Return Loss

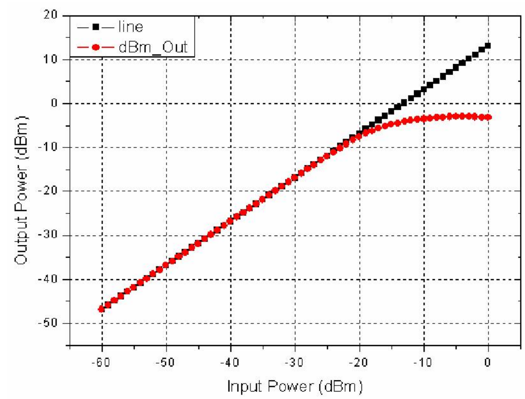


Fig.10 Input Power Compression 1dB

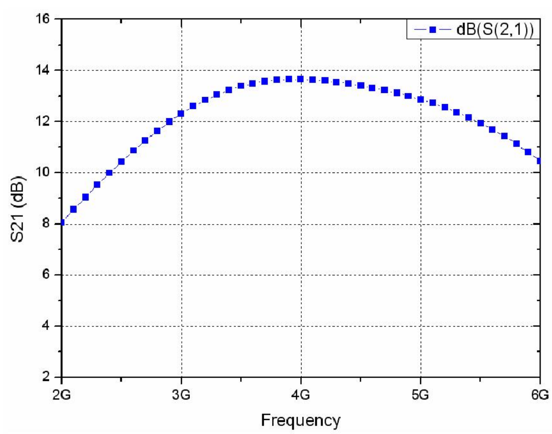


Fig.8 Power Gain

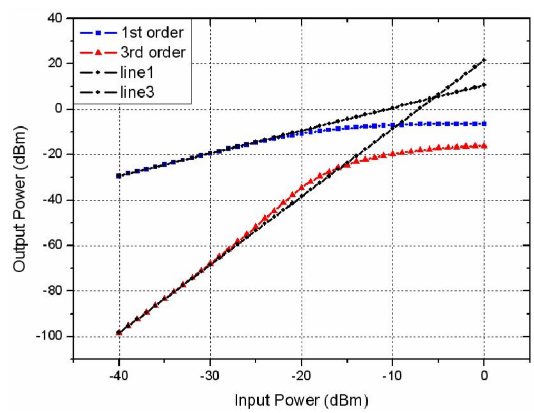


Fig.11 IIP3

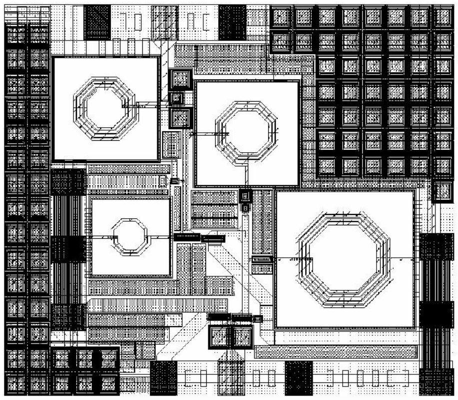


Fig.11 Layout of the Purposed UWB LNA

	3.1-5.0GHz
S11 (dB)	< -10.10
S22 (dB)	< -9.76
S21 (dB)	12.60 ~ 13.65
S21 Max. (dB)	13.65
Working Bandwidth(GHz)	3.1 ~ 5.0
3dB Bandwidth (GHz)	2.5 ~ 6.0
NF (dB)	3.67 ~ 4.05
P1dB (dBm)	-19
IIP3 (dBm)	-5
Power Consumption (mW)	12.51

Table.1 Performance Conclusions

ACKNOWLEDGEMENT

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Paper	Circuit Topology	Technology	S11(dB)	S22(dB)	S21(dB)	BW(GHz)	Gmax(dB)	NF(dB)	NFmin(dB)	Pdiss(mW)
[4]	resistive feedback	0.18um CMOS	< -9	< -10	6.8-9.8	2.0-4.6	9.8	2.3-5.2	2.3	12.6
[5]	3-stages comm.-source	0.18um CMOS	<-12.2	< -10.1	13.5-15.8	3.0-6.0	15.7	4.7-6.7	4.7	59.4
[6]	2-stage shunt-peaked	0.18um CMOS	< -9.5	< -8.1	15.3-18.0	3.1-5.0	18.03	2.7-3.1	2.7	25.9
This work	2-stages shunt-peaked	0.18um CMOS	< -8.7	< -9.3	11.2-13.1	2.8-6.3	13.1	3.7-5.0	3.7	12.5

Table.2 Performance Comparisons