Characteristics and Physical Mechanisms of Positive Bias and Temperature Stress-Induced Drain Current Degradation in HfSiON nMOSFETs

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***Abstract*—Drain current degradation in HfSiON gate dielectric nMOSFETs by positive gate bias and temperature stress is investigated by using a fast transient measurement technique. The degradation exhibits two stages, featuring a different degradation rate and stress temperature dependence. The first-stage degradation is attributed to the charging of preexisting high-k dielectric traps and has a $\log(t)$ dependence on stress time, whereas the second-stage degradation is mainly caused by new high-k trap creation. The high-k trap growth rate is characterized by two techniques, namely 1) a recovery transient technique and 2) a charge-pumping technique. Finally, the effect of processing on high-k trap growth is evaluated.**

***Index Terms*—HfSiON, positive bias temperature instability (PBTI), transient measurement, trap generation, two-stage degradation.**

I. Introduction

HIGH-DIELECTRIC-CONSTANT (high-k) materials have emerged as a replacement for SiO_2 as gate dielectric in CMOS devices [1] to boost device drivability (due to a smaller effective oxide thickness) or to alleviate gate leakage current while keeping comparable device performance. Among various high-k gate dielectrics, Hf-based silicates (e.g., HfSiON) are considered to be the most promising and have been successfully integrated into CMOS devices for low-power applications with good reliability, comparable mobility to SiO_2, and greatly reduced gate leakage current [2].

The reliability issues concerning high-k gate dielectrics include stress-induced leakage current (SILC) [3], dielectric breakdown (BD) [4]–[8], and bias temperature stress-induced threshold voltage instability (BTI) [9]–[13]. Crupi *et al.* concluded that SILC imposes no reliability constraint at room temperature in high-k devices [3]. Degraeve *et al.* indicated that high-k dielectric traps at shallow and deep energies are respectively responsible for V_t hysteresis and SILC and that low stress gate voltage induces no degradation in high-k dielectrics due to energy loss in trap-assisted conduction [4]. They also claimed that charge-to-breakdown $(Q_{\rm BD})$ in high-k gate dielectrics is extrapolated to be virtually infinite at low stress voltages. Moreover, a thermochemical model with leakage current acceleration was proposed for high-k dielectric BD in [8].

Unlike SiO_2 CMOS where negative bias temperature instability (NBTI) in pMOSFETs is considered to be a dominant reliability constraint [14], positive bias temperature instability (PBTI) in high-k nMOSFETs actually dictates device lifetime [15]. PBTI in HfSiON nMOSFETs arises from trap charging and creation in the high-k layer [9]–[13]. Various PBTI models have been proposed to explain the evolution of the V_t shift, although the measured results in literature are not consistent. For example, Zafar *et al.* found that PBTI-induced V_t shift increases with a stretched exponential dependence on stressing time and is saturated after prolonged stressing. In their model, they assumed that high-k traps have a continuous distribution in cross sections to derive the observed time dependence. Creation of additional high-k traps during stressing is ignored, and the V_t shift is solely due to trapping of electrons in preexisting high-k traps. On the other hand, Shanware *et al.* showed that the V_t shift has a log-time dependence and no saturation. They attributed the V_t shift to electron tunneling into high-k traps with a continuous distribution in space and also could explain the log-time dependence. Nevertheless, they ignored trap creation during stressing, too.

In this paper, we use a fast transient technique to characterize PBTI-induced drain current degradation. With this measurement setup, we are able to monitor the drain current evolution over seven decades of time (from 10^{-3} to 10^4 s). We find that the drain current degradation exhibits two stages. The first stage has a log-time dependence, whereas the second stage follows a power-law dependence on stress time. The onset time of the second stage is related to stress voltage, stress temperature, and device process condition. To characterize high-k trap growth rate, a recovery transient technique is developed [16], [17]. We also perform charge-pumping (CP) measurement for comparison. The impact of process effect on the two-stage degradation behavior is discussed.

II. Experimental

The gate stack in our measured devices consists of a poly-Si gate electrode, HfSiON as the high-k layer with physical thickness of 2.5 nm, and a 1.3-nm-thick interfacial SiO_2 layer. The transistors have an equivalent oxide thickness (EOT) of 1.8 nm, a gate length of 0.08–100 μm, and a gate width of

Manuscript received September 15, 2005; revised February 22, 2006. This work was supported by the National Science Council under Contract NSC93-2215-E009-032. The review of this paper was arranged by Editor G. Groeseneken.

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Digital Object Identifier 10.1109/TED.2006.874160

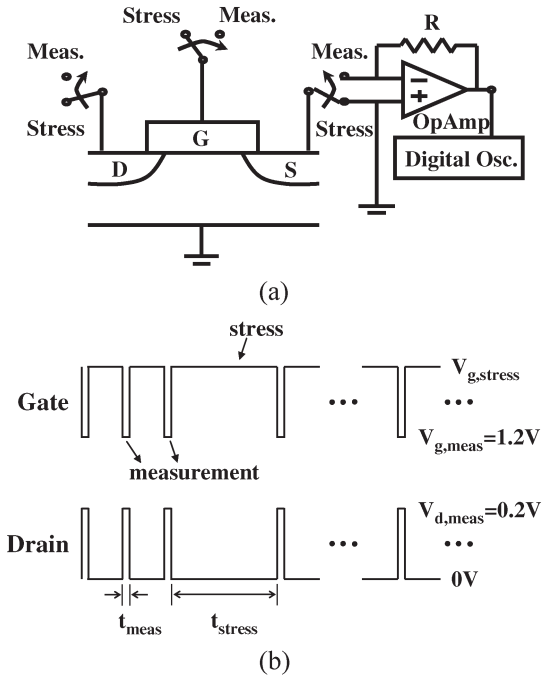

Fig. 1. (a) Setup for fast transient measurement. The high-speed switches minimize the transition delay down to microseconds between stress and drain current measurement. (b) Pulses applied to gate and drain for stress and measurement. The measurement time is chosen on a log-time base. The measurement condition is $V_{g,\mathrm{meas}} = 1.2$ V, $V_{d,\mathrm{meas}} = 0.2$ V, and $t_{\mathrm{meas}} = 50$ μs.

0.16–100 μm. Detailed process conditions and device characteristics can be found in [2], [15].

Conventionally, BTI characterization is carried out by periodically interrupting stress to measure device electrical parameters such as V_t or drain current (I_d) degradation. A delay as long as a few seconds is introduced as a result of switching between stress and measurement. Inasmuch as poststress HfSiON CMOS exhibits a large recovery effect in the millisecond range, the above delay will significantly underestimate the degradation and may lead to an erroneous interpretation [12], [16], [18]. Therefore, throughout this paper, a transient measurement technique illustrated in Fig. 1(a) is employed to measure PBTI-induced drain current degradation [12], [16]. The computer-automated transient measurement system consists of high-speed analog switches, an operational amplifier, and a digital oscilloscope. The high-speed switches minimize the switching delay down to microseconds. I_d rather than V_t is monitored because measurement of V_t requires a sweep in V_g, thus requiring a longer measurement time. The waveforms applied to the gate and drain are depicted in Fig. 1(b). Measurement phase is inserted into stress phase on a log-time base. The measurement bias is $V_g/V_d = 1.2$ V/0.2 V, and the measurement time (t_{meas}) is chosen to be 50 μs such that it is long enough for integrating reliable signals and short enough to avoid introducing additional stress.

III. Results and Discussion

A. Two-Stage Degradation

As shown in Fig. 2, the drain current degradation initially evolves relatively slowly. After a certain stress time, denoted by

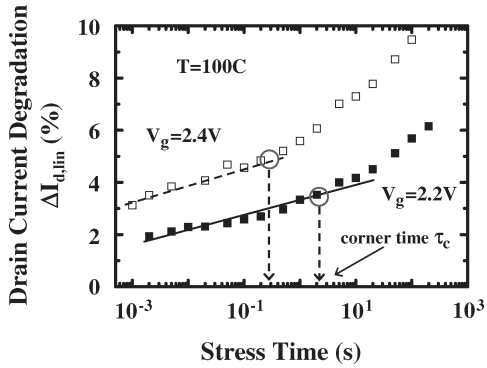

Fig. 2. Linear drain current degradation measured at $V_g/V_d = 1.2$ V/0.2 V. The PBTI stress is at $V_g = 2.2$ and 2.4 V and $T = 100$ °C. The onset time of the accelerated degradation is denoted by τ_c (corner time). The first-stage degradation is before τ_c, whereas the second stage is after τ_c.

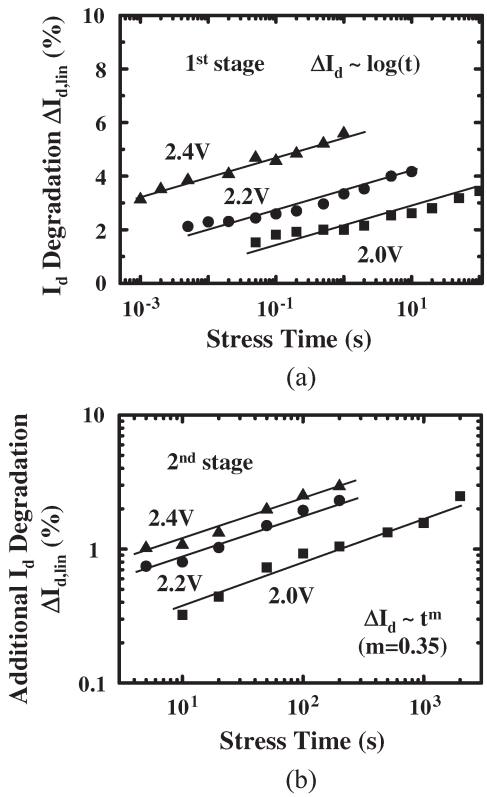

Fig. 3. Drain current degradation rate: (a) in the first stage and (b) in the second stage. The second-stage degradation is obtained by subtracting the extrapolation of the first-stage degradation from the measured I_d degradation.

τ_c in Fig. 2, accelerated degradation is observed. The acceleration was also observed in literature [11, Figs. 4 and 5], whereas the authors attributed the imperfect log-time dependence to a nonuniform initial trap distribution. The drain current degradation versus stress time before τ_c ("the first stage" hereafter) and after τ_c ("the second stage") is plotted in Fig. 3(a) and (b), respectively. The stress conditions are $V_g = 2{-}2.4$ V and $T = 100$ °C. The second-stage degradation is obtained by subtracting the extrapolation of the first-stage degradation from the measured I_d degradation. Notably, the first-stage I_d degradation [Fig. 3(a)] has a $\log(t)$ dependence, whereas the second-stage I_d degradation [Fig. 3(b)] exhibits a power-law time dependence with a power factor of 0.35 without regard

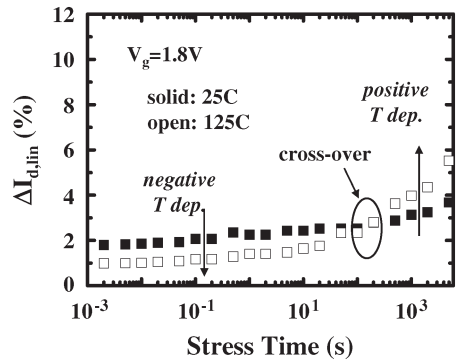

Fig. 4. Stress temperature effect on I_d degradation at $V_g = 1.8$ V. A crossover of the I_d degradation at $T = 25$ °C and 125 °C is noticed.

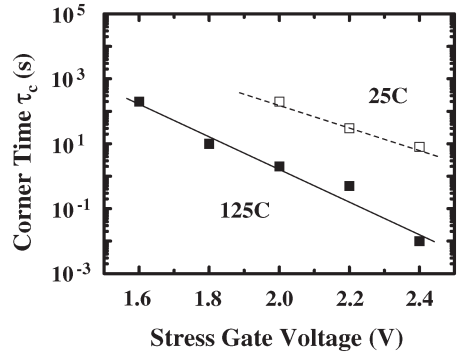

Fig. 5. Corner time τ_c versus stress V_g at $T = 25$ °C and 125 °C. The I_d degradation is driven into the second stage earlier (a smaller τ_c) at higher stress V_g and temperature.

to stress V_g. Stress temperature effect is also characterized in Figs. 4 and 5. Three points are worth noting.

1) At a higher stress temperature, the I_d degradation enters the second stage earlier or a smaller τ_c.
2) The first-stage current degradation has negative stress temperature dependence, i.e., a smaller drain current degradation at a higher stress temperature. Nevertheless, the second stage shows an opposite trend, a positive temperature effect. A crossover of the drain current degradations at $T = 25$ °C and 125 °C is noticed (Fig. 4). The opposite temperature dependence implies that the dominant degradation mechanisms in the first and second stages are different.
3) The degradation is driven into the second stage earlier at a higher stress V_g. For example, the corner time is around 10 s for $V_g = 1.8$ V and 1 s for $V_g = 2.2$ V in Fig. 5.

B. Degradation Model

The $\log(t)$ degradation rate in the first stage suggests that charging [11] and concomitant discharging [12] of preexisting high-k traps dominate the first-stage I_d degradation. A higher V_g induces a larger electron density in the inversion channel readily for trapping, thus causing a more severe I_d degradation. The negative temperature dependence can be explained as follows. Inasmuch as the high-k charge detrapping rate increases with temperature [12], a higher temperature results in a smaller net charge trapping rate and thus a smaller drain current degradation. On the other hand, new high-k traps are created during stress. At a certain stress time (the aforementioned "corner time"), the additionally created high-k trap density reaches a level comparable to or even more than preexisting ones. Charging and discharging of the preexisting traps are then no longer the limiting process. Thus, the drain current degradation is dictated by trap generation, which exhibits a power-law stress-time dependence [5]. Furthermore, larger stress V_g and higher temperatures lead to faster high-k trap generation in the second stage (Figs. 2–4) because of larger carrier fluence and energy [4], [5] and thus an accelerated thermochemical reaction for trap creation [8]. As a result, the device I_d degradation is driven into the second stage earlier (or a smaller τ_c) at higher stress V_g and/or temperature.

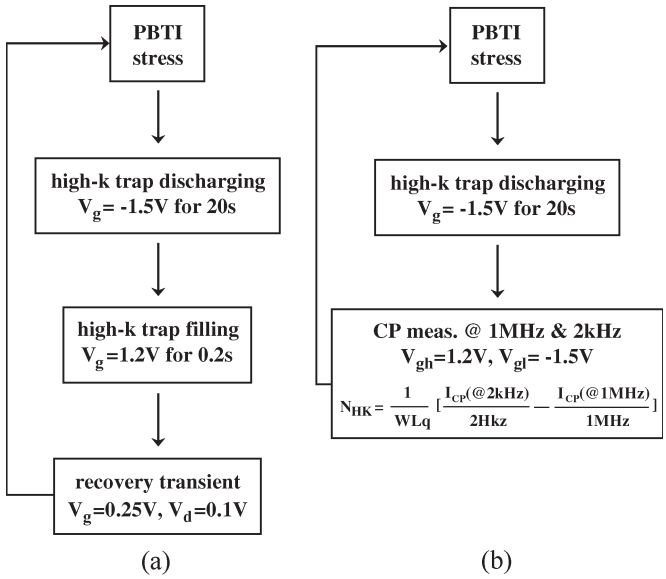

Fig. 6. Characterization procedure of two high-k trap density extraction methods. (a) Drain current recovery transient technique. (b) Two-frequency CP technique.

C. High-k Trap Growth Rate

To characterize high-k trap growth, two techniques are employed, namely 1) a recovery transient technique [16], [17] and 2) a CP technique [5]. The characterization procedure of these two techniques is shown in Fig. 6. The devices are first subject to PBTI stress followed by a discharging step to empty the high-k traps. The discharging step is necessary or the residual trapped charges generated by PBTI stress would detrap during the recovery transient or CP measurement, giving rise to incorrect results.

1) Recovery Transient Technique: After the discharging, a moderate V_g ($= 1.2$ V) is applied for 0.2 s to fill high-k traps with electrons, and the drain current is measured at $V_g/V_d = 0.25$ V/0.1 V immediately after the filling. Fig. 7 shows the drain current recovery transients in a fresh device, after 1-s stress, and after 2000-s stress. The device dimension is $W/L = 100\ \mu$m$/0.08\ \mu$m. A large transient in the millisecond range is observed, suggesting an underestimate of the stress effect from conventional measurement. All curves in Fig. 7 have $\log(t)$

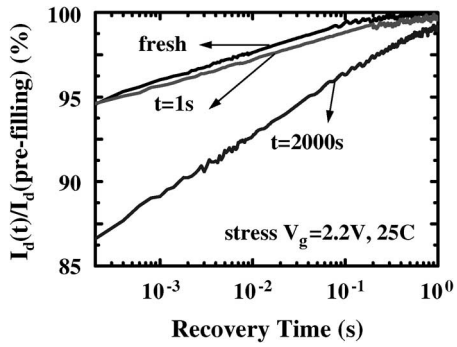

Fig. 7. Drain current recovery transients measured at $V_g/V_d = 0.25$ V/0.1 V for different PBTI stress times: $t = 0, 1,$ and 2000 s. Device dimension is $W/L = 100\ \mu\text{m}/0.08\ \mu\text{m}$.

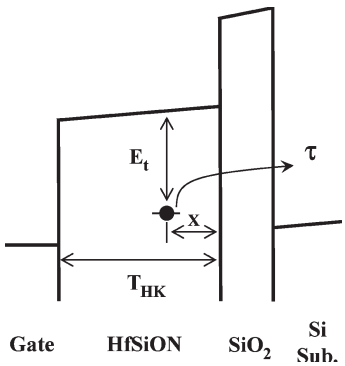

Fig. 8. Energy band diagram illustrating high-k trapped charge detrapping during drain current recovery transient.

dependence. The recovery rate (i.e., the slope in Fig. 7) at $t = 1$ s is about the same as in the fresh device and increases considerably at $t = 2000$ s. Our previous study has shown that the drain current recovery is caused by detrapping of charges spatially distributed in the high-k layer [16], [17]. Concerning a high-k trapped charge at a distance x from the HfSiON/SiO_2 interface, as illustrated in Fig. 8, the charge tunneling emission time can be written as

$$\tau(x) = A\ \exp(\alpha_k x) \tag{1}$$

where the prefactor A is a function of trap cross section, recovery V_g and temperature, thickness of the interfacial SiO_2, and the HfSiON/SiO_2 conduction band offset [17], and

$$\alpha_k = \frac{2\sqrt{2m_k^* q E_t}}{\hbar} \tag{2}$$

with m_k^* as the electron effective mass in the high-k layer and E_t as the trap energy. The threshold voltage shift as a result of high-k trapped charge emission thus can be approximated as

$$\Delta V_t(t) = \int_0^x \frac{qN_{\text{HK}}^V(x,0)}{\varepsilon_{\text{HK}}}(T_{\text{HK}} - x) \times \{1 - \exp\left[-t/\tau(x)\right]\}\, dx \propto \frac{qN_{\text{HK}}^V T_{\text{HK}}}{\varepsilon_{\text{HK}}\alpha_k}\log(t) \tag{3}$$

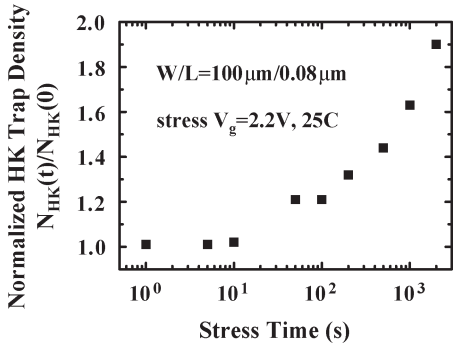

Fig. 9. High-k trap density versus stress time from the recovery transient technique. The trap density is normalized to the initial high-k trap density.

where N_{HK}^V is the volumic trap density in the high-k gate dielectric, ε_{HK} is the dielectric constant, and T_{HK} is the thickness of the HfSiON layer. Other variables have their usual definition. The corresponding drain current change is then readily obtained as

$$\Delta I_d(t) \propto G_m \Delta V_t(t) \propto \frac{qN_{\text{HK}}^V T_{\text{HK}}}{\varepsilon_{\text{HK}}\alpha_k}\log(t) \tag{4}$$

where $G_m = dI_d/dV_g$ is obtained from measurement. In the above equation, the slope of the $\Delta I_d - \log(t)$ plot is linearly proportional to the high-k trap density. Therefore, we can extract the high-k trap density from the recovery slope, and the result is shown in Fig. 9. Our result shows that the high-k trap density in the first stage ($\tau_c \sim$ tens of seconds) is dominated by preexisting traps. The high-k trap density, however, increases drastically in the second stage. Moreover, as reported in our earlier paper [12], [16], individual electron detrapping from the high-k dielectric can be observed directly in a small-area device, which is manifested by a staircase evolution of the recovery drain current rather than a continuous $\log(t)$ increase with time. Fig. 10 compares the prestress and poststress recovery drain current evolutions in a small-area device ($W = 0.16\ \mu$m, $L = 0.08\ \mu$m). Each current jump in the current evolution accounts for a single charge detrapping. Apparently, the poststress device has more current jumps in the same measurement period than the prestress device (from one jump in a fresh device to five jumps after 100 s stress). This result, again, provides evidence of high-k trap generation during PBTI stress.

2) CP Technique: We also characterize high-k trap generation by using a two-frequency CP method. The experimental procedure is described in Fig. 6(b). The PBTI stress condition is identical to that used in Fig. 6(a). The high-k trap density is obtained from the difference between CP results at two frequencies, i.e.,

$$N_{\text{HK}} = \frac{1}{WLq}\left[\frac{(I_{\text{CP}}\text{ at 2 kHz})}{2\text{ kHz}} - \frac{(I_{\text{CP}}\text{ at 1 MHz})}{1\text{ MHz}}\right]. \tag{5}$$

Note that N_{HK} in the above equation denotes the number of traps per unit area. The choice of 2 kHz as the lower CP measurement frequency is somewhat arbitrary, and N_{HK} reflects only the relative high-k trap density. Fig. 11 shows normalized high-k trap growth in various stress conditions. A larger stress

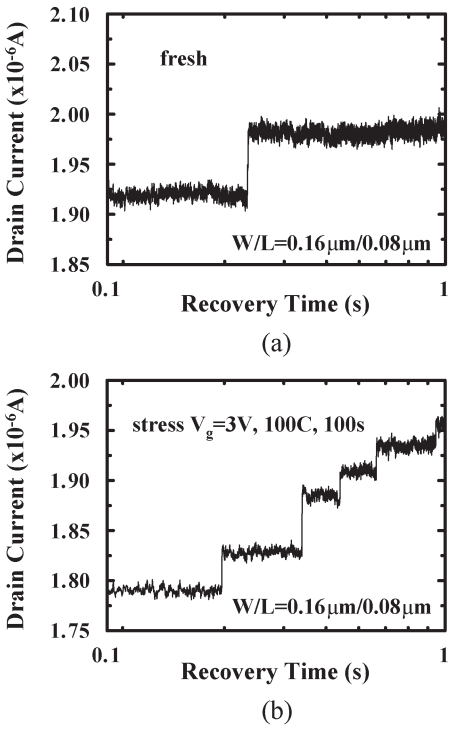

Fig. 10. Drain current recovery transient in a small-area device with $W/L = 0.16\ \mu\text{m}/0.08\ \mu\text{m}$. (a) Fresh device where only one current jump appears. (b) After stress at $V_g = 3$ V, $T = 100\ ^\circ$C for 100 s, five current jumps are observed in the same measurement interval. The increase in the number of current jumps indicates new high-k trap generation.

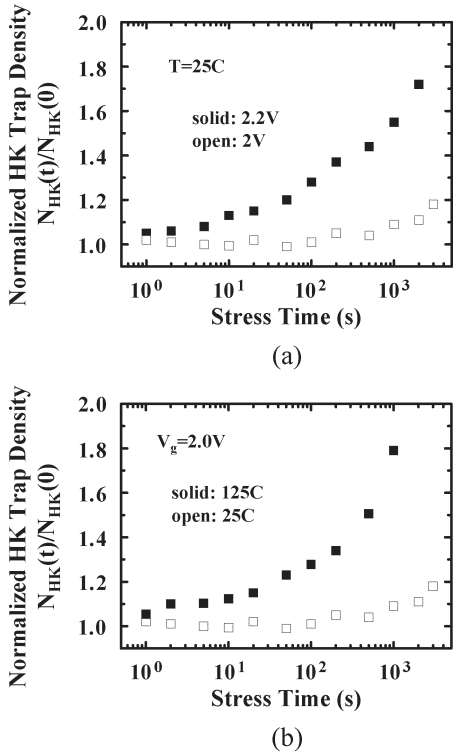

Fig. 11. High-k trap density versus time from the CP technique. The trap density is normalized to the initial high-k trap density. (a) Stress temperature $= 25\ ^\circ$C. (b) Stress voltage $= 2$ V.

V_g [Fig. 11(a)] and/or a higher stress temperature [Fig. 11(b)] result in a larger trap generation rate and drive the device into the second stage earlier. This is consistent with Fig. 5. Fig. 12 compares the high-k trap density measured from the recovery transient technique and from the CP technique. N_{HK}^{V} from the recovery slope method is multiplied by the thickness of the high-k layer in Fig. 12. Note that the areal high-k trap density extracted from the CP method is about three times lower than that from the recovery transient technique. The reason is that high-k dielectric traps are distributed in space. The inverse of the frequency used in CP measurement determines the depth into the high-k dielectric the electron tunneling front can reach. Thus, only high-k traps that has a tunneling time shorter than the inverse of the CP frequency can contribute to the CP current. In other words, only a small portion of high-k dielectric traps can be detected by the CP method. Despite the absolute value of the trap density, the trap growth rate from the two methods follows the same power-law time dependence with an exponent of ~ 0.33, which is close to that in Fig. 3(b).

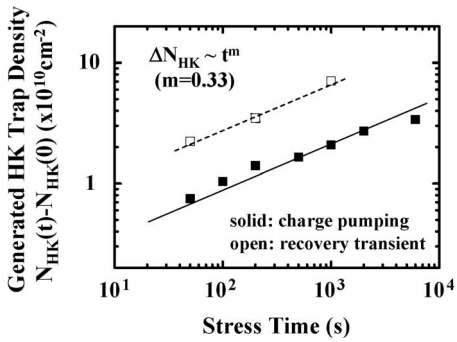

Fig. 12. Generated high-k trap density versus stress time from the recovery transient and the CP techniques. The stress condition is $V_g = 2.2$ V and $T = 25\ ^\circ$C.

D. Process Effect

Appropriate nitrogen incorporation into Hf-silicate can substantially improve the gate dielectric electrical reliability [15]. To evaluate the nitrogen effect on HfSiON nMOSFET degradation, two devices, i.e., "optimal" versus "control," which have different nitrogen profiles in the HfSiON gate dielectric, are compared. The high-k film in the optimal sample remains amorphous, whereas that in the control becomes crystallized after 1100 °C annealing of source/drain dopant activation [15]. The time-to-breakdown, hot carrier, and PBTI lifetime are improved, with other parameters such as V_t and gate leakage current not adversely affected. High-k bulk trap generation is suppressed in the optimal samples. Detailed comparisons and discussions are summarized in [15]. The two devices have almost identical $I_d - V_g$ characteristic, as shown in the inset of Fig. 13. After PBTI stress, the normalized trap density from the CP method for these two samples is shown in Fig. 13. A large trap density difference between high- and low-frequency CP measurements in the control sample suggests considerable high-k trap creation during stress. On the other hand, the optimal device shows better robustness against high-k trap generation. Correspondingly, Fig. 14 shows the drain current degradation versus stress time in the two samples. Again, the optimal device shows smaller degradation. We also evaluate

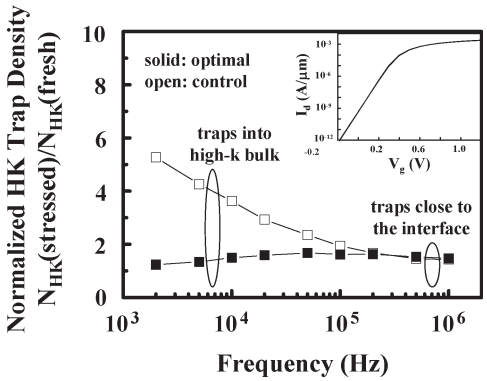

Fig. 13. Normalized trap density versus CP measurement frequency in the control and optimal samples. PBTI stress condition is $V_g = 2.2$ V and $T = 125\,^{\circ}$C. The prestress $I_d - V_g$ characteristics in the control and optimal samples are shown in the inset.

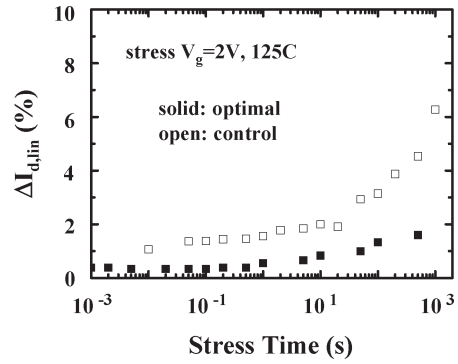

Fig. 14. Comparison of I_d degradation in the two samples. The optimal nitrogen incorporation sample shows lower initial trap density and better stress immunity.

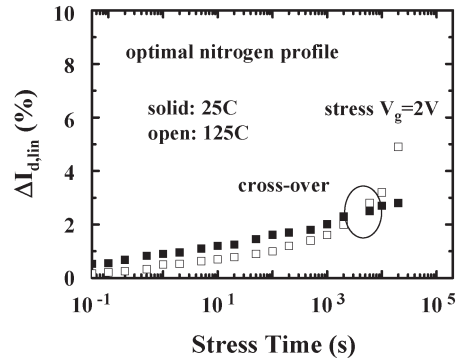

Fig. 15. Stress temperature effect on I_d degradation rate in the optimal sample. The crossover is still observed, indicating the existence of two-stage degradation in the optimal sample.

the stress temperature effect in the optimal sample (Fig. 15). Opposite temperature dependence between the first stage and the second stage is still observed. The crossover time in the sample is about 10^4 s, much longer than ~ 20 s in the control sample.

IV. Conclusion

HfSiON gate dielectric nMOSFETs exhibit two-stage drain current degradation in PBTI stress. The first-stage drain current degradation is attributed to the charging of preexisting high-k traps, whereas the second-stage degradation is mainly caused by new high-k trap creation. The degradation rate and stress temperature effect in the two stages have been characterized. Larger stress gate voltages and/or elevated temperatures shorten the time required to enter the second stage. High-k trap density is characterized by two different methods. The trap growth rate follows a power-law stress-time dependence in the second stage. Finally, an optimized nitrogen profile in HfSiON layer is demonstrated to have better stress immunity and thus prolongs the time to enter the second stage. An accurate PBTI lifetime extrapolation strategy should be built upon the physics considering both degradation stages.

Acknowledgment

The authors would like to thank Taiwan Semiconductor Manufacturing Company (TSMC/NCTU JDP program) for the technical support.

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