Novel Dual-Metal Gate Technology Using Mo−$MoSi_x$ Combination

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***Abstract*—A novel dual-metal gate technology that uses a combination of Mo−$MoSi_x$ gate electrodes is proposed. An amorphous-Si/Mo stack was fabricated as a gate electrode for the n-channel device. It was thermally annealed to form $MoSi_x$. Pure Mo served as the gate electrode for the p-channel device. The work functions of $MoSi_x$ and pure Mo gates on SiO_2 are 4.38 and 4.94 eV, respectively, which are appropriate for devices with advanced transistor structures. The small increase in the work function ($<$ 20 meV) and the negligible equivalent oxide thickness variation ($<$ 0.08 nm) after rapid thermal annealing at 950 °C for 30 s also demonstrate the excellent thermal stabilities of Mo and $MoSi_x$ on SiO_2. Additional arsenic ion implantation prior to silicidation was demonstrated further to lower the work function of $MoSi_x$ to 4.07 eV. This approach for modulating the work function makes the proposed combination of Mo−$MoSi_x$ gate electrodes appropriate for conventional bulk devices. The developed dual-metal-gate technology on HfO_2 gate dielectric was also evaluated. The effective work functions of pure Mo and undoped $MoSi_x$ gates on HfO_2 are 4.89 and 4.34 eV, respectively. A considerable work-function shift was observed on the high-κ gate dielectric. The effect of arsenic preimplantation upon the work function of the metal silicide on HfO_2 was also demonstrated, even though the range of modulation was a little reduced.**

***Index Terms*—Dual-metal gate, molybdenum, silicide, thermal stability.**

I. Introduction

ACCORDING to the International Roadmap for Semiconductors (ITRS) [1], the introduction of high-κ gate-dielectric materials and dual-metal-gate electrodes with appropriate work functions will be required in the near future to reduce gate-leakage current [2]–[4] and eliminate boron penetration and polydepletion effect [4], [5]. For conventional bulk devices, the required work functions (Φ_m) of n- and p-channel devices are about 4 and 5 eV, respectively. However, the required Φ_m values for n- and p-channel devices with advanced transistor structures, such as FinFET or ultrathin-body (UTB) MOSFETs, are about 4.4–4.6 and 4.8–5.0 eV, respectively [6]. Since the work function of the metals cannot easily be modulated, a straightforward dual-metal gate CMOS process has been proposed, but it degrades the integrity of the gate dielectric by exposing it to the metal etchant [7]. A novel dual-metal-gate technology based on the full silicidation (FUSI) of polysilicon gates has also been reported [8]–[10], and dopants in the polysilicon are believed to be responsible for providing the difference between the work functions of n- and p-type metal-silicide (MeSi) gates [11], [12]. The major advantage of the FUSI method is the ease of process integration. Moreover, since the source/drain dopant activation annealing will be performed prior to silicide formation, the requirement for the thermal stability of MeSi can be alleviated. Thermal treatment prior to silicidation process, however, results in the incomplete elimination of boron penetration in p-channel devices [13]. Additionally, the impurity doping dose has been reported not to help modulate the Φ_m of FUSI-MeSi, such as NiSi and PtSi, on HfON high-κ gate dielectric because of the Fermi-level pinning effect [14]. Consequently, the FUSI gate on high-κ gate dielectric becomes single work function metal-gate candidate and its application is strictly limited. Therefore, Nabatame *et al.* presented a partial silicides technology that uses n^+-polysilicon and n-type MeSi as gate electrodes for n- and p-channel devices, respectively [14]. This approach, however, suffers from the poly depletion effect in n-channel devices.

The Hf–Si bond has been suggested to be responsible for the pinning effect and the large device threshold voltages observed in polysilicon and FUSI gates with an Hf-based gate dielectric [15]. The Hf–Si bond is likely to have been formed during the deposition of polysilicon and may not be eliminated by subsequent annealing or silicidation process [16]. The amount of Hf–Si bonds, which strongly depends on the type and quality of the gate/dielectric interface, becomes the key parameter in controlling the Fermi-level pinning effect. The suppression of the pinning effect by replacing HfO_2 with Si-rich Hf-silicates [16]–[19] or Al-incorporating HfAlON [20], [21] has been proposed. Also, the use of capping layer such as SiO_2 [19] or Al_2O_3 [16] on the high-κ gate dielectric has been reported to reduce effectively the Hf–Si interaction. These improvements, however, come at the expense of a large equivalent oxide thickness (EOT), a reduced average dielectric constant and poor scalability. In addition to the use of the capping layer and the modulation of the Hf concentration in Hf-based high-κ gate dielectric, a novel retardation of the pinning effect has been proposed using phase-controlled FUSI (PC-FUSI) gates [22], [23]. Although a negligible Φ_m difference between NiSi and Ni_3Si can be obtained on SiO_2, a small (about 0.25–0.33 eV) Φ_m difference can be achieved on Hf-based high-κ gate dielectric, and is believed to be caused by Fermi-pinning

Manuscript received September 8, 2005; revised March 2, 2006. This work was supported by the Taiwan Semiconductor Manufacturing Company under Contract 94C222. The review of this paper was arranged by Editor S.-I. Kimura.

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Digital Object Identifier 10.1109/TED.2006.874227

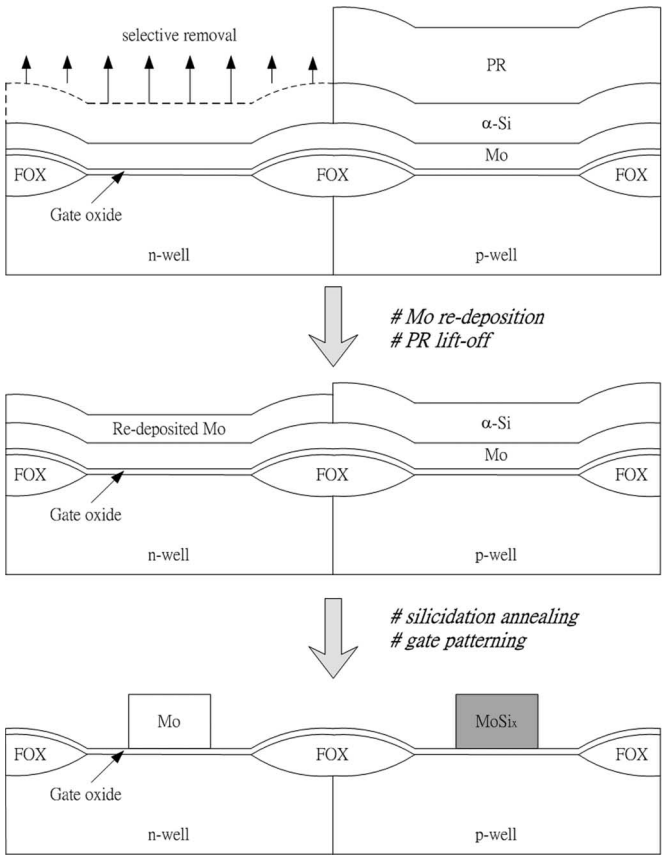

Fig. 1. Schematic illustration of the proposed novel dual-metal-gate technology that uses the combination of Mo−$MoSi_x$ gate electrodes.

relaxation associated with the metal-rich silicide (Ni_3Si), which reduces the number of Hf–Si bonds at the gate-dielectric interface.

This work proposes the use of a combination of Mo−$MoSi_x$ gate electrodes for dual-metal-gate technology. In view of the process integration, the $MoSi_x$ gate was formed by the FUSI of the α-Si/Mo/gate-dielectric stack to prevent the exposure of the gate dielectric in the channel region to the metal etchant. The extracted Φ_m values for $MoSi_x$ and as-deposited pure Mo gates on SiO_2 are appropriate for devices with advanced transistor structures. The small increase in Φ_m and the negligible variation in EOT after rapid thermal annealing (RTA) at 950 °C demonstrate the superior thermal stabilities of Mo and $MoSi_x$ on SiO_2. Implanting additional arsenic prior to silicidation process can further lower the Φ_m of $MoSi_x$ to make it suitable for n-channel bulk devices. The combination of pure Mo and $MoSi_x$ gates on HfO_2 was also demonstrated to provide a considerable Φ_m difference. Moreover, n-type $MoSi_x$ can still have a lower Φ_m value than undoped $MoSi_x$ on HfO_2, even though the range of the work-function modulation is a little smaller than that on SiO_2.

II. Experiments

Fig. 1 schematically depicts the proposed novel dual-metal-gate technology that combines Mo and $MoSi_x$. The first layer metal and α-Si are deposited over the entire wafer in sequence on the gate dielectric. A noncritical lithography step is performed, and an appropriate wet-etching recipe should be investigated to remove selectively the α-Si from the p-MOS side. The redeposition of Mo in the p-MOS region is needed after the selective removal of α-Si, to equalize the thickness of the gate electrode across the entire wafer. Consequently, potential gate patterning and spacer formation challenges can be prevented. Since only Mo remains in the p-MOS region, it solely determines the work function of the p-MOS gate electrode. The remaining α-Si/Mo stack in the n-MOS region will be subsequently transformed into molybdenum silicide and determine the work function of the n-MOS gate electrode. In this process, the gate dielectric in the channel region will not be exposed to the metal etchant, therefore, the side effects encountered in the straightforward dual-metal-gate technology [7] can be prevented. Notably, the thermal stability of the selected metal film on the gate dielectric should be sufficiently high to ensure that no interaction occurs between the metal and the gate dielectric during the silicidation and following high-temperature processes. The (110) Mo gate has been reported to have a work function that is appropriate for the p-channel device [24], [25] and exhibits high thermal stability (1000 °C) on the SiO_2 gate dielectric [26]. Accordingly, pure Mo will be adopted as the first-layer metal so that the Φ_m value and the thermal stability of the formed $MoSi_x$ become the main issue.

MOS capacitors with Mo/gate dielectric/n-Si and α-Si/Mo/gate dielectric/n-Si structures were fabricated on 6-in Si wafers. After the local-oxidation-of-silicon (LOCOS) isolation, thermal SiO_2 (3, 6, and 9 nm) or metal organic chemical vapor deposition (MOCVD) HfO_2 (5, 7.5, and 10 nm) was deposited as the gate dielectric. According to the ITRS, the thickness of the gate electrode must be reduced as the MOSFET devices are miniaturized [1]. To meet this criterion, a thin (10 nm) layer of Mo was sputter deposited on top of the gate dielectrics for all samples. Some samples were followed by sputter deposition of α-Si (25 nm). The gate electrodes were then patterned by reactive ion etching (RIE) using Cl_2-based chemistry. After the gate-electrode patterning, some of the samples with an α-Si/Mo/gate-dielectric stack were then subjected to arsenic implantation $(1 \times 10^{15}, 5 \times 10^{15}\ \text{cm}^{-2})$. The low implantation energy (10 keV), corresponding to a projected implant-range (R_p) value of one half of the thickness of the α-Si layer, was employed to avoid the direct implantation of dopants into the channel region. Samples with an α-Si/Mo/gate-dielectric stack were then subjected to successive RTA $(600\ ^\circ\text{C}, 1\ \text{min.} + 700\ ^\circ\text{C}, 1\ \text{min.} + 800\ ^\circ\text{C}, 1\ \text{min.})$ in N_2 ambient for $MoSi_x$ formation. All samples were then subjected to 950 °C RTA for 30 s to evaluate the thermal stabilities of the gate electrodes. The flatband voltage (V_{FB}) and EOT were extracted from the measured capacitance–voltage $(C$–$V)$ curve using the quantum mechanical C–V (QMCV) simulator [27]. The Φ_m values of the gate electrodes were then extrapolated from the V_{FB}–EOT plots by setting the electron affinity (χ) of the Si substrate to 4.05 eV.

III. Results and Discussion

Fig. 2 shows the C–V characteristics of the capacitor (MOSCAP) devices gated by α-Si/Mo stack before and after

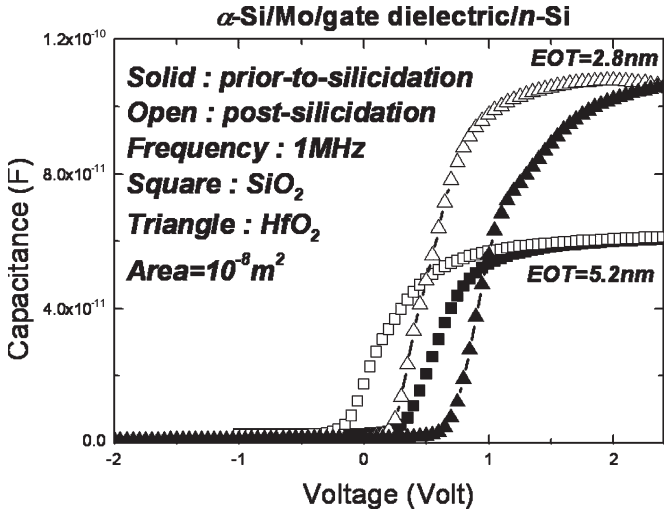

Fig. 2. C–V characteristics of MOSCAP devices with α-Si/Mo/SiO_2 (or HfO_2)/n-Si structure before and after silicidation annealing.

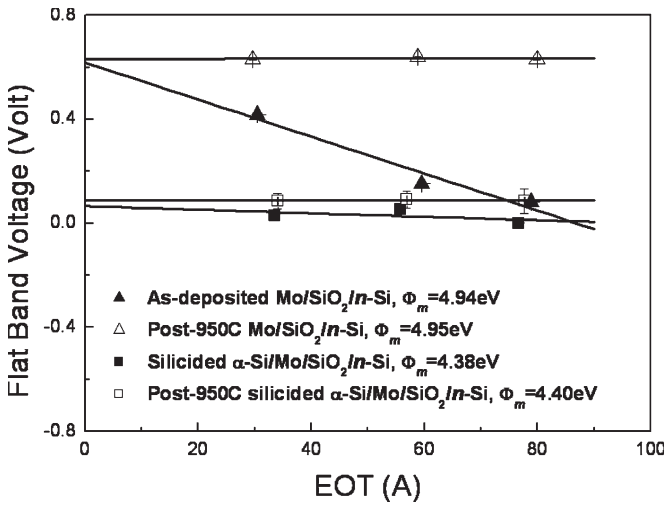

Fig. 3. V_{FB} versus EOT plots of Mo and $MoSi_x$ gated MOSCAP devices before and after 950 °C RTA for thermal-stability evaluation.

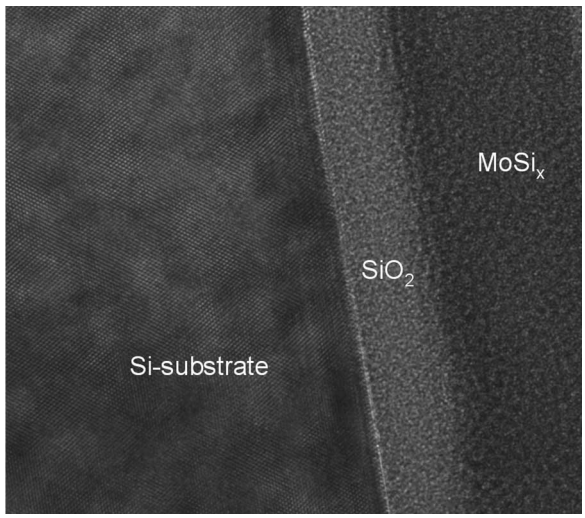

Fig. 4. TEM image of the postsilicidation α-Si/Mo/SiO_2 stack.

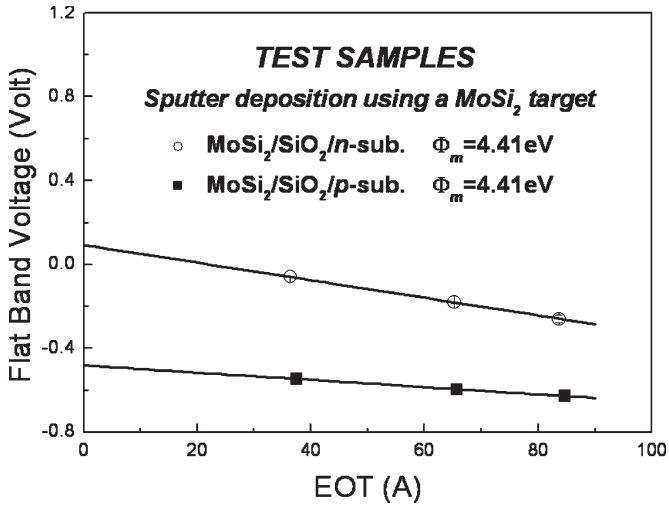

Fig. 5. Work-function extraction of $MoSi_2$ films that were sputter deposited on SiO_2 using the $MoSi_2$ target.

silicidation annealing. A negative postsilicidation flatband voltage shift without EOT variation can be observed for both SiO_2 and HfO_2 gate dielectrics. The change in the work function of the gate electrode and the reduction of the fixed charge can contribute to the flat-band voltage shift.

Fig. 3 reveals that both as-deposited Mo/SiO_2 and postsilicidation α-Si/Mo/SiO_2 samples exhibit linear behavior in V_{FB}–EOT plots. The large fixed oxide charge density in the as-deposited Mo/SiO_2 sample may be caused by the damage done by sputtering and can be reduced by high-temperature annealing. The Φ_m values of the as-deposited pure Mo film and the formed $MoSi_x$ on SiO_2 are extracted to be 4.94 and 4.38 eV, respectively, so the Φ_m difference is 0.56 eV. Moreover, the small increase in Φ_m (Mo: 10 meV; $MoSi_x$: 20 meV) along with the negligible EOT variation (Mo: 0.08 nm; $MoSi_x$: 0.06 nm) after RTA at 950 °C demonstrates the excellent thermal stabilities of Mo and $MoSi_x$ films on SiO_2. Fig. 4 shows the TEM image of the postsilicidation sample, confirming the smooth gate electrode/SiO_2 interface.

$MoSi_2$ has been reported to be likely the only silicide phase observed for the Mo:Si $= 1:2$ stacked samples annealed at a temperature of higher than 600 °C [28]. MOSCAP devices gated by the sputtering deposition of $MoSi_2$ using the $MoSi_2$ target were also fabricated. The V_{FB} versus EOT plots of $MoSi_2/SiO_2$/n-Si and $MoSi_2/SiO_2$/p-Si structures yielded the work function of the $MoSi_2$ film that was sputter deposited on SiO_2 using the $MoSi_2$ target at 4.41 eV, regardless of the dopant of the substrate, as shown in Fig. 5. Moreover, the X-ray photoelectron spectroscopy (XPS) analysis was also performed to estimate the chemical condition of the silicided film. Figs. 6 and 7 compare the Si 2p and Mo 3d spectra of the silicided films with those of pure Si and pure Mo, respectively. The binding energies that correspond to the Si 2p spectrum of pure Si and the silicided film obtained in this paper were 99.4 and 99.0 eV, respectively. Similarly, the binding energies that correspond to the Mo 3d spectrum of pure Mo and the silicided film were 228.2 and 228.0 eV, respectively. Both the binding energy that corresponds to the Si 2p spectrum of the pure Si film and that

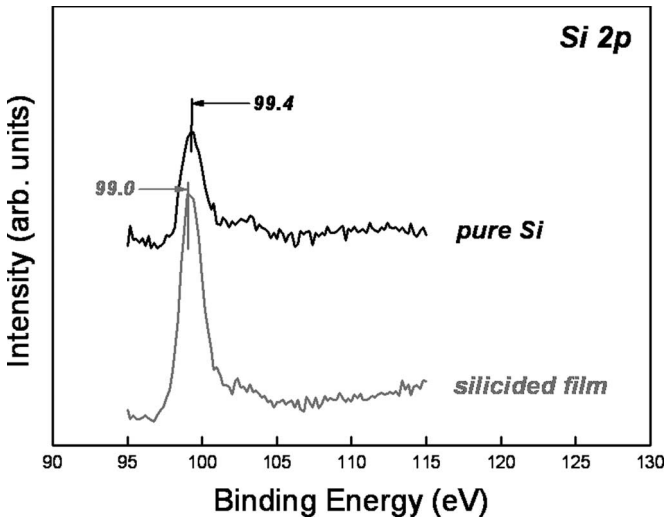

Fig. 6. XPS analysis shows that the binding energy, which corresponds to Si 2p spectrum, of the silicided films is 0.4 eV lower than that of the pure Si.

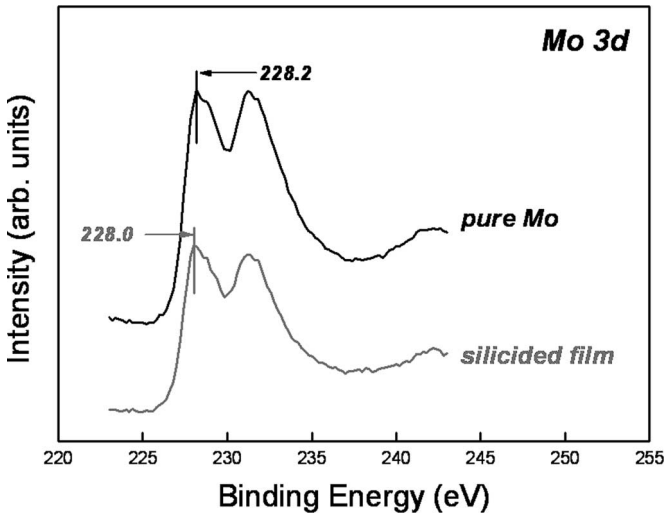

Fig. 7. XPS analysis shows that the binding energy, which corresponds to Mo 3d spectrum, of the silicided films is 0.2 eV lower than that of the pure Mo.

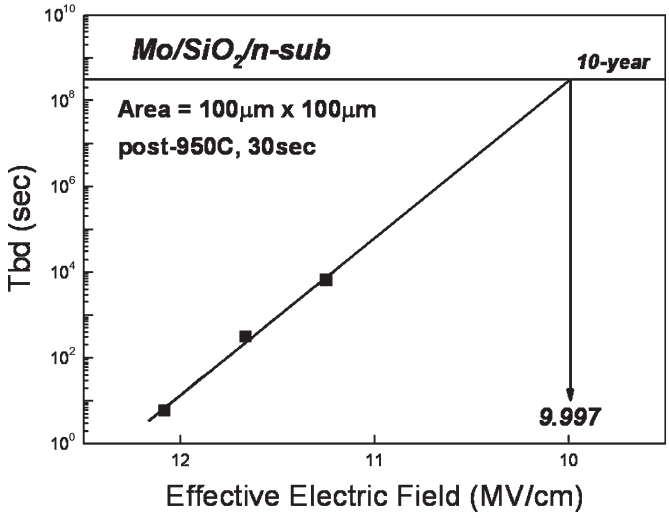

Fig. 8. TDDB lifetime projection of the Mo/SiO_2 device. Superior TDDB characteristic for pure Mo gate annealed by 950 °C RTA for 30 s is demonstrated.

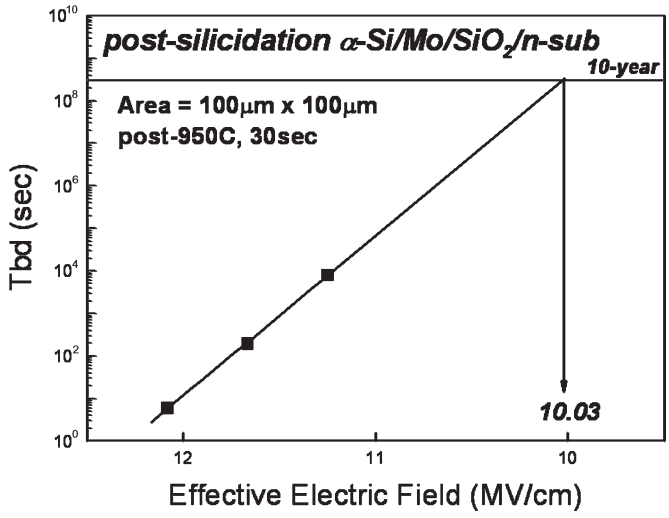

Fig. 9. TDDB lifetime projection of the postsilicidation α-Si/Mo/SiO_2 device. Superior TDDB characteristic for the $MoSi_x$ gate annealed by 950 °C RTA for 30 s is demonstrated.

which corresponds to the Mo 3d spectrum of the pure Mo film are strongly consistent with the reported handbook data [29]. Furthermore, a downward shift in the binding energy of 0.4 eV for the silicided films is observed from the Si 2p spectra. The magnitude of this shift is close to the value previously reported for $MoSi_2$ (-0.3 eV) [30]. Similarly, a downward shift in the binding energy of 0.2 eV for silicided films is observed from Mo 3d spectra, and the magnitude of the binding-energy shift corresponds closely to the previously reported values (-0.2 eV) [31]. Accordingly, we speculate that $MoSi_2$ is the main constituent of the $MoSi_x$ film formed in this paper, and the full silicidation of the Mo layer is responsible for the large shift in the work function after silicidation annealing.

The constant voltage stressing (CVS) method was employed to generate the ten-year lifetime projections of Mo/SiO_2 (2.3 nm) and postsilicidation α-Si/Mo/SiO_2 (2.4 nm) devices at room temperature for oxide integrity evaluation. Figs. 8 and 9 show that pure Mo and $MoSi_x$ gates have superior time dependent dielectric breakdown (TDDB) characteristics, respectively, after 950 °C RTA for 30 s. Fig. 10 compares the accumulation leakage-current densities of Mo/SiO_2/n-Si and postsilicidation α-Si/Mo/SiO_2 devices to investigate further the possible metal interdiffusion into the oxide or channel region following high-temperature annealing. Both devices were annealed by 950 °C RTA for 30 s, and the $MoSi_x/SiO_2$ device exhibited slightly higher leakage-current density than the Mo/SiO_2 device. This increase in the leakage current may be caused by the additional thermal budget required for the formation of metal silicide. Notably, pure Mo has been demonstrated as a p^+-polysilicon-compatible gate candidate for PMOS with negligible metal contamination and metal diffusion [32]. The comparable TDDB characteristics and leakage-current densities of pure Mo and $MoSi_x$ gated devices also reveal that the silicidation process required for the formation of $MoSi_x$ will not severely degrade the device performance or oxide integrity.

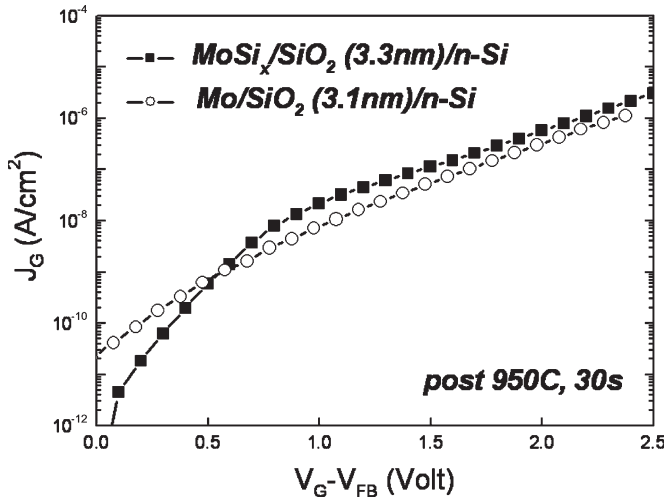

Fig. 10. Accumulation leakage-current densities of Mo/SiO_2/n-Si and $MoSi_x$/SiO_2/n-Si devices annealed by 950 °C RTA for 30 s.

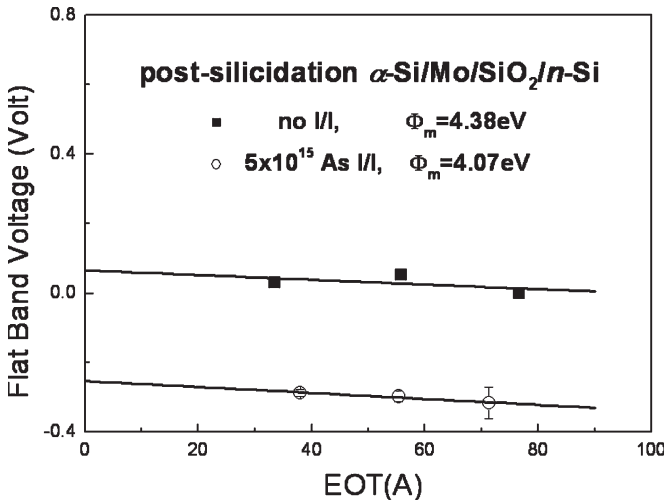

Fig. 11. $V_{\rm FB}$ versus EOT plots of postsilicidation α-Si/Mo gated MOSCAP devices with (5×10^{15} cm^{-2}) and without arsenic preimplantation.

Fig. 11 indicates that postsilicidation α-Si/Mo/SiO_2 with and without arsenic preimplantation exhibit linear $V_{\rm FB}$ versus EOT plots. A parallel shift in the $V_{\rm FB}$ versus the EOT plot is observed. Evidently, the incorporation of low-energy arsenic preimplantation indeed leads to the modulation of the work function, rather than the channel dopant-induced adjustment in the threshold voltage. Fig. 12 summarizes the effect of the arsenic preimplantation dosage upon the magnitude of the work-function modulation. The extracted Φ_m values of $MoSi_x$ on SiO_2 with the preimplantation of 1×10^{15} and 5×10^{15} cm^{-2} doses of arsenic are 4.19 and 4.07 eV, respectively. Although the introduction of arsenic impurities has been demonstrated to expand the difference between the Φ_m of $MoSi_x$ and pure Mo, and to extend the range of applications of the proposed approach from devices with advanced structures to conventional bulk devices; the exact mechanism of the modulation of the work function by the preimplantation of As is still under investigation.

Fig. 13 plots the dependence of Φ_m on the gate-dielectric material. Effective Φ_m values of pure Mo and $MoSi_x$ gates on

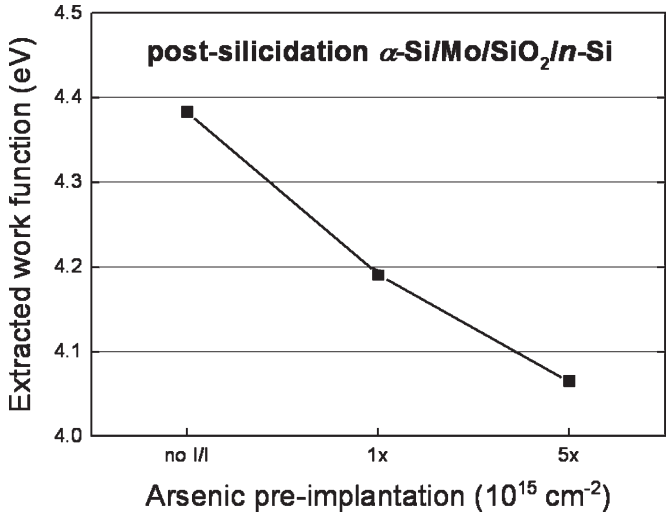

Fig. 12. Dependence of Φ_m values of postsilicidation α-Si/Mo/SiO_2 gated MOSCAP devices on doses of arsenic preimplantation.

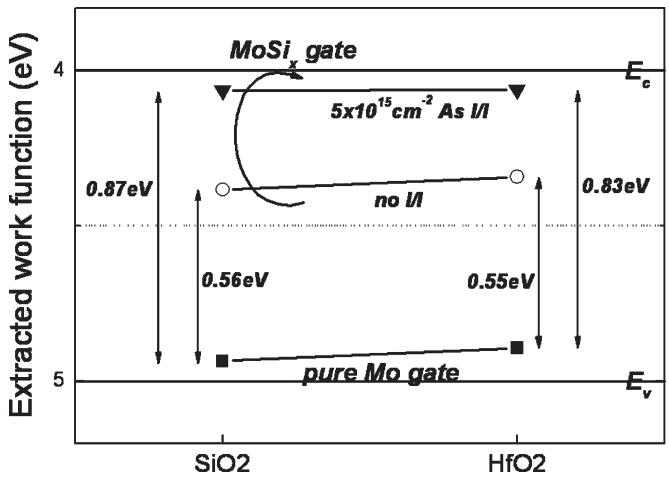

Fig. 13. Dependence of Φ_m values on gate-dielectric material.

HfO_2 are reduced slightly to 4.89 and 4.34 eV, respectively, while maintaining a large Φ_m difference of 0.55 eV, regardless of the underlying gate-dielectric materials. This observation is consistent with the results of Lee *et al.* [33]. Notably, arsenic preimplantation can still lower the effective Φ_m value of $MoSi_2$ on the HfO_2 gate dielectric. The effective Φ_m of $MoSi_x$ on HfO_2 with the preimplantation of arsenic at a dose of 5×10^{15} cm^{-2} is found to be 4.06 eV, which is 0.28 eV lower than that of the undoped sample. As mentioned above, preimplantation of impurities does not help modulate the Φ_m of FUSI gates on the HfO_2 gate dielectric because of the Fermi-level pinning effect [14]. By contrast, the possibility of Φ_m modulation using the dopant preimplantation is still maintained herein, even though a small reduction (0.03 eV) in the modulation range can be observed. This improvement may be attributed to the use of Mo as the first-layer metal, which effectively separates most Si atoms from the gate/HfO_2 interface prior to its participation in silicidation. The formation of Hf-Si bonds during α-Si deposition or silicidation annealing is noticeably mitigated, and the pinning effect, which is believed to be caused by the Hf–Si interaction, can be less pronounced.

IV. Conclusion

This work presented a novel dual-metal gate technology for gating with Mo and $MoSi_x$. On the SiO_2 gate dielectric, Mo−$MoSi_x$ combination can be appropriate not only for devices with advanced transistor structures but also for conventional bulk devices if arsenic preimplantation is adopted. The thermal stabilities of pure Mo and $MoSi_x$ on SiO_2 were also evaluated to be higher than 950 °C. The effective Φ_m of pure Mo or $MoSi_x$ gate on HfO_2 is found to be slightly lower than that on SiO_2. Nevertheless, the difference between Φ_m of Mo and that of undoped $MoSi_x$ is independent of the underlying gate-dielectric material. Arsenic preimplantation still affects the modulation of the Φ_m of the metal silicide on HfO_2, even though the modulation range is slightly smaller than that on SiO_2.

Acknowledgment

The authors would like to thank the UC Berkeley Device Group for the use of QMCV simulator.

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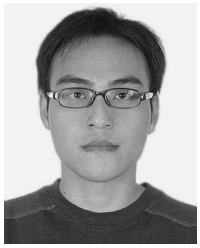

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