HfAlON n-MOSFETs Incorporating Low-Work Function Gate Using Ytterbium Silicide

C. H. Wu, B. F. Hung, Albert Chin, *Senior Member, IEEE*, S. J. Wang, F. Y. Yen, Y. T. Hou, Y. Jin, H. J. Tao, S. C. Chen, and M. S. Liang, *Fellow, IEEE*

***Abstract*—The authors have fabricated low-temperature fully silicided $YbSi_{2-x}$-gated n-MOSFETs that used an HfAlON gate dielectric with a 1.7-nm EOT. After a 600 °C rapid thermal annealing, these devices displayed an effective work function of 4.1 eV and a peak electron mobility of 180 $cm^2/V \cdot s$. They have additional merit of a process compatible with current very large scale integration fabrication lines.**

***Index Terms*—HfAlON, MOSFET, YbSi.**

I. Introduction

METAL-GATE/HIGH-κ is needed for highly scaled CMOS [1]–[11]. Unfortunately, the Fermi-level pinning causes the undesired large threshold voltage (V_t) in MOSFETs. Although high-κ n-MOSFET using TaC has shown low effective work function $(\phi_{m,\text{eff}})$ [1], [2], work is still needed to develop full silicidation (FUSI) gated high-κ n-MOSFET [3]–[5], [8]–[11] and deal with the $\phi_{m,\text{eff}}$ reduction. This is because of the process compatibility with current poly-Si gate CMOS technology. In this letter, we have used $YbSi_{2-x}$ FUSI-gate for high-κ n-MOSFETs. The Yb has the lowest work function in Lanthanide that previously gave $YbSi_{2-x}$ low-electron barrier to Si contact *with good uniformity* [12]. However, the $YbSi_{2-x}/HfO_2$ showed large leakage current and failed. To overcome this problem, we have used the robust HfAlON by combining high-diffusion-barrier Al_2O_3 and oxynitride [13]–[16] with HfO_2. The $YbSi_{2-x}$/HfAlON showed good low $\phi_{m,\text{eff}}$ of 4.1 eV and electron mobility of 180 $cm^2/V \cdot s$, indicating the potential application for metal-gate/high-κ n-MOSFETs.

II. Experimental Procedure

Standard p-type Si wafers, with a resistivity of 1–10 $\Omega \cdot$ cm ($10^{15}-10^{16}$ cm^{-3} doping level), were used in this letter. A nonself-aligned MOSFET [9] was fabricated to study the effect of FUSI gate on high-κ HfAlON. After device isolation and active area definition, the n^+ source-drain regions are formed first by using a thick dummy SiO_2 gate and phosphorus ion implantation at 35 KeV. After removing the dummy gate by patterning, the HfAlON high-κ gate dielectric was formed on Si wafer by depositing HfAlO using physical vapor deposition (PVD), a postdeposition anneal (PDA), NH_3 plasma surface nitridation and followed a second 800 °C PDA. Subsequently, the $\sim$ 25-nm amorphous Si was deposited and annealed at 950 °C rapid thermal annealing (RTA) for 30 s to activate the implanted dopant. The silicide was formed by depositing 60-nm Yb using PVD and 20-nm Mo using PVD, patterned and silicided at 400 °C–600 °C RTA for 30 s [9]–[11]. Here, the Mo is needed to cover the Yb and prevent oxidation during RTA silicidation. From the secondary ion mass spectroscopy (SIMS) and cross-sectional TEM measurements, little Mo can diffuse into the FUSI/high-κ interface and thus no effect on work function. For comparison, we also fabricated Al-, Yb-, or NiSi-gated devices on HfAlON, where the Al or Yb was directly deposited on HfAlON without silicidation thermal cycle. The fabricated n-MOS devices were characterized by capacitance–voltage (C–V) and current–voltage (I–V) measurements.

III. Results and Discussion

Fig. 1(a) and (b) shows the C–V and J–V characteristics for $YbSi_{2-x}$/HfAlON, Yb/HfAlON, NiSi/HfAlON, and control Al/HfAlON capacitors, annealed at different RTA temperatures. The Al-gated capacitor was used as a reference, since the pure metal displays little Fermi-level pinning on high-κ dielectrics due to the low-temperature process with less interface reaction [6], [7]. The shift of the C–V curves with different gate electrodes is due to the different work functions since the relative low-temperature silicidation thermal cycle has less effect on high-κ dielectric. However, the $YbSi_{2-x}/HfO_2$ device failed, which may be due to the Yb diffusion into HfO_2 and/or reaction of amorphous-Si with HfO_2. Using the robust HfAlON, the thermal stability was improved with a reasonable leakage current of 2.3×10^{-4} A/cm at -1 V with an equivalent oxide thickness (EOT) of $\sim$ 1.7 nm. The decreasing flat-band voltage (V_{fb}) with increasing RTA silicidation temperature for $YbSi_{2-x}$/HfAlON capacitors may be due to increased Yb diffusion toward the HfAlON surface, increasing the work function. From the C–V shift referenced to the Al control gate, the extracted $\phi_{m,\text{eff}}$ of $YbSi_{2-x}$/HfAlON and Yb/HfAlON are 4.1 and 3.6 eV, respectively. Therefore, much improved Fermi-level pinning is obtained. We also measured the C–V in the

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C. H. Wu and S. J. Wang are with the Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan, R.O.C.

B. F. Hung and A. Chin are with the Department of Electronics Engineering, National Chiao-Tung University, University System of Taiwan, Hsinchu, Taiwan, R.O.C. (e-mail: achin@cc.nctu.edu.tw).

F. Y. Yen, Y. T. Hou, Y. Jin, H. J. Tao, S. C. Chen, and M. S. Liang are with the Taiwan Semiconductor Manufacturing Corporation, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C.

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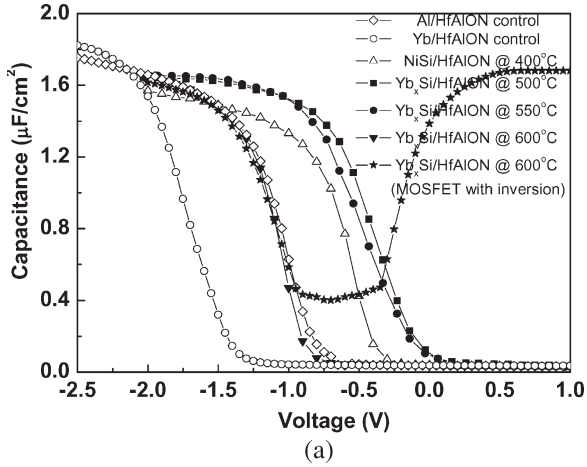
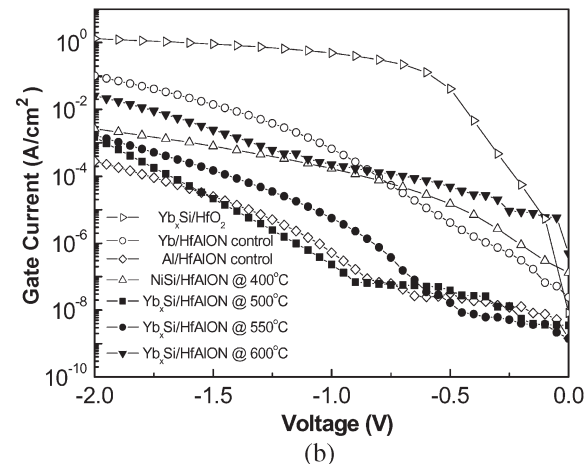


(a)



(b)

Fig. 1. (a) C–V and (b) $J_g - V_g$ characteristics for $YbSi_{2-x}$/HfAlON, Yb/HfAlON, Ni/HfAlON, and Al/HfAlON capacitors, measured under accumulation. The device area was 100 μm $\times$ 100 μm.

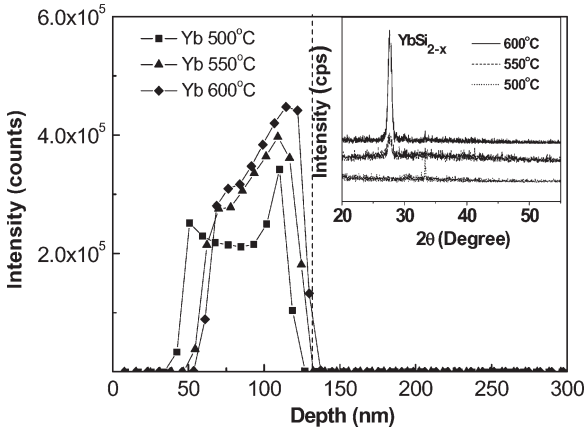


Fig. 2. SIMS of Yb in the $YbSi_{2-x}$/HfAlON structure. The inset figure is the XRD profiles.

MOSFET [9] and the same value of accumulation and inversion capacitance indicates the bottom surface of Si gate is silicided after 600 °C RTA without depletion. Thus, reasonable low $\phi_{m,\text{eff}}$ of 4.1 eV and a low gate-dielectric leakage current can be simultaneously achieved in $YbSi_{2-x}$/HfAlON MOS capacitors.

To further understand the desired negative shift of V_{fb} with increasing RTA temperature, we have down SIMS measure-

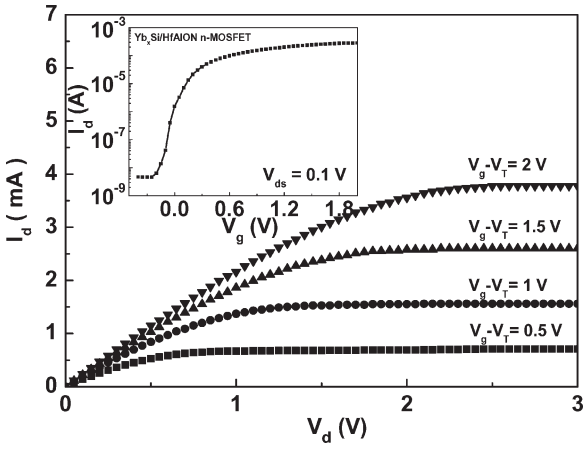
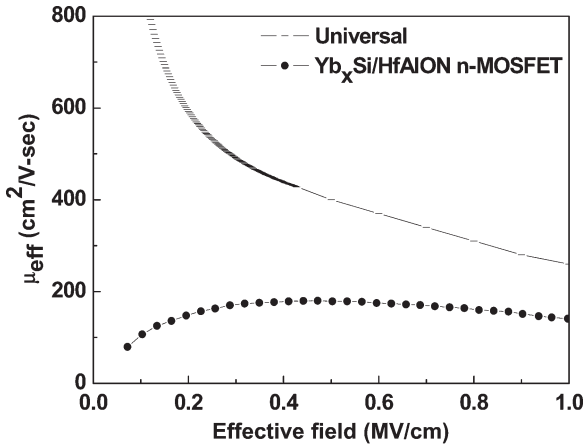
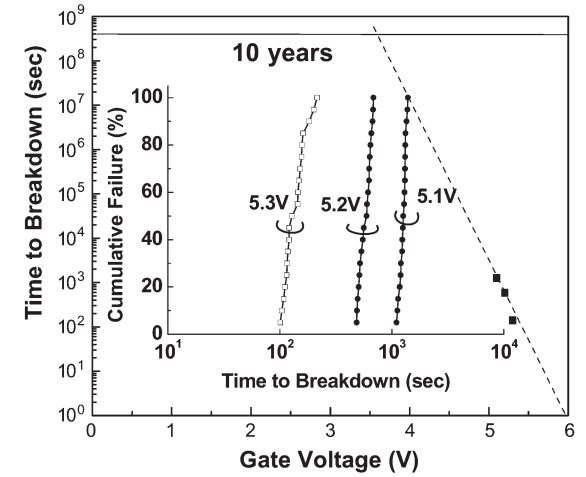


Fig. 3. I_d–V_d characteristics of an $YbSi_{2-x}$/HfAlON n-MOSFET. The inset figure is I_d–V_g curves. The gate length was 10 μm.



(a)



(b)

Fig. 4. (a) Electron mobility extracted from the I_d–V_d characteristics of an $YbSi_{2-x}$/HfAlON n-MOSFET and (b) the time-to-breakdown distribution and maximum operation voltage plots.

ments. As shown in Fig. 2, continuous diffusion of Yb toward interface was measured by $YbSi_{2-x}$ formation from X-ray diffraction (XRD) pattern (inset) [12], [17]. Here, the x is ~ 0.2 due to Si vacancy in silicide [17]. Such metal at interface is

known to unpin the Fermi level due to the high concentration of electrons in the metals [6], [7].

Fig. 3 displays the transistor I_d-V_d characteristics as a function of $V_g - V_t$ for 600 °C RTA annealed, $YbSi_{2-x}/HfAlON$ n-MOSFETs. The well-behaved I_d-V_d curves showed little degradation of the device performance from using an $YbSi_{2-x}$ gate. The inset figure is the I_d-V_g characteristics. A V_t as low as 0.1 V was obtained from the linear I_d-V_g plot, which is consistent with the large $\phi_{m,\text{eff}}$ of 4.1 eV from the C–V curves. Fig. 4(a) shows the electron mobility extracted from the measured I_d-V_g curves of the n-MOSFETs. A peak electron mobility of 180 $\text{cm}^2/\text{V}\cdot\text{s}$ was obtained for the $YbSi_{2-x}/HfAlON$ n-MOSFETs. Further mobility improvement to recently published data [18], [19] may be reachable by using HfSiON and/or forming gas anneal. Fig. 4(b) is the dielectric time-to-breakdown plot. Good reliability of large extrapolated voltage of 3.5 V is obtained for a ten-year operation.

IV. Conclusion

Good device performance has been demonstrated for long channel $YbSi_{2-x}/HfAlON$ n-MOSFETs with low $\phi_{m,\text{eff}}$ and V_t values. This promising n-MOS device has the merit of process compatibility with existing VLSI lines.

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