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A novel method to improve VCSELs oxide-confined aperture uniformity using selective As$^+$-implanted underlying layer

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Abstract

We report the utilization of an selective As$^+$-implanted underlying layer and regrowth method to enhance and control the wet thermal oxidation rate for 850 nm oxide-confined VCSEL. The oxidation rate of the As$^+$-implanted device showed a four-fold increase over the non-implanted one at the As$^+$ dosage of 1×10^{16} cm^{-3} and the oxidation temperature of 400 °C. The 50 side-by-side As$^+$-implanted oxide-confined VCSELs fabricated using the method achieved very uniform performance with a deviation in threshold current of $\Delta I_{th} \sim 0.2$ mA and slope-efficiency of ΔS.E. $\sim 3\%$. Finally, we accumulated life test data for oxide-confined VCSELs with As$^+$-implanted underlying layer up to 1000 h at 80 °C/15 mA.

Keywords: As$^+$-implanted; Oxide-confined; VCSEL; Wet-thermal oxidation

1. Introduction

Vertical-cavity surface-emitting lasers (VCSELs) have emerged as the attractive light sources for various optoelectronic applications such as optical communications, which offer several advantages over edge-emitting semiconductor lasers, such as low divergence circular beam, low threshold current, the possibility of one- and two-dimensional array formation, and cost-effective wafer-scale fabrication, etc. Over the past few years, the oxide-confined VCSELs have been shown to exhibit excellent performances such as low threshold current, high wall-plug efficiency, and high frequency modulation capability [1]. Up to now, the optical-confinement method commonly used for the VCSEL is the selective wet-oxidation of AlGaAs layers with desired oxidized aperture circulating around the VCSEL [2–4]. Various reports have reported about the control of wet thermal oxidation rate [5–8]. However, such a thermal oxidation process has a relatively slow oxidation rate, which is also difficult to control and to achieve uniformity for large area wafer. To overcome, Reese et al. [5] used the low-temperature-grown GaAs (LT-GaAs) layer below the oxidation layer to enhance wet thermal oxidation rate, while a maximum oxidation rate of 1.4 μm min^{-1} was achieved. The gallium vacancy (V_{Ga}) defects left in LT-GaAs after annealing was considered to be responsible for the acceleration of the oxidation rate. However, the V_{Ga} density in the LT-GaAs is difficult to be precisely controlled due to the uncertainty in growth temperature of the LT-GaAs (well below the system limit). In addition, the poor quality of the LT-GaAs material could affect the device reliability, and thus degrade the device uniformity of VCSELs. In addition, Yoshikawa et al. [7] demonstrated a self-stopping selective-oxidation process to control the oxide aperture, providing a controlled oxide aperture as small as about 3 μm in diameter. Chavarkar et al. [8] studied the effect of antimony (Sb) composition on the oxidation mechanism of $AlAs_{1-x}Sb_x$ ($x < 0.21$) layers grown on GaAs substrate.

Recently, we have also demonstrated an alternative arsenic-rich GaAs material using arsenic-ion implanting technique, which exhibits almost identical properties to the LT-GaAs layer [5–7]. The advantages for preparation of arsenic-rich GaAs layer by ion-implantation is its flexibility in controlling the arsenic excess density and the associated arsenic anti-site defect concentration by adjusting the implanting dosage [9]. Subpicosecond carrier lifetimes and

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picosecond photoconductive responses of GaAs:As^+ comparable to that of LT-GaAs were also reported [10]. After annealing, the dense As precipitates within the implanted region introduces highly resistive electrical and ultra fast optoelectronic properties [11]. These make the GaAs:As^+ a best candidate for electric-buffer layer with extremely low leakage current. In this paper, we report the use of selective As^+-implanted buffer layer to enhance the oxidation rate of an AlGaAs layer grown upon the buffer layer. The mechanism for oxidation rate acceleration and aperture control of the AlGaAs layer grown on the As^+-implanted buffer layer is interpreted. An array of 1×50 (1-dimensional) and die size of $250\,\mu m \times 350\,\mu m$ VCSELs fabricated with an oxidized AlGaAs layer of accelerated oxidation rate have shown to achieve uniform performances. Finally, the lifetime test of the oxide-confined VCSELs with As^+-implanted underlying layer is presented.

2. Device structure and fabrication

The cross-sectional schematic of As^+-implanted oxide-confined VCSEL is shown in Fig. 1. The VCSEL epitaxial layers were grown on n^+-type GaAs (1 0 0) 6° off toward with orientation of (1 1 0) substrate by metal organic chemical vapor deposition (MOCVD) system. The bottom distributed Bragg reflector (DBR) consists of 35-pairs of quarter wavelength-thick n-type (Si-doped) $Al_{0.9}Ga_{0.1}As/Al_{0.15}Ga_{0.85}As$. The active region has three GaAs/AlGaAs quantum wells with peak gain at 850 nm. Afterwards, a partial top DBR structure with three pairs of p-type (C-doped) $Al_{0.9}Ga_{0.1}As/Al_{0.15}Ga_{0.85}As$ was grown for As^+-implantation. The aperture of As^+-implantation is $13\,\mu m \times 13\,\mu m$, the dosage of As^+ is varied from 1×10^{15} to $2 \times 10^{16}\,cm^{-3}$, and the implanted energy is 100 KeV. After implantation, the sample was annealed at 700 °C for 2 h. Subsequently, 22 pairs of p-type (C-doped) $Al_{0.9}Ga_{0.1}As/Al_{0.15}Ga_{0.85}As$ DBR structures with an oxidation layer of 30 nm $Al_{0.98}Ga_{0.02}As$ were grown upon the As^+-implanted AlGaAs layer. For comparison, a similar VCSEL wafer structure without As^+ implanted buffer layer was also grown by MOCVD. Both MOCVD grown wafers with different structures were patterned by lithography

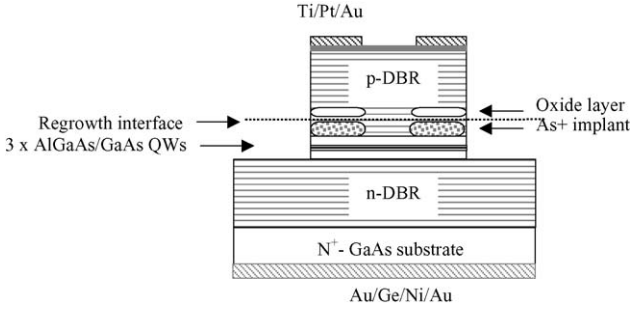

Fig. 1. The schematic of As^+-implanted oxide-confined GaAs VCSEL.

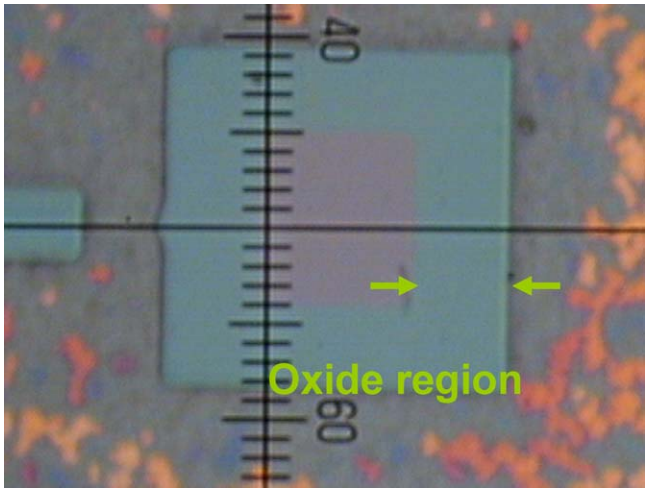

Fig. 2. Nomarski microscopic photograph of the VCSEL containing oxided $Al_{0.98}Ga_{0.02}As$ layer after oxidation for 45 min.

and were mesa-etched down to n-DBR layer. Later on, both samples were oxidized in a N_2/H_2O atmosphere at various temperatures with an oxidation aperture of $13\,\mu m \times 13\,\mu m$. Finally, the p-type metal (Ti/Pt/Au) with a window aperture is $21\,\mu m \times 21\,\mu m$ and the n-type metal (Au/Ge/Ni/Au) contacts were deposited and annealed sequentially. The lateral oxidation of width (from the test mesa) of the $Al_{0.98}Ga_{0.02}As$ layer grown upon the As^+-implanted, three periods of p-type $Al_{0.9}Ga_{0.1}As/Al_{0.15}Ga_{0.85}As$ layers is determined using Nomarski microscopic photograph. It is seen that the color and the size of the region containing oxided $Al_{0.98}Ga_{0.02}As$ layer are significantly changed after oxidation for 45 min, as shown in Fig. 2.

3. Results and discussions

The relationship between the oxidation rate at 400 °C and the As^+ implantation dosages is depicted in Fig. 3.

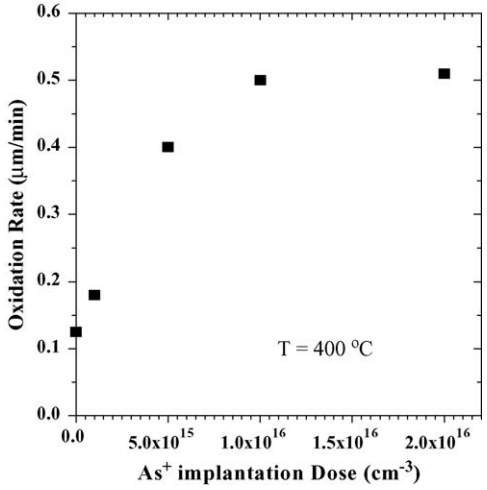

Fig. 3. Relationship between the As^+-implanted dose and the oxidation rate.

The oxidation rate shows a rapid increasing trend with the As^+ dose, however, which is found to saturate at the dose beyond $1 \times 10^{16}\,cm^{-3}$. The oxidation rate at the dosage higher than $1 \times 10^{16}\,cm^{-3}$ saturates at a constant rate of about $0.5\,\mu m\,min^{-1}$. Such an improvement in oxidation rate of the AlGaAs layer is mainly attributed to the enhancement in the removal of the products of the oxidation reaction. This eventually leads to the accelerated oxidation of AlGaAs layer and the improved oxide–GaAs interface quality. Since the faster oxidation rate of the AlGaAs layer is strongly correlated with the V_{Ga} density in the As^+-implanted layer [12], a further enhancement of oxidation speed due to the increasing of the defect density at higher implanted doses is thus expected. Therefore, we have established a saturation of these defects at implanting dose beyond 10^{16} ions cm^{-2}.

The oxidation depth versus oxidation time for the VCSEL samples with As^+-implantation of $2 \times 10^{16}\,cm^{-3}$ and without implantation is shown Fig. 4. By measuring the oxidation depth from Nomarsky microscope photograph, most of the data at two different oxidation temperatures show approximately linear dependency. Nonetheless, the VCSEL sample with underlying As^+-implanted layer exhibits a saturated oxidation depth beyond 40 μm after oxidizing at 420 °C. Such a saturation in oxidation rate has indicated a diffusion-limited oxidation phenomenon [5]. After oxidizing at temperature of 400 °C for 120 min, the lateral depths of the oxidized AlGaAs layer are 60 and 15 μm for the VCSEL samples with and without As^+-implanted underlying layer, respectively. This corresponds to a four-fold increase in oxidation rate of the VCSEL with As^+-implanted underlying AlGaAs layer as compared to that of the non-implanted one.

Fig. 5 shows the power–current (*L–I*) curves of 50 units of side-by-side VCSELs fabricated using the As^+-implantation assistant wet-selective oxidation process. The dosage and energy of As^+ implantation were $1 \times 10^{16}\,cm^{-3}$ and 100 KeV, respectively. The oxidation temperature and time were 400 °C and 40 min. At the driving current of 20 mA, the average output power is about 5.5 mW, the threshold current of the VCSEL is 1.2 mA, and the slope efficiency (S.E.) is 34%. The variation of threshold current and S.E. are only 0.2 mA and 3%, respectively. These results indicate that the VCSELs with As^+-implanted underlying layer have a better control on the oxidation depth and aperture, which results in the VCSELs with nearly identical performances. Since the As^+-implanted region has a faster oxidation rate than the non-implanted region, when the oxidation proceeds close the designed aperture (non-implanted region), the oxidation rate will significantly reduces and hence the tolerance of oxidation time can be released. This essentially reduces the processing failures occurring during oxidation and greatly improves the uniformity performance of the VCSELs. With the adding of underlying AlGaAs:As^+ layer, the increase in production yield and reduction in the fabrication cost of the VCSELs are straightforward.

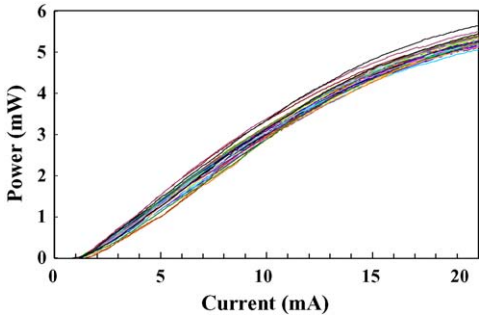

Fig. 5. *L–I* curves of 50 side-by-side As+ implanted oxide-confined GaAs VCSELs.

To guarantee the VCSELs reliability is a very important issue for many practical applications especially the addition of underlying AlGaAs:As^+ layer. Fig. 6 shows the lifetime data of As^+-implanted oxide-confined GaAs VCSELs. We have accumulated life test data of our VCSELs up to 1000 h at

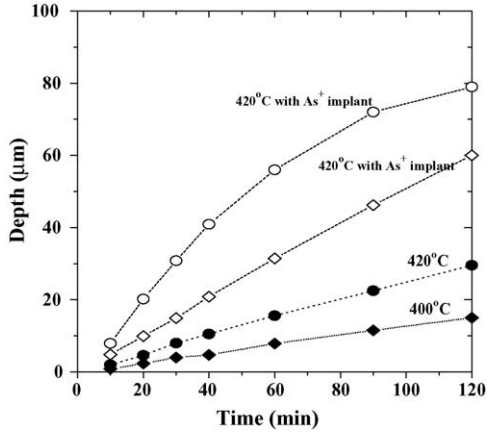

Fig. 4. The oxidation depth vs. the oxidation time at 400 and 420 °C. The open markers and solid markers represent the samples with and without As^+-implanted, respectively.

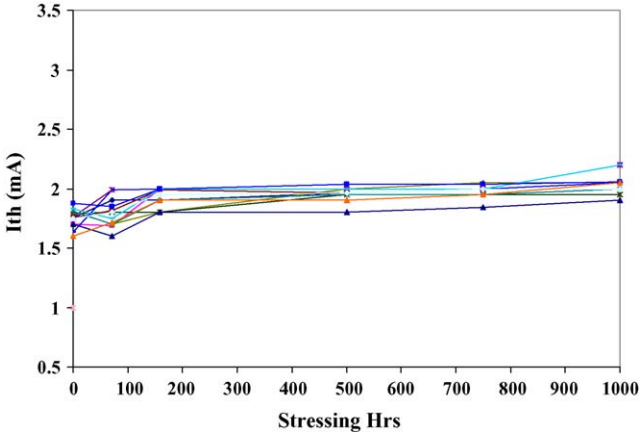

Fig. 6. Lifetime test of As^+-implanted oxide-confined GaAs VCSELs at 80 °C/15 mA.

80 °C/15 mA with exceptional reliability. The results suggest that the VCSELs with As^+-implanted underlying layer have a better control on the oxidation depth and aperture as well as reliable performance.

4. Conclusion

By adding an As^+-implanted underlying AlGaAs layer and using the MOCVD regrowth method, we have successfully demonstrated the enhancement and precise control the wet thermal oxidation rate of the AlGaAs layer in the 850 nm oxide-confined VCSEL. With the As^+ dosage of $1 \times 10^{16}\,cm^{-3}$ and the oxidation temperature of 400 °C, our results reveal that the oxidation rate of the VCSELs with As^+-implanted underlying layer have a four-fold increase on the oxidation rate over the non-implanted one. The testing on 50 units of side-by-side As^+-implanted and oxide-confined VCSELs fabricated using the method shows high uniformity in their overall performances. The deviations in threshold current and slope-efficiency of these VCSELs are $\Delta I_{th}/I_{th} \sim 16\%$ (standard deviation ∼0.07) and ΔS.E. ∼ 3%. The application of As^+-implanting technique in fabrication of the large-area and reliable VCSEL array has been demonstrated. The lifetime test data of As^+-implanted oxide-confined GaAs VCSELs up to 1000 h at 80 °C/15 mA with exceptional reliability.

Acknowledgment

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