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Trench gap-filling copper by ion beam sputter deposition

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Abstract

The ion beam sputter deposition (IBSD) and electroless plating techniques have been combined to achieve the precipitation of Cu onto an amorphous (a)-TaN diffusion barrier layer in order to accomplish the ultralarge-scale-integrated interconnect metallization. The copper-filled specimens were annealed at various temperatures in a reduced atmosphere. The preferred orientation was analyzed by X-ray diffraction, and field emission scanning electron microscopy was used to elucidate the growth mechanism of the trench-filled electroless deposited Cu film on the Cu seeded layer by IBSD. The Cu(1 1 1) texture was strengthened by annealing at 300 °C for 1 h. The surface roughness increased notably with increasing annealing temperature. The electrical resistivity of the as-deposited copper film (3.05 μΩ cm) decreased with increasing annealing temperature. The major contribution of this study is to successfully combine the techniques of IBSD and electroless plating for the Cu gap-filling of submicron trenches with an excellent step coverage.

Keywords: Ion beam sputter deposition; Annealing; Gap-filling; Trench

1. Introduction

Electro-deposition of metals has wide applications in microelectronic packaging and printed circuit board. Copper has recently been proposed as the most reliable interconnecting material to replace aluminum because of its significant advantages of lower electrical resistivity and power dissipation, and high resistance to electro-migration during the fabrication of ultralarge-scale-integrated devices [1]. The most promising copper deposition technologies are chemical vapor deposition and electroless plating techniques, and both are successful in depositing good quality films. Copper electroless plating benefits from its low tool cost and low-temperature process compared with the other [2–5]. In the process of electroless plating, it is necessary to activate the surface of the specimens in a solution of $PdCl_2$ and $SnCl_2$ as activators [6–8]. However, if a trace of chloride ions remains in the Cu interconnects, corrosion reactions would occur and, therefore, failure can result.

The objective of this work was to overcome such shortcomings through the establishment of an ion beam sputtering deposition (IBSD) [9] system as the Cu seeding techniques for the subsequent electroless plating of copper on the silicon wafer. The related properties and microstructures of the deposited copper thin film are influenced by this process for the copper metallization of ultralarge-scale-integrated interconnect, and will be analyzed.

2. Experimental details

The substrates were 8-in. p-type (1 0 0) silicon wafers on which 1.2 μm thick fluorosilicate glass film was deposited by chemical vapor deposition as a dielectric interlayer with a low dielectric constant. Both patterned and non-patterned wafers deposited the fluorosilicate glass film were used to grow amorphous (a)-TaN as an adhesion and a diffusion barrier layer by ionized metal plasma. The Cu catalyst layer

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Table 1
Chemical composition of the electroless Cu plating solution employed in this study

Solution constituent	Concentration range (g^{-1})
$CuSO_4 \cdot 5H_2O$	6–10
EDTA	25–35
TMAH	100–140
PEG	0.5–1.5
2,2′-Bipyridine	0.1–1.2
HCHO (37%)	6–10

was prepared by IBSD. The deposition chamber was pumped down to a base pressure of 2×10^{-6} torr prior to the deposition. A 3 cm Kaufmann-type ion source was used to sputter the copper target with Ar^+. The ion beam voltage, sputter rate and deposition time were 700 V, 0.01–0.03 nm s^{-1} and 30 min, respectively.

Cu as seeds by IBSD were then put into the Cu electroless plating bath for Cu plating, whose chemical composition is listed in Table 1. The bath temperature was kept in the range 50–60 °C, and the solution pH value ranged from 12 to 13. The chemistry of the electroless plated Cu used in this study was the redox reactions between Cu–(EDTA) complex ions and formaldehyde [10]. The cathodic reduction occurred in several steps whose final products were Cu and $EDTA^{4-}$. The electrons were supplied by the oxidation of formaldehyde in a very basic solution, using methyl-ammonium-hydroxide (TMAH) to control the bath pH. 2,2′-Bipyridine, as a stabilizer, could trap Cu^+ ions to prevent Cu deposition in the plating solution and polyethyleneglycol (PEG) was added as a surfactant to reduce the surface tension of the specimens, thereby inhibiting the formation of the hydrogen gas bubble on the Cu surface. The thickness of electroless plated Cu films on the wafer was about 0.8 μm.

The specimens were annealed in a tube furnace with an atmosphere of 90% nitrogen and 10% hydrogen mixed gases for preventing the surface oxidation at temperatures varying from 100 to 500 °C for 1 h. The cross-sectional microstructures of the patterned wafer were examined by field emission scanning electron microscopy (FESEM). The crystallinity of the electroless plated Cu on the sample was analyzed by X-ray diffraction (XRD). The surface topography of the formed film was examined by atomic force microscopy (AFM), which measures the root mean square roughness (R_{rms}) in a square area of 1 μm. The same vertical scale was chosen for all the specimens for comparison. The sheet electrical resistivity was measured by a four-point probe method.

3. Results and discussion

Fig. 1a shows a FESEM cross-section image of trenches without Cu seeding by IBSD. The width of the trench is 0.5 μm and the aspect ratio is 2. Fig. 1b shows the result of Cu seeding by IBSD; a copper film is effectively formed inside the trenches in comparison with Fig. 1a. The Cu seeded

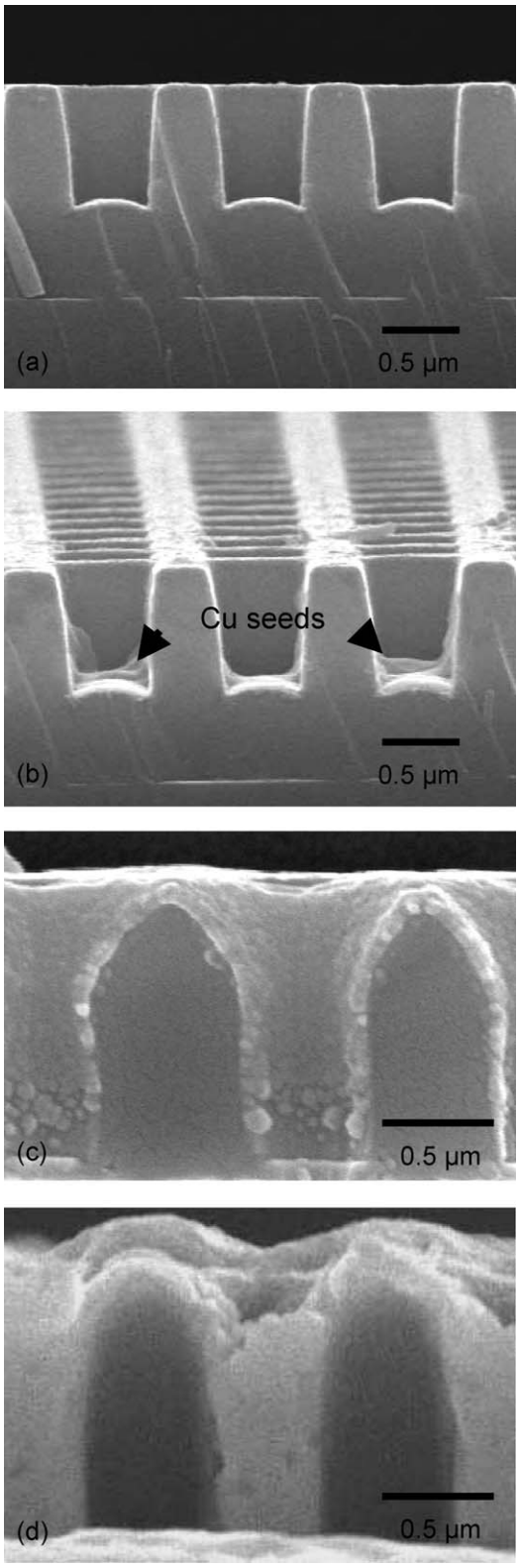

Fig. 1. FESEM cross-section view of the trenches. (a) Before gap-filling, gap width: 0.5 μm, aspect ratio: 2, (b) Cu as seeds by IBSD for gap-filling, (c) Cu electroless plating for gap-filling of the trenches and (d) quality of the gap-filling.

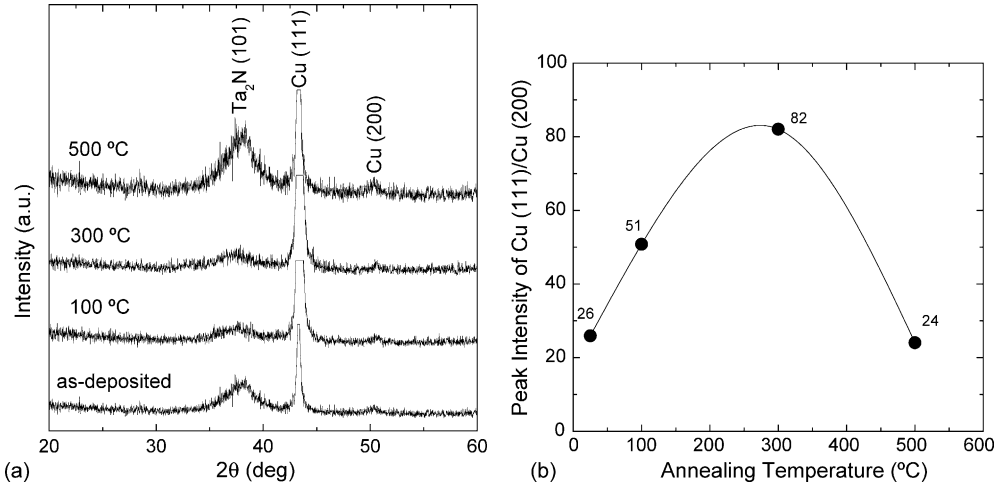

Fig. 2. Cu electroless plating on (IBSD Cu seeds)/a-TaN as a function of annealing temperature: (a) XRD patterns and (b) variation of the peak intensity ratio Cu(1 1 1)/Cu(2 0 0); diffraction angle $2\theta = 43.3^\circ$ for Cu(1 1 1) and $2\theta = 50.4^\circ$ for Cu(2 0 0).

a-TaN is the substrate, on which electroless Cu reactions initiate a process of autocatalytic nucleation and growth. Fig. 1c shows an image of the appropriate quality for gap-filling of the submicron trenches, resulting from Cu seeding by IBSD, followed by Cu electroless plating. Furthermore, the appropriate quality for gap-filling is shown in Fig. 1d.

Fig. 2a shows the XRD patterns obtained for the assembly of Cu/(IBSD seeded Cu)/a-TaN/Si without annealing and with annealing at 100, 300 and 500 °C. From the normalized peak heights, it was found that the as-deposited Cu film mainly manifests the Cu(1 1 1) preferred orientation. The peak height ratio of Cu(1 1 1)/Cu(2 0 0) as given by in the Joint Committee on Powder Diffraction Standards (JCPDS) [11] card is near 2.17. As shown in Fig. 2b, the peak height ratio value of Cu(1 1 1)/Cu(2 0 0) increases at annealing temperatures >300 °C. Since the most close-packed plane

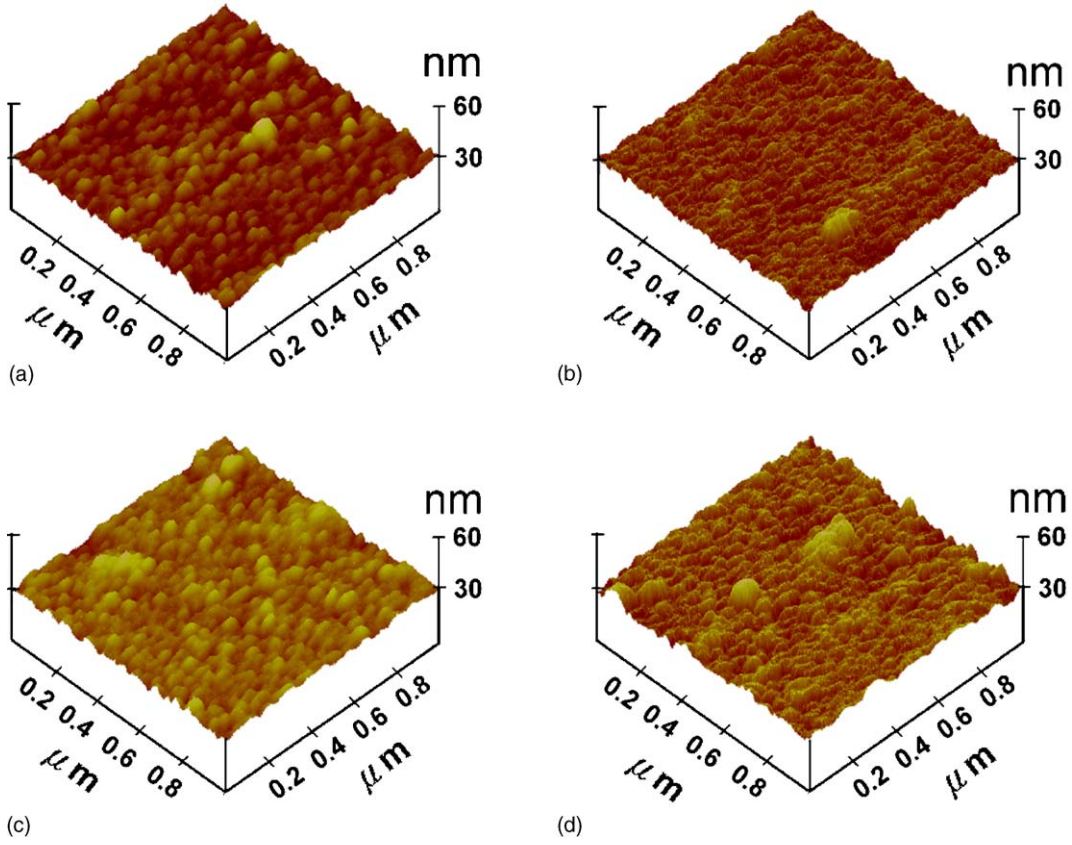

Fig. 3. Variation of the AFM surface morphology as a function of annealing temperature: (a) as-deposited, (b) 100 °C, (c) 300 °C and (d) 500 °C.

Cu(1 1 1) is the preferred orientation in this study, it can be concluded that the overall energy of the Cu/(IBSD seeded Cu)/a-Ta:N/Si assembly tends to be minimized through the predominance of the (1 1 1) plane which has a lower surface energy than the (2 0 0) plane [12]. The maximum of the Cu(1 1 1)/Cu(2 0 0) peak ratio is 82 for the specimen annealed at 300 °C, but the peak ratio decrease to 24 as temperature further increases to 500 °C, indicating that the strong Cu(1 1 1) texture has been reduced at >300 °C. It could be the strong Ta_2N(1 0 1) peak for the specimen annealed at 500 °C that reduces the Cu(1 1 1)/Cu(2 0 0) peak ratio. Higher annealing temperatures (>500 °C) are required to elucidate the phenomenon. The strong Cu(1 1 1) preferred orientation after annealing at 300 °C is, after all, significant in this research.

Fig. 3a–d shows distinct AFM images of the surface topography acquired at different annealing temperatures. The surface of the annealed specimen is rougher than that of the as-deposited sample. For instance, the surface morphology is strongly affected by the annealing temperature, as shown in Fig. 4, where the surface roughness is increased notably with increasing the annealing temperature. Films with higher R_{rms} resulting from the annealing show adverse effects on the continuity of the electroless deposited Cu, indicating that no necessity of higher annealing temperature, e.g., >300 °C in the metallization process is required.

The sheet resistivity as a function of annealing temperature is also shown in Fig. 4. The electrical resistivity of the as-deposited Cu film is 3.05 μΩ cm, it is decreased with increasing annealing temperature up to 2.02 μΩ cm at 500 °C. It is apparent that annealing promotes recovery and recrystallization of the as-deposited Cu film [13,14], which result in a decrease of the resistivity. For comparison, the resistivity of bulk Cu is 1.67 μΩ cm [15]. Cu seeding by IBSD for copper

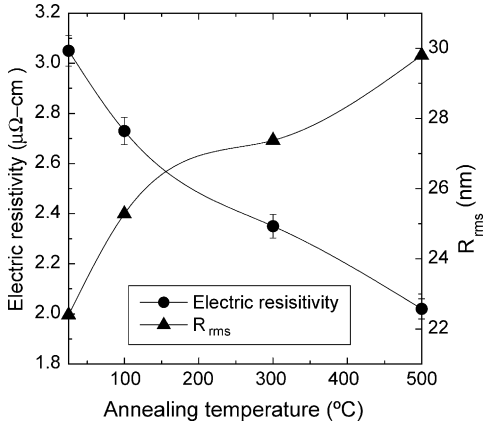

Fig. 4. Variation of the surface and sheet resistivity as a function of annealing temperature of the assembly using Cu seeds formed by IBSD.

electroless plating will invariably encounter the problem of the high electrical resistivity of ultralarge-scale-integration Cu interconnect metallizations in the future.

4. Conclusions

This study successfully combines the techniques of IBSD and electroless plating for Cu gap-filling. Based on the results, we can draw the following conclusions:

1. Cu seeding by IBSD, followed Cu electroless plating, has the ability to grow a film from the bottom toward the top of the trench, revealing an appropriate quality for gap-filling of submicron trenches with a high aspect ratio.
2. The peak height ratio of Cu(1 1 1)/Cu(2 0 0) increases at annealing temperatures ≦300 °C; a strong Cu(1 1 1) preferred orientation of the specimen annealed at 300 °C is significant in this research.
3. It is clear that the surface roughness increases notably with increasing annealing temperature.
4. The electrical resistivity of the as-deposited Cu film (3.05 μΩ cm) decreased with increasing annealing temperature to 2.02 μΩ cm at 500 °C.

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