Design and Anaylsis of A 2.5-Gbps Optical Receiver Analog Front-End in a 0.35-μm Digital CMOS Technology

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***Abstract*—This paper presents the design of an optical receiver analog front-end circuit capable of operating at 2.5 Gbit/s. Fabricated in a low-cost 0.35-μm digital CMOS process, this integrated circuit integrates both transimpedance amplifier and post limiting amplifier on a single chip. In order to facilitate high-speed operations in a low-cost CMOS technology, the receiver front-end has been designed utilizing several enhanced bandwidth techniques, including inductive peaking and current injection. Moreover, a power optimization methodology for a multistage wide band amplifier has been proposed. The measured input-referred noise of the optical receiver is about 0.8 $\mu A_{\rm rms}$. The input sensitivity of the receiver front-end is 16 μA for 2.5-Gbps operation with bit-error rate less than 10^{-12}, and the output swing is about 250 mV (single-ended). The front-end circuit drains a total current of 33 mA from a 3-V supply. Chip size is $1650\ \mu$m $\times$ $1500\ \mu$m.**

***Index Terms*—Active inductor, limiting amplifier (LA), transimpedance amplifier (TIA).**

I. Introduction

FIBER-OPTICAL networks have become a main stream for long haul and ultra high-speed data communications. The growing demands in broad-band access to internet, such as fiber to the home (FTTH), have motivated marvelous explorations of high performance optical transceivers recently [1]–[10]. This paper presents the design of a 2.5-Gbps optical receiver analog front-end (AFE) circuits in a low-cost 0.35-μm digital CMOS process [1]. With the progress of CMOS photo detector (PD) technology, integrating photo detector, transimpedance amplifier (TIA), and limiting amplifier (LA) on a single chip provides the feasibility of system integration in the future [9].

The architecture of the optical receiver AFE is shown in Fig. 1. The incoming nonreturn to zero (NRZ) optical signal is converted to a photo current by an external photo detector, and regenerated to a voltage signal suitable for clock-and-data recovery (CDR) by a TIA and an LA. Conventionally, the TIA converts the tiny photo current generated from a photo detector to a voltage signal of tens to hundreds millivolts, and couples it to a LA in the other package for post amplification. Since the TIA's output signal is still small, off-chip voltage coupling is susceptible to noise disturbance.

In this design, both the TIA and the LA are integrated in a single chip. Thus, TIA's output can be on chip dc-coupled to the LA, and no external coupling capacitor is required to minimize noise interference. Furthermore, data jitter induced by low cutoff frequency in ac-coupled scheme can be alleviated. For on-chip dc-coupling, an automatic dc level control circuit (ADC) is incorporated as TIA's output stage to adjust its output dc level to that of the post-LA's input dc level.

This paper is organized as follows. Section II describes the design of the TIA in the receiver. Several bandwidth enhancement techniques for CMOS TIA's have been utilized. Its noise performance is also analyzed and discussed. The design of LA is introduced in Section III. The LA is basically a cascaded amplifier chain. The gain-bandwidth performance and power optimization are investigated in detail. Section IV describes the experimental results. And finally, conclusions are drawn in Section V.

II. Transimpedance Amplifier

For CMOS TIAs, the primary factors that constrain signal bandwidth and noise performance are the inherent parasitic capacitance introduced by the photo detector and the bonding pad. Therefore, in a conventional common source TIA architecture, its signal bandwidth has to be severely compromised with conversion gain and noise performance [2]. In this design, a low input impedance TIA using regulated cascode input stage [3] with shunt-feedback configuration is utilized [4]. Fig. 2 depicts the circuit schematic of the TIA. The input impedance of the TIA is greatly reduced by the local feedback amplifier $(M4 + M5)$ and shunt-feedback. This prevents the input pole from dominating signal bandwidth, and the gain degradation caused by the input shunting capacitance can be avoided.

To further enhance signal bandwidth, inductive loads at each gain stage are also utilized to partially trim out the parasitic capacitance at the drain of M_1 and M_2 [4], [5]. Compared to using resistive loads, signal bandwidth is improved by 80% without gain peaking according to experimental results [4]. In this design, active inductors are employed instead of passive spiral inductors for the latter ones are in general bulky and contribute significant parasitic capacitance. The active inductors are made up of an nMOS and a resistor, and are configured as $M_6 + M_7$, $M_8 + M_9$, and $M_{11} + M_{12}$. The nMOS is operated in the saturation region, and the resistor is implemented using a pMOS operated in the triode region. Let C_{gs} and C_{gd} be the parasitic

Manuscript received December 20, 2004; revised April 28, 2005 and September 6, 2005. This work was supported by the National Science Foundation under Contract NSC-93-2220-E009-004, 93-EC-17-A-07-S1-001, by ITRI/STC, and by MediaTek Inc. This paper was recommended by Associate Editor K. Pedrotti.

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Digital Object Identifier 10.1109/TCSI.2005.862068

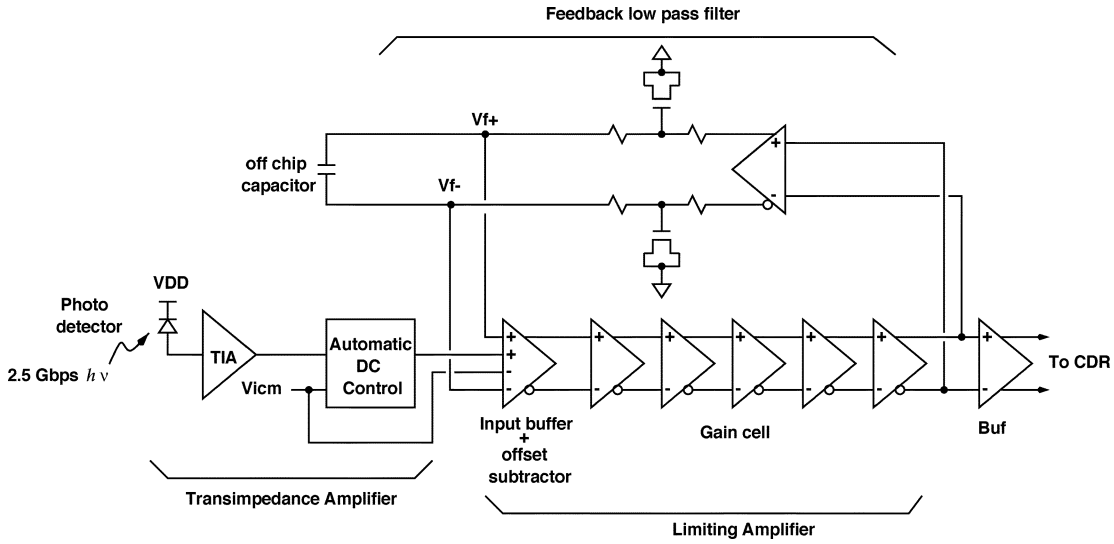

Fig. 1. Optical receiver AFE architecture.

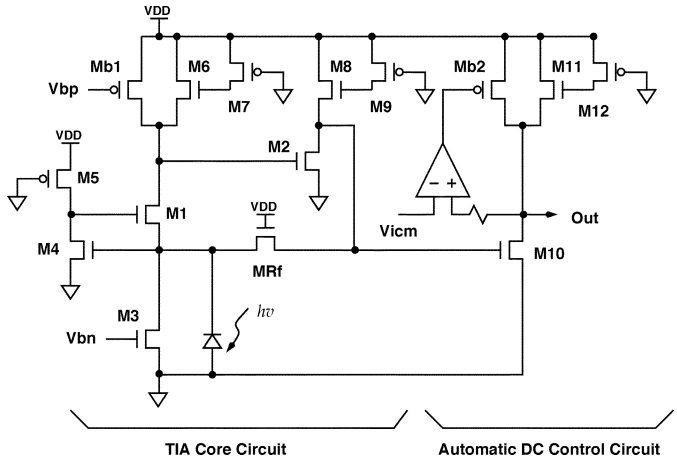

Fig. 2. TIA circuit schematic.

capacitance of M_6, M_8, M_{11}, M_7, M_9, and M_{12}, C_L be the loading capacitance at the source node of M_6, M_8, and M_{11}, g_m be the transconductance of M_6, M_8, M_{11}, and r_{ds} be the turn on resistance of M_7, M_9, and M_{12}. The input impedance looking into the active inductor can be expressed as Z_{in}, where (1), shown at the bottom of the page, is true, and

$$z_1 \approx \frac{1}{(C_{gsi}+C_{gdj}+C_{gdi})r_{dsj}} \tag{2}$$

$$p_1 \approx \frac{g_{mi}}{C_{gsi}+C_L+g_{mi}r_{dsj}(C_{gdj}+C_{gdi})} \tag{3}$$

$$p_2 \approx \frac{C_L+C_{gsi}+g_{mi}r_{dsj}(C_{gdj}+C_{gdi})}{[C_L(C_{gsi}+C_{gdj}+C_{gdi})+C_{gsi}(C_{gdj}+C_{gdi})]r_{dsj}} \tag{4}$$

$i = 6, 8, 11$ and $j = 7, 9, 12$.

The additional zero is introduced by the gate resistor r_{dsj}. For Z_{in} to behave as an inductor, i.e., $z_1 < p_1$, it is required that

$$g_{mi}r_{dsj} > 1 + \frac{C_L}{C_{gsi}}. \tag{5}$$

Under this condition, the active loads behave as inductors within the frequency range $z_1 < f < p_1$. In this case the open-loop bandwidth of the TIA dominated by the pole, p_1, can be alleviated by the active inductor.

Within the inductive region, Z_{in} can be modeled as an ideal inductor L in series with a passive resistor $R2$ and with another resistor $R1$ in parallel, as is shown in Fig. 3. Let g_{mL} be the transconductance of M_L, we have

$$R_1 \approx R_L \quad R_2 \approx \frac{1}{g_{mL}-\frac{1}{R_L}} \quad L \approx \frac{R_L(C_{gs}+C_x)}{g_{mL}-\frac{1}{R_L}}. \tag{6}$$

In order to increase the open-loop gain of the TIA, another current source $M_{bi}(i = 1, 2)$ is added in parallel to the active inductor. Since the tolerated input current level of the TIA is determined by I_{M3}, by the current injection technique, $1/g_{m6}$ can be increased without sacrificing the TIA's input dynamic range and degrading the input pole frequency. In addition, it mitigates dc drop of the active inductors. Thus, dual supplies are not required compared to the prior art in [5].

Assuming the equivalent impedances introduced by the active inductors (M_6, M_7, M_{b1}) and (M_8, M_9) are approximated by $X_{L1}+sL_1$ and $X_{L2}+sL_2$, and C_{tot1}, C_{tot2}, and C_{load} respectively represents the parasitic capacitance at the drain node

$$\begin{aligned} Z_{\text{in}} &= \frac{1}{g_{mi}} \times \frac{1+s(C_{gsi}+C_{gdj}+C_{gdi})r_{dsj}}{1+s\left[\frac{C_L+C_{gsi}+g_{mi}r_{dsj}(C_{gdj}+C_{gdi})}{g_{mi}}\right]+s^2\left[\frac{C_L(C_{gsi}+C_{gdj}+C_{gdi})+(C_{gdj}+C_{gdi})C_{gsi}}{g_{mi}}\right]r_{dsj}} \\ &\approx \frac{1}{g_{mi}} \times \frac{1+\frac{s}{z_1}}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)} \end{aligned} \tag{1}$$

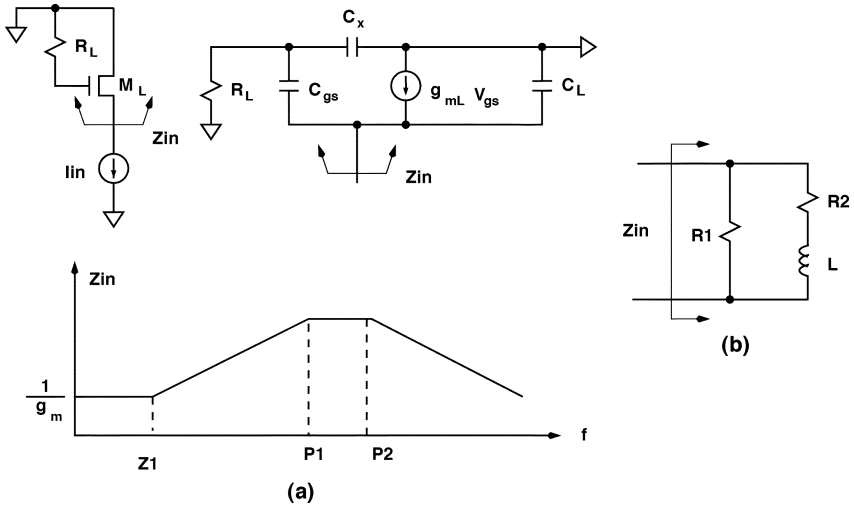

Fig. 3. Active inductor (MOS-L).

of M_3, M_1, and M_2, the open-loop gain, $T_{oz}(f)$, of the TIA can be approximated as

$$T_{oz}(f) \approx X_{L1} g_{m2} X_{L2} \times \frac{1}{1+\frac{s}{p_1}} \times \frac{1+\frac{s}{z_1}}{1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}} \times \frac{1+\frac{s}{z_2}}{1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}} \quad (7)$$

where

$$p_1 \approx \frac{(A+1)g_{m1}}{C_{\text{tot1}}} \quad A \approx \frac{g_{m4}}{g_{m5}} \quad (8)$$

$$z_1 = \frac{X_{L1}}{L_1} \quad \omega_1 = \frac{1}{\sqrt{L_1 C_{\text{tot2}}}} \quad Q_1 = \frac{1}{X_{L1}}\sqrt{\frac{L_1}{C_{\text{tot2}}}} \quad (9)$$

$$z_2 = \frac{X_{L2}}{L_2} \quad \omega_2 = \frac{1}{\sqrt{L_1 C_{\text{load}}}} \quad Q_2 = \frac{1}{X_{L2}}\sqrt{\frac{L_1}{C_{\text{load}}}}. \quad (10)$$

The closed-loop gain $T_{cz}(f)$ can be derived as

$$T_{cz}(f) = \frac{T_{oz}(f)}{1+g_{mR_f}T_{oz}(f)} \approx \frac{T_z \times \left(1+\frac{s}{z_1}\right)}{1+s\frac{g_{m2}X_{L2}+\frac{1}{Q_1\omega_1 g_{mR_f}}}{\frac{1}{g_{mR_f}}+X_{L1}g_{m2}X_{L_2}}+\frac{s^2}{\omega_1^2\left(X_{L1}g_{m2}X_{L2}g_{mR_f}+1\right)}} \quad (11)$$

where

$$T_z \approx \frac{1}{g_{mR_f}} \times \frac{1}{1+\frac{g_{m6}}{g_{mR_f}}\frac{g_{m8}}{g_{m2}}} \times \frac{g_{m10}}{g_{m12}} \approx \frac{1}{g_{mR_F}} \times \frac{g_{m10}}{g_{m12}}. \quad (12)$$

At critical damping, the −3-dB bandwidth of T_{cz} can be extended to $\omega_1\sqrt{1+X_{L1}g_{m2}X_{L2}g_{mR_f}}$ according to (11). In addition, another zero at z_1 is introduced by inductive peaking, which can be placed at the roll-off region of $T_{cz}(f)$ to further enhance bandwidth.

Both the inductive peaking and current injection techniques are also applied in the buffer stage, which is a common source gain stage comprised of $M_{10} - M_{12}$ and M_{b2}. In contrast to a source follower buffer stage, it provides a moderate gain at a relatively low power dissipation. The buffer stage also functions as an ADC, whose output common mode voltage is preset to the input common mode voltage (V_{icm}) of the LA by a local feedback loop. This ensures dc level tracking of the TIA and the LA despite of process and temperature variations. In this way, the sensitive signal paths can be on-chip directly coupled and no external coupling capacitor is required to avoid noise disturbance.

The price paid in the regulated cascode (RGC) input stage is the extra noise introduced by the RGC feedback amplifier. The input-referred noise can be derived as [6]

$$\overline{i_{eq}^2} = 4kT\gamma(g_{m3}+g_{mb1}+g_{m6})+4kT\gamma g_{mR_f} + \frac{4kT\gamma(g_{m2}+g_{m8})\left[\omega^2(C_{g2}+C_{d1})^2+g_{m6}^2\right]}{g_{m2}^2} + \frac{4kT\gamma(g_{m4}+g_{m5})}{(g_{m4}+g_{ds5})^2} \times \left[g_{ds3}^2+g_{mR_f}^2+\omega^2(C_{\text{in}}+C_{gs4})^2\right] \quad (13)$$

$$+ \frac{4kT\gamma(g_{m1}+g_{m6}+g_{mb1})\omega^2(C_{gs1}+C_{gd4})^2}{g_{m1}^2} \quad (14)$$

where γ is the noise factor of the MOSFETs, C_{in} is the parasitic capacitance at the input node, C_{g2} and C_{d1} respectively represent the total parasitic capacitance at the gate of $M2$ and the drain of $M1$. To mitigate this drawback, the transconductance of $M4$ is chosen to be as large as possible to reduce the input-referred noise coming from $M4$and $M5$'s thermal noise [6]. Additionally, the tail current source (I_{M_3}) needs to be sufficiently large to tolerate the input dynamic range.

III. Limiting Amplifier

Fig. 1 depicts the architecture of the LA, which is composed of a chain of gain cells, an offset cancellation circuit, a feedback low-pass filter, and a current mode output buffer to drive 50-Ω output loads.

A. Architecture

For a LA design, how to determine the number of gain stages with gain-bandwidth tradeoffs and power optimization is an im-

portant issue. Assuming each gain cell is identical and can be approximated by a two pole amplifier, then its conversion gain can be described by $A(s)$, where

$$A(s) = \frac{A_s \cdot \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{15}$$

Here, A_s denotes its small-signal dc gain, ζ is the corresponding damping factor, and ω_n is the natural frequency. Thus, the -3-dB bandwidth of a single-stage amplifier can be derived as ω_s, where

$$\omega_s = \left[1 - 2\zeta^2 + \sqrt{(1-2\zeta^2)^2 + 1}\right]^{\frac{1}{2}} \omega_n. \tag{16}$$

After N stages gain cells are cascaded, the overall conversion gain becomes $A^N(s)$. The -3-dB bandwidth of the LA is reduced to ω_c, where

$$\omega_c = \left[1 - 2\zeta^2 + \sqrt{(1-2\zeta^2)^2 + 2^{\frac{1}{N}} - 1}\right]^{\frac{1}{2}} \omega_n. \tag{17}$$

For a Butterworth response, we want to have $\zeta \approx \sqrt{2}/2$. By substituting (16) into (17), the bandwidth requirement for a single-stage amplifier in terms of the cascaded amplifier's -3-dB bandwidth can be derived as

$$\omega_s = \left(\frac{1}{2^{\frac{1}{N}} - 1}\right)^{\frac{1}{4}} \omega_c. \tag{18}$$

Also, the gain requirement of the individual stage, A_s, in terms of the LA's conversion gain, A_c, can be expressed as

$$A_s = A_c^{\frac{1}{N}}. \tag{19}$$

Under the above assumptions, the unity-gain frequency ω_u for the individual stages in terms of the targeted A_c and ω_c can be derived by substituting (19) and (17) into (15). Let $|A(j\omega_u)| = 1$, we have

$$\omega_u = \omega_c \cdot \left(\frac{1}{2^{\frac{1}{N}} - 1}\right)^{\frac{1}{4}} \times \left(A_c^{\frac{2}{N}} - 1\right)^{\frac{1}{4}}. \tag{20}$$

For a common-source voltage amplifier with an input stage transconductance g_{mi} and a loading capacitor C_L, the relationship between the achievable unity gain bandwidth ω_u and the dc biased current I_{in} can be described as

$$\omega_u \propto \frac{g_{mi}}{C_L} \propto \frac{\sqrt{I_{\text{in}}}}{C_L}. \tag{21}$$

Thus, the estimated total power consumption of an N-stage LA can be approximated by

$$\begin{aligned} P &\propto N \times \omega_u^2 \\ &\propto N \times \omega_c^2 \cdot \left(\frac{1}{2^{\frac{1}{N}} - 1}\right)^{\frac{1}{2}} \times \left(A_c^{\frac{2}{N}} - 1\right)^{\frac{1}{2}}. \end{aligned} \tag{22}$$

In this design, the TIA provides a conversion gain of 55 dBΩ, and the LA provides a voltage gain of 42 dB. Both circuitries have a -3-dB bandwidth over 2 GHz for 2.5-Gbps operation. To obtain the optimum number of stages which will require the least power consumption, the simulated gain-bandwidth requirements and power consumption of LAs with various number of stages based on (22) are illustrated in Fig. 4. The gain-bandwidth product and power consumption are normalized to those of a single-stage amplifier for ease of comparison. The figure reveals that a 3-stage cascaded amplifier consumes minimum power. However, the required unity gain frequency for a single-stage amplifier would be as high as 7 GHz, which is difficult to achieve in this technology. As a compromise, we choose a 5-stage architecture for its unity gain frequency is more feasible ($\sim$ 5 GHz).

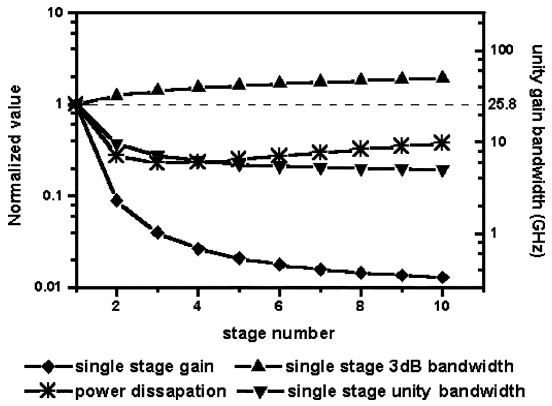

Fig. 4. Gain-bandwidth performance and power consumption versus number of stages.

In the above analysis, we use a 2-pole system to model a single-stage amplifier. Compared to a single pole model as were proposed in [11], [12], the bandwidth requirement estimated by (20) would be closer to meet the specifications.

B. Gain Cell

The core circuit of each gain cell is shown in Fig. 5, which is a source coupled pair with regulated cascode and inductive loads. The regulated cascode gain cell is free from Miller effect, which prevents signal bandwidth from being severely deteriorated when the gain cells are hooked up. On the other hand, input impedance of the common gate gain stage is reduced by the loop gain $g_{m5}/g_{m7}(g_{m6}/g_{m8})$. Thus, the nondominant pole is further pushed to a higher frequency band for stability. Let C_{L1} be the parasitic capacitance at the drain of $M3$, C_{L2} be the parasitic capacitance at the drain of $M5$, C_{L3} be the parasitic capacitance at the drain of M_{i1}, and $C_{d9\text{tot}}$ be the parasitic capacitance at the drain of M9. A_i is the single-stage small-signal dc gain, $(W/L)_i$ and $(W/L)_L$ denote the device size of M_{i1}, M_{i2}, and M_{L1}, M_{L2}. I_i and I_L represent the current flowing through input device M_i and inductor load M_L respectively, and I_b is the injected current provided by M_b.

The conversion gain of each gain cell can be derived as

$$A_v = A_i \cdot \frac{\left(1 + \frac{s}{z_1}\right)\left(1 + \frac{s}{z_2}\right)}{\left(1 + \frac{s}{p}\right)\left(1 + \frac{2\zeta s}{\omega_n} + \frac{s^2}{\omega_n^2}\right)} \tag{23}$$

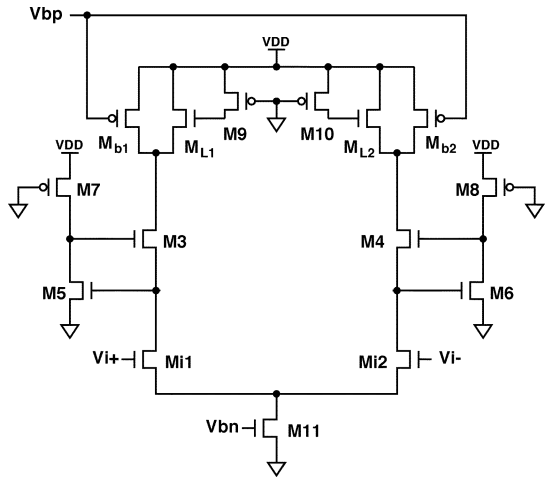

Fig. 5. LA core circuit input buffer.

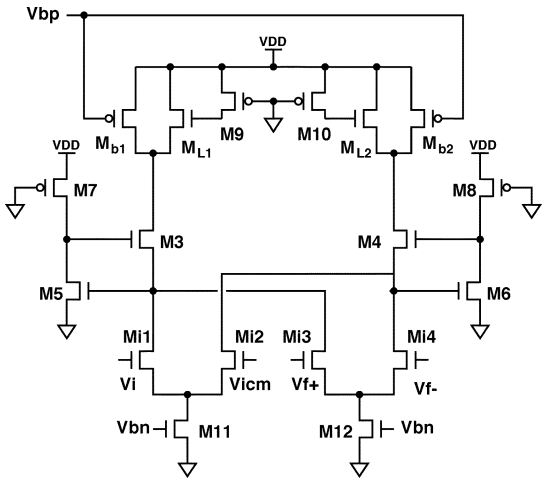

Fig. 6. LA input buffer and offset subtractor.

where

$$A_i = \sqrt{\frac{(W/L)_i I_i}{(W/L)_L I_L}} = \sqrt{\frac{(W/L)_i (I_L + I_b)}{(W/L)_L I_L}} = \sqrt{\frac{(W/L)_i}{(W/L)_L}} \sqrt{1 + \frac{I_b}{I_L}} \tag{24}$$

$$z_1 \approx \frac{g_{m9}}{C_{gsL1} + C_{d9\text{tot}}}$$

$$z_2 \approx \frac{g_{m5} + g_{m7}}{C_{L2}}$$

$$p \approx \frac{g_{mL1}}{C_{gsL1} + C_{L1}} \tag{25}$$

$$\omega_n \approx \sqrt{\frac{g_{m3} \cdot (g_{m5} + g_{m7})}{(C_{gs3} + C_{L3}) C_{L2}}} \tag{26}$$

$$\zeta = \frac{\omega_n}{2 \cdot g_{m3}} \left(C_{gs3} + \frac{g_{m7} C_{L3} + g_{m3} C_{L2}}{g_{m5} + g_{m7}} \right). \tag{27}$$

It shows that the single-stage conversion gain A_v is determined by the ratio of device size ($\sqrt{(W/L)_i/(W/L)_L}$) and the current ratio of the input device with respect to the inductive load ($\sqrt{I_i/I_L}$). To increase the conversion gain of each stage, another biased current M_{b1} and M_{b2} are injected in parallel with the active inductor. According to (24), A_i can be enhanced by boosting $\sqrt{I_b/I_L}$. Incorporating active inductor with current injection, the conversion gain and signal bandwidth can be increased simultaneously.

Equation (27) shows that p is the dominant pole frequency, z_1 is the zero introduced by the inductive load, and z_2 is contributed by the regulated cascode gain stages. Here dominant pole is located at the drain of M_3 and M_4. By choosing z_1 to be close to p, the -3-dB bandwidth of each gain stage can be extended by partially trim out the parasitic capacitance at the output node. The -3-dB bandwidth can be further enhanced by placing z_2 around the roll-off corner. The damping factor is chosen at the vicinity of 1 to avoid severe gain peaking.

The input stage of the LA is shown in Fig. 6, which plays an important role in isolating loading effects introduced by the loop

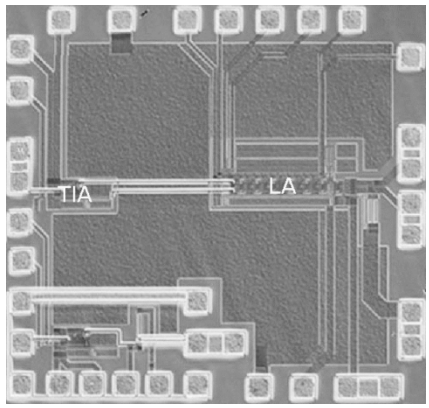

Fig. 7. Chip photograph of the optical receiver AFE.

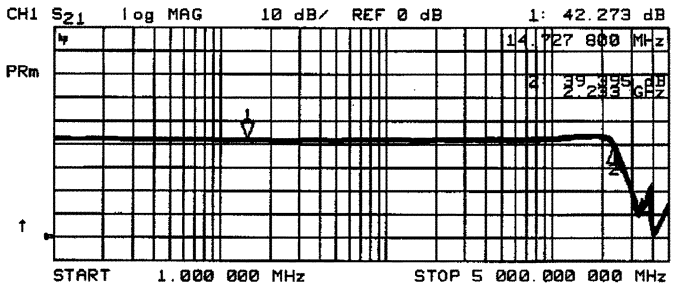

Fig. 8. Measured gain response of the LA.

filter. The source coupled pair in the input stage is decomposed into 4 transistors so as to function as an input buffer and an offset subtractor simultaneously. The offset voltage derived from the low-pass loop filter is converted to a compensation current and is subtracted from the input signal at the input node of a regulated cascode gain stage. Also, the input stage translates the single-ended input signal to fully differential output voltages, thus the amplifier chain would have higher immunity to common-mode noise.

As shown in Fig. 1, the input-referred offset voltage of the LA is derived from its output common mode voltage by a second-order low-pass filter, and fed back to the offset subtractor at the input port. By this means, LA's input-referred offset voltage is reduced by $1/A\beta$ after offset compensation, where $A\beta$ is the

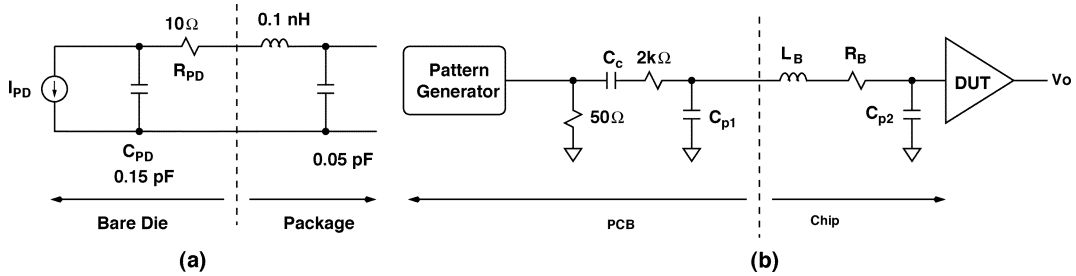

Fig. 9. (a) Photo diode with packaging parasitics. (b) Experimental setup for the receiver measuerment in the electrical domain.

closed-loop gain of the feedback network. The dominant pole of the loop filter is introduced by on chip resistors and an external capacitor to save chip area and reduce the low cutoff frequency $f_{L-3\mathrm{dB}}$. Moreover, in this design, a replicated gain cell is cascaded in front of the low-pass filter. The gain cell in the feedback path isolates the capacitive loading introduced by the feedback filters from the output port.

IV. Experimental Results

The single-chip optical receiver AFE has been fabricated in a generic single-poly triple-metal 0.35-μm digital CMOS technology. The chip micrograph of the receiver is shown in Fig. 7. Chip size is $1400 \times 1500\ \mu\mathrm{m}^2$, which is limited by testing pads. The core circuit of LA occupies a chip area of $225 \times 500\ \mu\mathrm{m}^2$, and TIA occupies a chip area of $110 \times 210\ \mu\mathrm{m}^2$ only. The chip area is mainly limited by test pads, and the two circuitries are separated by 400 μm (as far as possible) to alleviate substrate noise coupling. Operating from a single 3-V supply, the total power consumption is about 99 mW.

Also, individual TIA and LA test kits have been built up to characterize their performance in detail. Both the circuits are measured using network analyzer. The transimpedance gain and voltage gain of the receiver are derived from S-parameters. The TIA has a 3-dB bandwidth over 2.2 GHz with a conversion gain of about 54.5 dBΩ [4]. The measured gain response of LA is shown in Fig. 8. The $f_{-3\ \mathrm{dB}}$ of LA is 2.2 GHz and the conversion gain is about 42 dB, while the low cutoff frequency is about 100 kHz.

The intersymbol interferene (ISI) induced timing jitter ΔT of the receiver front-end is estimated by [15]

$$\Delta T = \frac{1}{\omega_{-3\ \mathrm{dB}}} exp(-\omega_{-3\ \mathrm{dB}} T_b). \tag{28}$$

For $\omega_{-3\ \mathrm{dB}} = 2\pi(2.2 \cdot 10^9)$ rad/s, $T_b = 0.4$ ns, the ΔT is about 0.3 ps, which is almost negligible in a 2.5-Gbps application.

The transient characteristic of the optical receiver (TIA + LA) is measured in the electrical domain. Fig. 9(a) shows the equivalent ac circuits for a 10 Gbps p-i-n photodetector [14], and Fig. 9(b) illustrates the experimental setup and its parasitic components. Here the ac coupled capacitor C_C is about 0.1 μF. The 50-Ω resistor is utilized for impedance matching. On the other hand, the 2-kΩ resistor, which is much larger than the input impedance of the TIA, is utilized to convert external voltage excitation into input current. The parasitic capacitance introduced by the surface mount *RC* devices at the input of the receiver is modeled by C_{P1}, which is about 0.3 pF and can be treated as the parasitic capacitance of a photo detector. L_B and R_B represent the inductance and series resistance of the bonding wire, which are about 3 nH and 0.3 Ω respectively. C_{p2} denotes the parasitic capacitance of the bonding pad, which is about 0.05 pF.

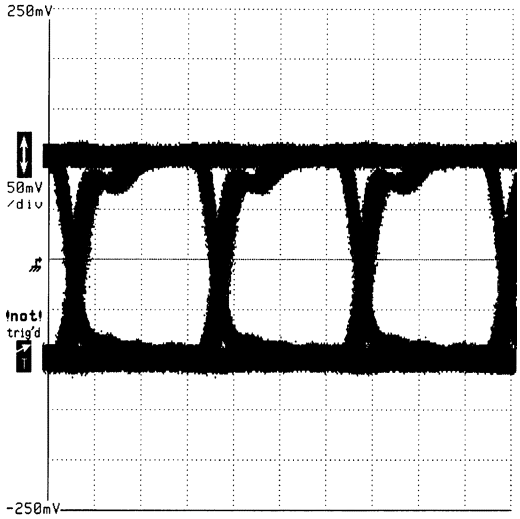

Fig. 10. Measured eye diagram @1.25 Gbps, x-axis $= 260$ ps/div, y-axis $= 50$ mV/div.

The measured input sensitivities for bit-error rate (BER) at 10^{-10} are about 12.6 and 6.5 μA, respectively, for 2.5- and 1.25-Gbps operations. The input sensitivity for BER less than 10^{-12} is estimated by extrapolation using the Q function [15]. As

$$\mathrm{BER} = Q(x) = \frac{1}{\sqrt{2\pi}x} e^{-\frac{x^2}{2}}$$
$$x = \frac{\frac{I_{pp}}{2}}{I_{\mathrm{noise,rms}}}. \tag{29}$$

Here, I_{pp} denotes the input photo current, and $I_{\mathrm{noise,rms}}$ is the rms noise current at the receiver input, including the input-referred noise of the optical receiver and external noise disturbance. The corresponding input sensitivities of the optical receiver at a BER of less than 10^{-12} are about 8 and 16 μA, respectively, for 1.25- and 2.5-Gbps operations. When the input current is a $2^{23} - 1$ PRBS test pattern, the measured eye diagrams at 1.25 Gbps ($I_{\mathrm{in}} = 8\ \mu$A) and 2.5 Gbps ($I_{\mathrm{in}} = 16\ \mu$A) are shown in Figs. 10 and 11, respectively. The LA's output swing is limited to 250 mV (single-ended, 500 mV$_{pp}$ differential) in both cases. The input dynamic range of the receiver AFE is limited by the RGC input stage of the TIA. The measured input-referred noise current of the receiver front-end is

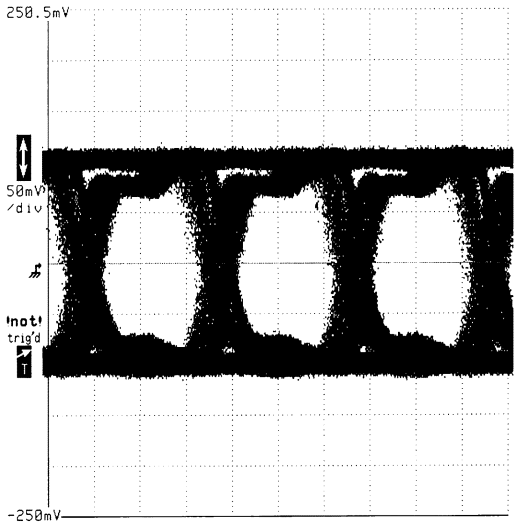

Fig. 11. Measured eye diagram @ 2.5 Gbps, $\mathrm{x-axis} = 130$ ps/div, $\mathrm{y-axis} = 50$ mV/div.

about 0.8 $\mu\mathrm{A_{rms}}$ within 2.5-GHz noise bandwidth using spectrum analyzer.

V. Conclusion

This paper describes the design of a 2.5-Gbps optical receiver AFE circuit in a low-cost digital CMOS process. Integrating both TIA and LA in a single chip, the front-end amplifier enlarges a 16 μA photo current at 2.5 Gbps to a 250 mV (single-ended) logic swing. To achieve both high gain and wide bandwidth simultaneously, several gain-bandwidth enhancement techniques have been explored to boost overall performance. Instead of using bulky spiral inductors, active inductors are utilized in this design. Thus, the chip area can be greatly reduced. The proposed architecture is suitable for low-cost application.

Acknowledgment

The authors would like to thank CIC for chip manufacturing. and NSC, ITRI/STC, and MediaTek Inc. for funding support.

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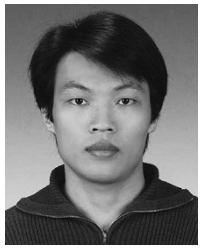

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