Phase Averaging and Interpolation Using Resistor Strings or Resistor Rings for Multi-Phase Clock Generation

Ju-Ming Chou, *Student Member, IEEE*, Yu-Tang Hsieh, and Jieh-Tsorng Wu, *Member, IEEE*

***Abstract*—Circuit techniques using resistor strings (R-strings) and resistor rings (R-rings) for phase averaging and interpolation are described. Phase averaging can reduce phase errors, and phase interpolation can increase the number of available phases. In addition to the waveform shape, the averaging and the interpolation performances of the R-strings and R-rings are determined by the clock frequency normalized by a *RC* time constant of the circuits. To attain better phase accuracy, a smaller *RC* time constant is required, but at the expense of larger power dissipation. To demonstrate the resistor ring's capability of phase averaging and interpolation, a 125-MHz 8-bit digital-to-phase converter (DPC) was designed and fabricated using a standard 0.35-μm SPQM CMOS technology. Measurement results show that the DPC attains 8-bit resolution using the proposed phase averaging and interpolation technique.**

***Index Terms*—Averaging, clocks, delay-locked loops (DLLs), interpolation, phase-locked loops (PLLs).**

I. Introduction

THIS paper deals with the generation of multi-phase clocks, i.e., generation of multiple periodic clock waveforms with different phases that equally divides the time period of an input reference clock. Multi-phase clocks can be found in applications such as timing recovery, phase/frequency modulation and demodulation, and delay measurement. The performance of those systems is mainly determined by the resolution of the available clock phases, i.e., how many and how accurate the available phases are.

Multi-phase clocks are usually generated using a delay line consisting of cascaded delay cells, whose delay time is controlled by either a delay-locked loop (DLL) or a phase-locked loop (PLL). If the delay cells are identical, then their outputs have identical waveform shapes but different phases. The number of available phases is the number of delay cells that constitute one (or half) clock period. The accuracy of the output phases is determined by the matching properties of the delay cells. At high clock frequencies, the available phases are limited by the minimum delay of the delay cells.

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It is possible to attain phase resolution beyond the phase quantization step set by the delay cells. One novel scheme is using two-dimensional array oscillators [1], [2]. The phase resolution is increased by the number of coupled rings at the expense of larger chip area and power dissipation. An alternative is using phase interpolators [3], which combine two clock waveforms of different phases to generate a new one. The resulting phase is determined by the combination weighting of the two inputs. In CMOS technologies, phase interpolators are usually realized using two source-coupled pairs (SCPs) sharing the same output port; and the ratio of their tail currents set the combination weighting. However, the relationship between the output phase and the current ratio is not linear and sensitive to other factors such as SCPs transconductance characteristics, waveform shape of the inputs, and the pole frequency of the output port. Phase accuracy can be improved by using cascaded arrays of identical phase interpolators with fixed combination weighting [4]. In this scheme, each phase interpolator is optimized to produce an output whose phase is located at the center of the two input phases.

This paper describes a circuit technique that uses resistor strings (R-strings) or resistor rings (R-rings) for phase interpolation. Due to the symmetric nature of the circuit topology, the phases of the generated new clocks can be uniformly spaced. The R-strings and R-rings also exhibit an averaging capability that can reduce phase error caused by mismatches among the delay cells [5]–[7].

The rest of this paper is organized as follows. Section II describes the phase averaging technique using the R-strings. A simplified model with capacitive loadings is used to analyze the phase averaging effect. Section III introduces the phase interpolation technique using the R-strings. The impact of capacitive loading on phase interpolation is also discussed. Section IV describes the condition and benefits of using R-rings. Section V describes a 125-MHz 8-bit CMOS digital-to-phase converter (DPC) to demonstrate the proposed phase averaging and interpolation techniques. The DPC chip was fabricated in a standard 0.35-μm CMOS technology [8]. Finally, conclusions are drawn in Section VI.

II. Phase Averaging Using R-String

Fig. 1(a) shows a simple delay line consisting of multiple delay cells. Assuming identical delay cells, the output of each delay cell would produce an equally-spaced phase. However, due to the mismatches among the delay cells, the phase difference between two adjacent delay cells would not be the same along the delay line.

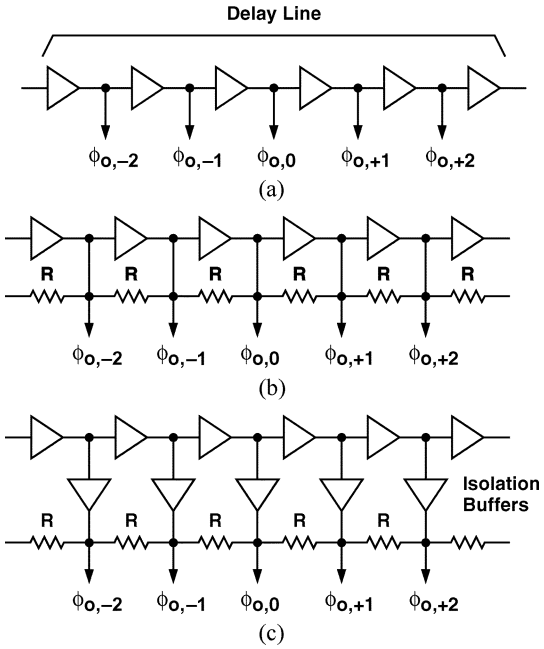

Fig. 1. (a) A simple delay line. (b) A delay line with a R-string. (c) A delay line with a R-string and isolation buffers.

Fig. 1(b) shows the schematic of a delay line coupling with a R-string whose resistor element has an identical resistance of R. The R-string introduces a spatial filtering effect on the outputs [7]. When R approaches to infinity, the interconnection between adjacent delay cells breaks and the outputs of the delay line are determined merely by their corresponding delay cells. With shrinking R, each output would begin to be affected by the neighboring ones. That is because the output currents of each delay cell would not only flow into their own loads, but also the neighboring ones via the R-string. The interaction between the outputs leads to the basic concept of phase averaging.

For most delay cell designs, the delay time is controlled by varying the equivalent output resistance R_o to change the R_oC_o product associated with the output node, where C_o is the total capacitance at the output node. This R_oC_o product will be changed if the R-string is added. In addition, the value of R is small comparing to R_o so as to achieve good phase averaging effect. This will lead to a reduction in the controllable range of delay time. Thus, it is necessary to separate the function of delay time control from the R-string's phase averaging function.

Fig. 1(c) shows a schematic consisting of a delay line, R-string, and isolation buffers. The buffers isolate the delay line from large resistive and capacitive loadings, and inherit the phase information from their corresponding delay-cell output. The output resistance of the buffers should be high to attain the strongest averaging effect offered by the R-string [6], [7]. The control of the delay line is separated from the R-string. The output phase errors due to the delay-cell mismatches and buffer mismatches can be reduced by the R-string.

The voltage waveform at each output node in Fig. 1(c) is determined not only by the output currents of the neighboring isolation buffers, but also by the resistive and capacitive loadings at the output nodes. In order to quantitatively analyze the circuit's

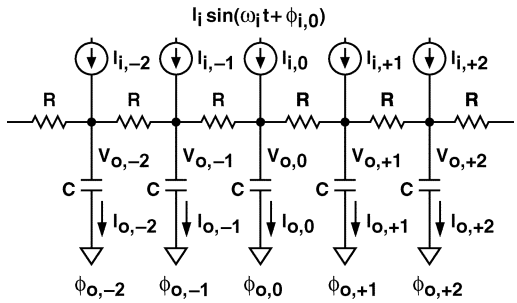

Fig. 2. A simplified model for analyzing a delay line with a R-string.

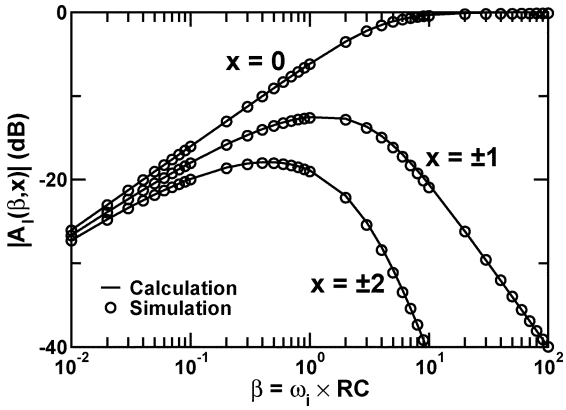

Fig. 3. R-string frequency response at locations $x = 0, x = \pm 1$, and $x = \pm 2$.

behavior, the simplified model shown in Fig. 2 is used. The capacitance at each output node is C. The buffers are modeled as ideal current sources with sinusoidal output currents expressed as

$$I_{i,x} = I_A \sin(\omega_i t + \phi_{i,x}), \qquad x = 0, \pm 1, \pm 2, \cdots \tag{1}$$

where I_A is the current amplitude, ω_i is the clock frequency, and $\phi_{i,x}$ is the clock phase. The output current flowing into the output capacitor is $I_{o,x}$. As derived in Appendix I, with $I_{i,x} = 0$ for $x \neq 0$, the frequency response of the single buffer current $I_{i,0}$ to the output current $I_{o,x}$ can be expressed as

$$A_I(\beta, x) = \frac{I_{o,x}}{I_{i,0}} = \frac{\left(-\frac{4j}{\beta}\right)^{|x|}}{\sqrt{1 - \frac{4j}{\beta}}\left(1 + \sqrt{1 - \frac{4j}{\beta}}\right)^{|2x|}} \tag{2}$$

where

$$\beta = \omega_i \times RC \tag{3}$$

is the input frequency normalized by the RC product of the R-string.

Fig. 3 shows the frequency response of $|A_I(\beta, x)|$ at different locations, i.e., $x = 0$, ± 1, and ± 2. Data from both calculation using (2) and simulation using SPICE are shown, thus verifying the validity of (2). At $x = 0$, the transfer gain $|A_I(\beta, 0)|$ is increased for larger β, i.e., at a higher clock frequency, more current flows into the capacitor directly connected to the signal source. For $\beta > 10$, $|A_I(\beta, 0)|$ approaches 1 and the R-string loses its phase averaging capability. Figs. 4 and 5 show the space response of $A_I(\beta, x)$, i.e., magnitude and phase responses at different locations, for $\beta = 1$, 1/10, and 1/100. For smaller β,

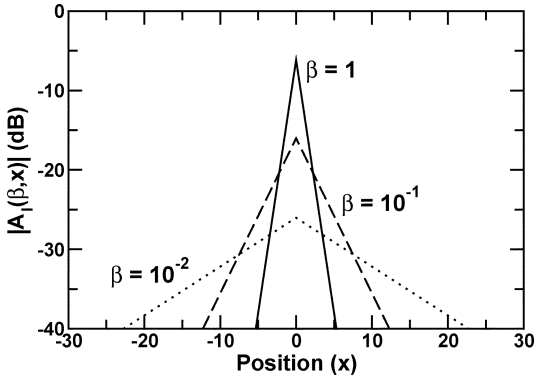

Fig. 4. R-string's space response of magnitude for $\beta = 1, 10^{-1}, 10^{-2}$.

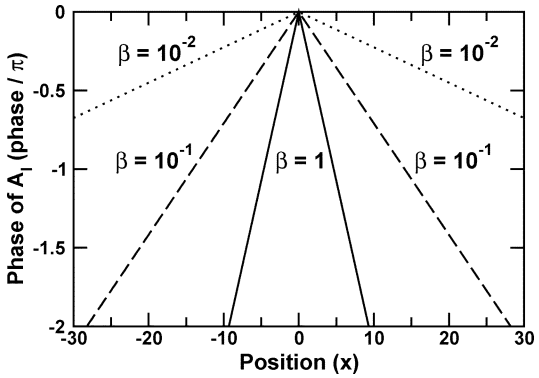

Fig. 5. R-string's space response of phase for $\beta = 1, 10^{-1}, 10^{-2}$.

the buffer current is distributed more evenly to the neighboring output capacitors, resulting in a stronger phase averaging effect.

By neglecting R-string's boundary conditions and assuming all sinusoidal current inputs have an identical amplitude of I_A, the voltage on the output nodes can be computed using spatial convolution:

$$V_{o,x} = \frac{1}{j\omega_i C} \times \sum_{k=-\infty}^{+\infty} I_{i,k} \times A_I(\beta, x-k) \tag{4}$$

$$= \frac{I_A}{j\omega_i C} \times \sum_{k=-\infty}^{+\infty} \left[|A_I(\beta, x-k)| \times \sin\left(\omega_i t + \phi_{i,k} + \angle A_I(\beta, x-k)\right)\right]. \tag{5}$$

As expressed in (5), each output voltage on the R-string, $V_{o,x}$, is a summation of sine waves with different amplitude and phases. If the current inputs, $I_{i,x}$ for all x, are sine waves with identical frequency, the resulting $V_{o,x}$ is still a pure sine wave but with different phase at different x locations. The phase of $V_{o,x}$ can be defined as the relative position of its zero crossing in the clock period.

The spatial convolution of (5) provides the necessary mechanism for phase averaging. Assume the input phases in (1) are uniformly spaced and can be expressed as

$$\phi_{i,x} = -x \cdot \Delta\phi + \phi^e_{i,x} \tag{6}$$

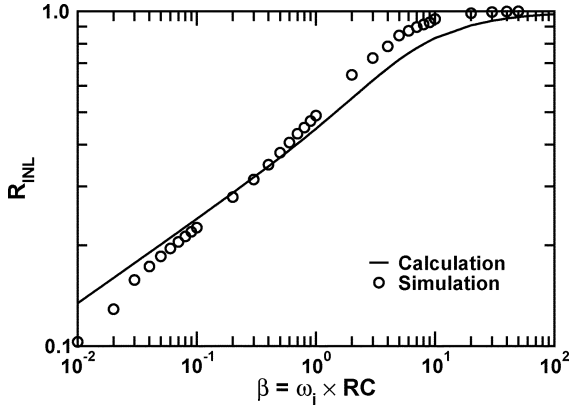

Fig. 6. R-string's INL reduction factor, $\mathcal{R}_{\rm INL}$, versus β.

where $\Delta\phi$ is the nominal phase difference between two adjacent inputs, and $\phi^e_{i,x}$ is the phase deviation at x-buffer's input. Then, the phase error, $\phi^e_{o,x}$, at the xth buffer's output can be approximated by

$$\phi^e_{o,x} \approx \frac{\sum_{k=-\infty}^{\infty}\left(M_k \times \phi^e_{i,x-k}\right)}{\sum_{k=-\infty}^{\infty} M_k} \quad \text{where } M_k = |A_I(\beta,k)|. \tag{7}$$

Equation (7) is obtained by letting $V_{o,x} = 0$ in (5). The sine functions are expanded in Taylor's series, and only the first-order terms are kept in the derivation of (7). Due to symmetric circuit topology, we have $M_{+k} = M_{-k}$. The phase response of $A_I(\beta, x)$ is not included in (7), since it causes only a constant phase shift for $V_{o,x}$ at all x locations in this first-order approximation. From (7), it is necessary to have $M_k \simeq M_0$ so that the inputs of neighboring $\pm k$-buffer can reduce the phase error, $\phi^e_{o,x}$, more effectively. Thus, the β of (3) needs to be small enough for the R-string averaging to be effective.

Let the input phase errors $\phi^e_{i,x}$ for all x be independent Gaussian variables with a mean of zero and a variance of $\sigma(\phi^e_i)$. Then, the output phase errors, $\phi^e_{o,x}$ for all x are also Gaussian, and their variance $\sigma(\phi^e_o)$ can be expressed as

$$\sigma\left(\phi^e_o\right) = \sigma\left(\phi^e_i\right) \times \left[\frac{\sum_{k=-\infty}^{\infty} M_k^2}{\left(\sum_{k=-\infty}^{\infty} M_k\right)^2}\right]^{\frac{1}{2}} = \sigma\left(\phi^e_i\right) \times \mathcal{R}_{\rm INL}. \tag{8}$$

The ratio, $\mathcal{R}_{\rm INL} = \sigma(\phi^e_o)/\sigma(\phi^e_i)$, is the R-string's reduction factor for the output phase's integral nonlinearity (INL) due to the averaging effect. Fig. 6 shows the plot of $\mathcal{R}_{\rm INL}$ ratio versus β. Data from both calculation using (8) and simulation using SPICE are shown. An R-string with a β of 1/100 is required to obtain an INL reduction factor of 1/10. Due to the use of 1st-order approximation in (7), deviation between calculation and simulation is revealed in Fig. 6.

The differential nonlinearity (DNL) for the input can be defined as $\Delta\phi^e_{i,x} = \phi^e_{i,x} - \phi^e_{i,x+1}$. The DNL for the output can be defined as $\Delta\phi^e_{o,x} = \phi^e_{o,x} - \phi^e_{o,x+1}$. Again, let the input phase errors, $\phi^e_{i,x}$ for all x, be independent Gaussian variables with a mean of zero and a variance of $\sigma(\phi^e_i)$. Then, both $\Delta\phi^e_{i,x}$ and $\Delta\phi^e_{o,x}$ are Gaussian for all x. Their variances, $\sigma(\Delta\phi^e_i)$ and

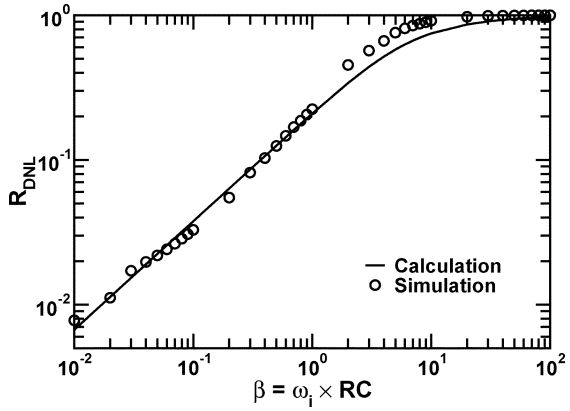

Fig. 7. R-string's DNL reduction factor $\mathcal{R}_{\rm DNL}$ versus β.

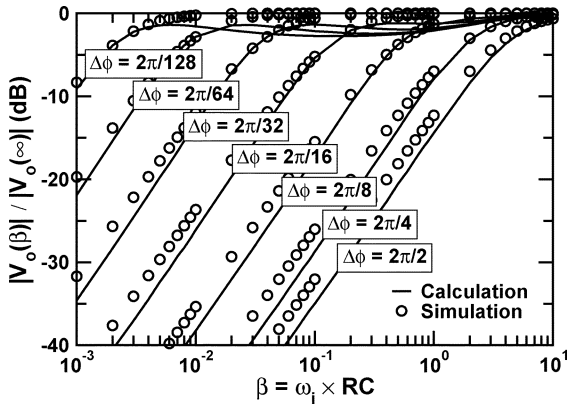

Fig. 8. R-string voltage response for different input phase spacing.

$\sigma(\Delta\phi_o^e)$, can be calculated using (7). The R-string's reduction factor for the output phase's DNL can be expressed as

$$\mathcal{R}_{\rm DNL} = \frac{\sigma\left(\Delta\phi_o^e\right)}{\sigma\left(\Delta\phi_i^e\right)} = \frac{\sqrt{2}}{2} \times \left[\frac{\sum_{k=-\infty}^{\infty}\left(M_k - M_{k-1}\right)^2}{\left(\sum_{k=-\infty}^{\infty} M_k\right)^2}\right]^{\frac{1}{2}}. \tag{9}$$

Fig. 7 shows the plot of $\mathcal{R}_{\rm DNL}$ ratio versus β. Data from both calculation using (9) and simulation using SPICE are shown. Comparing Fig. 7 to Fig. 6, the R-string is more effective in improving DNL than improving INL. This is expected from the spatial convolution function.

In addition to averaging, it is also necessary to consider the magnitude of voltage swing on the R-string, which must be sufficiently large to drive the succeeding circuitry. The peak-to-peak value of $V_{o,x}$, defined as $V_{o,pp}$, can be approximated by using (5) with $\omega_i t + \phi_{i,x} + \measuredangle A_I(\beta, 0) = \pm\pi/2$. Fig. 8 shows the results for different values of β and input phase spacing, $\Delta\phi$. Data from both calculation using (5) and simulation using SPICE are shown. In Fig. 8, the $V_{o,pp}$ is normalized by the peak-to-peak output voltage when $R = \infty$, $V_{o,\infty}$. The $V_{o,\infty}$ can be simply expressed as

$$V_{o,\infty} = \left|\frac{I_A}{j\omega_i C}\right| \tag{10}$$

where I_A is the current amplitude of all $I_{i,x}$ inputs. For a diminishing value of β, the response from any current input, $I_{i,x}$, to any output node becomes identical, i.e., $A_I(\beta, x) \approx A_I(\beta, x-k)$ for all k. As a result, every sine term in (5) is cancelled by another sine term with almost identical magnitude and $\pm\pi$ phase difference, thus resulting in a reduced $V_{o,pp}$.

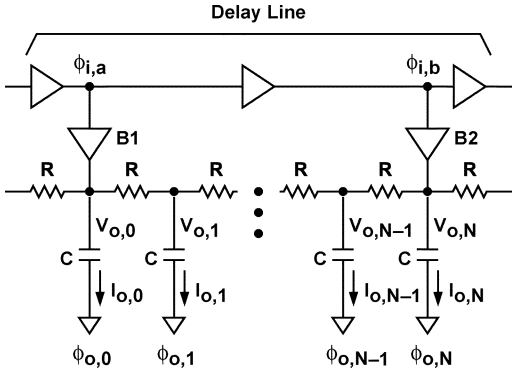

Fig. 9. Phase interpolation using R-string.

For a given ω_i and C, β can be reduced by using a smaller R to enhance the averaging effect. But a smaller β also results in decreasing voltage swing on the R-string, $V_{o,pp}$. Then, it is necessary to increase the buffer current I_A to restore $V_{o,pp}$. In other words, averaging effect can be enhanced by reducing R, but at the expense of more power dissipation so as to maintain the voltage swing on the R-string.

III. Phase Interpolation Using R-String

As illustrated in Fig. 9, the R-string can also be used for phase interpolation. The outputs of the buffers are connected using a R-string. There are N identical resistors between the B1 and B2 buffers. Thus, additional $\mathrm{N}-1$ clock phases are generated from the two original periodic waveforms with different phases of $\phi_{i,a}$ and $\phi_{i,b}$. The desired interpolated phases are

$$\phi_{o,x} = \phi_{o,0} - \delta\phi \times x \quad 1 \le x \le N-1 \tag{11}$$

where $\delta\phi = (\phi_{o,0} - \phi_{o,N})/N$. Ideal phase interpolation can be achieved only if waveforms of $V_{o,0}$ and $V_{o,N}$ in time domain are two parallel lines. Larger phase difference between $V_{o,0}$ and $V_{o,N}$ together with sharp transition of the rising/falling edges can lead to poor accuracy in phase interpolation. Once the errors in interpolation due to waveform shape is minimized by choosing a smaller phase difference between the input buffers and increasing the rise/fall times of the voltage waveforms on the R-string, the *RC* delay of the R-string ultimately dominates the error in phase interpolation.

Consider only the phase interpolation error due to the *RC* effect. The voltage on the R-string's internal nodes can be approximated by

$$V_{o,x} = \sum_{k=-\infty}^{\infty}\left[V_{o,-kN} \cdot H(x+kN)\right] \tag{12}$$

where

$$H(x) = e^{-|x|\sqrt{\frac{\beta}{2}}} \exp\left(-j|x|\sqrt{\frac{\beta}{2}}\right). \tag{13}$$

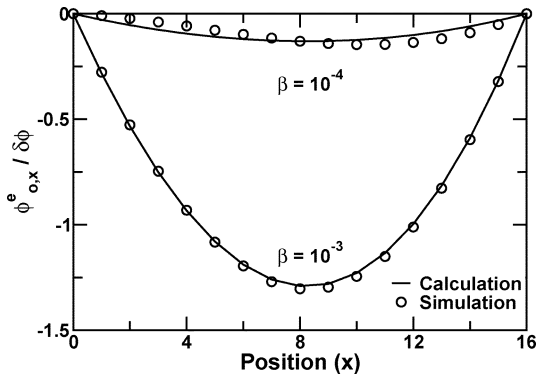

Fig. 10. Phase error of a 16X R-string phase interpolator.

Equation (13) represents the magnitude and phase responses of an infinite *RC* ladder network with a voltage signal source connected to the $x = 0$ node. Equation (13) was obtained by curve fitting the data from SPICE simulations of a *RC* ladder network. Assuming sinusoidal inputs and using the first-order approximation similar to one described in the previous section, the phase at node X can be expressed as

$$\hat{\phi}_{o,x} \approx \frac{\sum_{k=-\infty}^{\infty} \{|H(x+kN)| \cdot [\phi_{o,-kN} + \angle H(x+kN)]\}}{\sum_{k=-\infty}^{\infty} |H(x+kN)|} \tag{14}$$

where $\beta = \omega_i \times RC$ as defined in (3). From (11) and (14), the phase error $\phi^e_{o,x} = \hat{\phi}_{o,x} - \phi_{o,x}$ can then be obtained by

$$\phi^e_{o,x} = \hat{\phi}_{o,x} - \hat{\phi}_{o,0} + \delta\phi \times x. \tag{15}$$

Fig. 10 compares the calculation results using (15) with the simulation results. The R-string phase interpolator in Fig. 9 with $N = 16$ is used as an example. The isolation buffers, B1, B2, ..., output sinusoidal currents, and the phase difference between $\phi_{o,0}$ and $\phi_{o,16}$ is $2\pi/16$. Notably, the maximum phase error occurs around $x = N/2$. For a larger value of β, the phase error caused by the *RC* delay is more noticeable. In this case, a β on the order of 10^{-4} is required to obtain a maximum phase error less than $0.5 \times \delta\phi$.

IV. Resistor Rings

In Fig. 1(c) and Fig. 9, the mechanism of phase averaging and interpolating is accomplished by using R-string to distribute each buffer's output current to its neighboring output nodes. It is assumed that all buffers along the R-string experience the same circuit configuration at the output port, so that transfer functions such as (2) are identical for all buffers. However, at locations near both terminals of a R-string, the above assumption is no longer valid, and systematic phase errors occur. This edge-distortion phenomenon can be eliminated by using a R-ring. As shown in Fig. 11, if the phase shift along the delay line spans a full clock period, the two terminals of a R-string can be connected seamlessly to form a ring. Then all buffers (not shown in the figure) see the same output circuit configuration regardless of their locations. It is obvious that an oscillator can be formed by shorting the V_i and V_o of the delay line, whose delay can be controlled using a phase-locked loop.

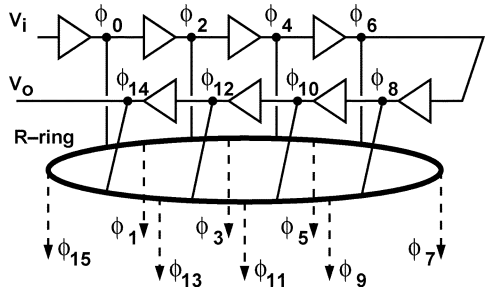

Fig. 11. Phase interpolation and averaging using R-ring.

V. Design Example

A 125-MHz 8-bit DPC has been designed to demonstrate the feasibility of phase interpolation and averaging using R-rings [8]. The DPC receives a reference clock at V_i and generate a clock of the same frequency at V_o with phase controlled by the 8-bit digital control input Din[7:0]. The total number of adjustable phases is 256, which is equally spaced in one clock period. Fig. 12 shows the DPC's block diagram. The DPC includes two delay lines with delay cells D1–D16 and D17–D24. All delay cells are identical and exhibit the same time delay. The delay is controlled by a delay-locked loop, so that the total delay of the first delay line, D1–D16, is one clock period and the total delay of the second delay line, D17–D24, is half clock period. At 125 MHz, one clock period T_s is 8 nsec, and one delay-cell delay t_d is 500 ps. The D1–D16 delay line produces 16 clocks with equally-spaced phases. The first ring, R-Ring 1, is added to reduce phase errors caused by mismatches among the delay cells as well as the isolation buffers. One of the clocks is selected by the MUX1 multiplexer to drive the D17–D24 delay line. The second ring, R-Ring 2, is used for phase interpolation. The MUX2 multiplexer selects one of 16 phases interpolated between the input and output signals of the D21 delay cell for the final clock output at V_o. The final timing resolution is $t_d/16 = 31.25$ ps, which is defined as 1 LSB for this 8-bit DPC.

The total delay of the D17–D24 delay line needs to be one half of the clock period in order to use the R-ring configuration for phase interpolation. It is granted that using the R-Ring 2 is not the most efficient scheme to interpolate the final 16 phases. One possible alternative is using a R-string for phase interpolation, which can be driven by fewer delay cells.

At circuit level, all delay cells are fully differential, thus 8 delay cells locked in half clock period with their complementary outputs can provide clock phases spanning a full clock period to drive the R-rings. However, the phase difference between the D1's positive output and D8's negative output as well as the phase difference between the D1's negative output and D8's positive output are distorted if the clock's duty cycle is not 50%. Thus, in this DPC design, a 16-stage delay line is used to drive R-Ring 1, so as to reduce phase error caused by duty cycle variation. On the other hand, an 8-stage delay line is used to drive R-Ring 2, since only the middle segment around D21 is critical for the required phase interpolation.

At input frequency $\omega_i = 125$ MHz, the β of R-Ring 1, as defined in (3), is 1/18 with $R = 240\ \Omega$. The differential voltage swing on R-Ring 1 is 1.12 V. The β of R-Ring 2 is 1/8500 with

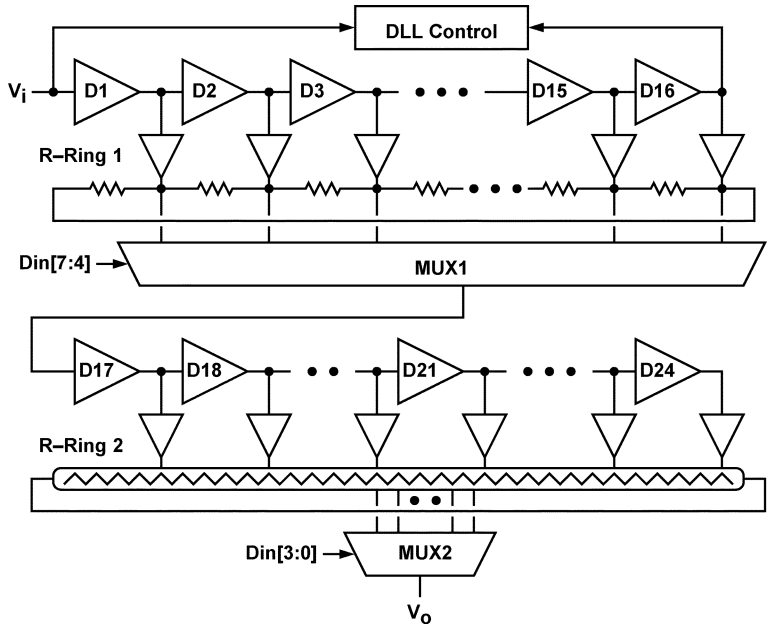

Fig. 12. An 8-bit DPC.

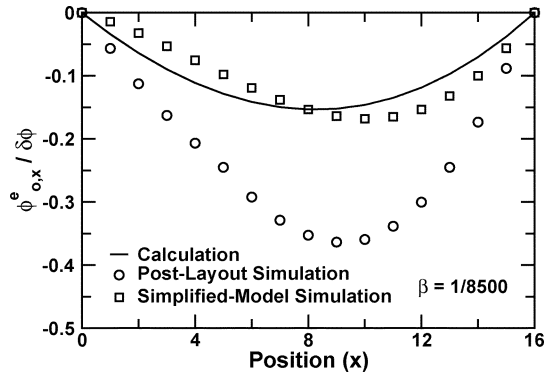

Fig. 13. Phase error of the R-Ring 2 phase interpolator.

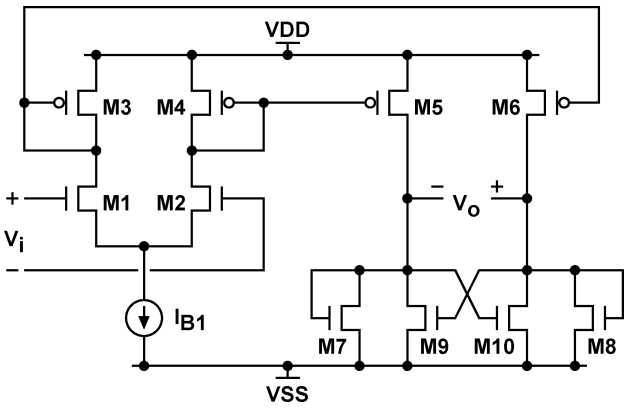

Fig. 14. Isolation buffer circuit schematic.

$R = 15\ \Omega$. The differential voltage swing on R-Ring 2 is 1 V. Fig. 13 shows the phase error of the R-Ring 2 phase interpolator from the results of both simulations and calculation of (15). Two different sets of simulations have been performed. One used circuit with devices and interconnects extracted from layout. One used the simplified circuit model described in Section III. The phase interpolator achieves a phase error less than $0.5 \times \delta\phi$, where $\delta\phi = 31.25$ ps. The phase errors obtained from the post-layout simulation are larger than those predicted by (15). This is mainly due to the fact that the clock signals are no longer sine waves.

The DPC is realized using the fully-differential current-mode logic circuit configuration. The delay cells are self-biased source-coupled pair with symmetrical loads [9]. A single-to-differential converter and a duty-cycle corrector (DCC) [10] are placed at the V_i input so that a single-ended reference clock can be converted into a differential signal with 50% duty cycle. Fig. 14 shows the schematic of the buffers placed between the delay lines and the R-rings. The combination of the M7–M8 diode-connected loads and the M9–M10 cross-coupled loads exhibits large differential-mode resistive loading and low common-mode resistive loading, eliminating the use of common-mode feedback [11]. The M3–M6 and M4–M5 current mirrors are designed to provide a current gain of 4.

The DPC was fabricated using a standard 0.35-μm single-poly quad-layer metal (SPQM) CMOS technology. Fig. 15 shows the chip micrograph. The chip area occupied by the DPC is $500 \times 600\ \mu\text{m}^2$. Fig. 16 shows the floorplan of R-Ring 1, including the routing of the clock signals. The R-Ring is folded four times to fit the width of overall floorplan, and also to reduce the effects of process gradient. The isolation buffers are placed around the R-Ring. The individual resistor is realized using polysilicon resistor with a resistance of $R = 240\ \Omega$ and a dimension of 31.4 μm by 1.6 μm. The random mismatch between the resistors is estimated to be $\sigma(\Delta R/R) = 0.63\%$. The R-Ring 2 has similar floorplan.

The input frequency of this DPC chip can be varied from 50 to 250 MHz. The power dissipation is 110 mW from a 3.3 V supply. The measured peak-to-peak jitter of the output is 30 ps

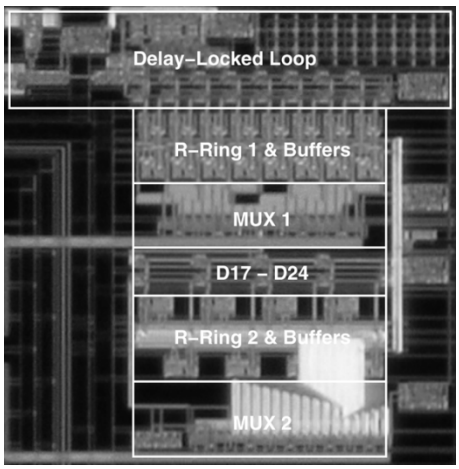

Fig. 15. Chip micrograph.

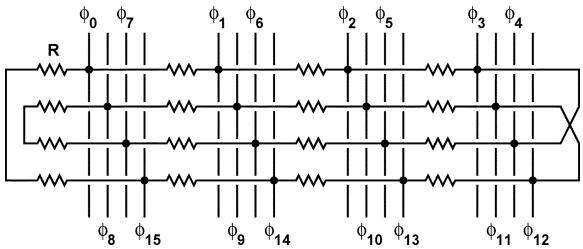

Fig. 16. Floorplan of R-Ring 1.

and the root-mean-square (RMS) jitter is 5.1 ps, while the RMS jitter of the input clock is 3.2 ps.

Define the DPC's normalized output phase with input $D_{\text{in}} = k$ as

$$\theta_o(k) = \frac{T(k) - T(0)}{\text{LSB}} \tag{16}$$

where $T(k)$ is the relative time delay of the DPC's output. Fig. 17 shows the measured DPC's transfer characteristic, i.e., θ_o versus D_{in}. The DPC's DNL, which is defined as $\theta_o(k+1) - \theta_o(k) - 1$ for $k = 0, \ldots, 254$, exhibits a similar pattern every 16 consecutive input codes, indicating some layout mismatches around the MUX2. The mismatches are mainly due to the parasitic capacitance of the interconnects. The DNL is within ± 1 LSB at most of the input codes, except the recurring -1.8 LSB DNL errors every 16 input codes. The INL, which is defined as $\theta_o(k) - k$ for $k = 0, \ldots, 255$, is measured to be within ± 2 LSB.

VI. Conclusion

Resistor strings can be used for phase averaging and interpolation. Phase averaging can reduce phase errors and phase interpolation can increase number of available phases. When clock phases spanning a full period are available for driving a resistor string, a resistor ring are preferred to mitigate the edge-distortion phenomenon. Capacitors on the resistor strings (or rings) can degrade the effectiveness of both averaging and interpolation. The design parameter $\beta = \omega_i \times RC$ need to be carefully chosen to optimize the tradeoff between phase accuracy and power dissipation.

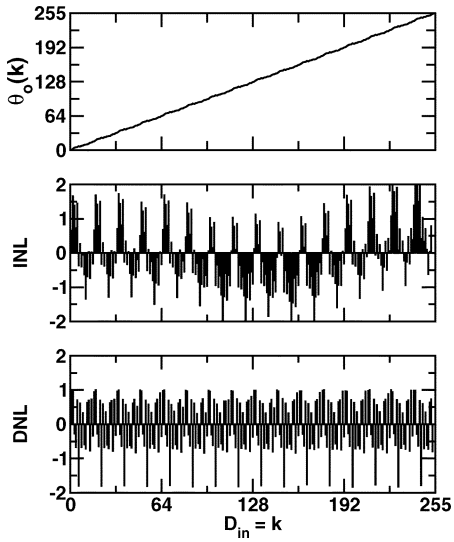

Fig. 17. Measured DPC transfer characteristics.

To demonstrate the R-Ring's capability of phase averaging and interpolation, a 125-MHz 8-bit DPC was designed and fabricated using a standard 0.35-μm SPQM CMOS technology. The DPC consists of two delay lines driving two R-rings respectively. Together, they generate 256 different clock phases. Measurement results show 8-bit resolution is possible using the R-ring technique.

Appendix
R-String's Frequency Response

In Fig. 2, the node, $V_{o,0}$, connects a current source, a capacitor, and two *RC* ladder networks on the right and left. If the length of the two networks is infinity, then the input impedance of each network can be expressed as

$$Z_{ld} = \frac{1}{2}R + \frac{1}{2}\sqrt{R^2 + 4RZ_c} \tag{17}$$

where $Z_c = 1/(j\omega_i C)$. Let $I_{i,x} = 0$ for $x \neq 0$. Using the principle of current dividing, the current flowing in the capacitor connected to the $V_{o,0}$ node is

$$I_{o,0} = I_{i,0} \times \frac{Z_{ld}}{2Z_c + Z_{ld}}. \tag{18}$$

The current flowing in the capacitor connected to the $V_{o,\pm 1}$ nodes can be computed from $I_{o,0}$ as

$$I_{o,\pm 1} = I_{o,0} \times \frac{Z_c}{Z_{ld}} \times \frac{Z_{ld}}{Z_c + Z_{ld}}. \tag{19}$$

The current flowing in the capacitor connected to the $V_{o,x}$ node, for $|x| > 1$, can be computed from $I_{o,|x|-1}$ as

$$I_{o,x} = I_{o,|x|-1} \times \frac{Z_c}{Z_{ld}} \times \frac{Z_{ld}}{Z_c + Z_{ld}}. \tag{20}$$

Thus, the frequency response of the current gain from $I_{i,0}$ to $I_{o,x}$ can be written as

$$\frac{I_{o,x}}{I_{i,0}} = \frac{R+\sqrt{R(R+4Z_C)}}{R+\sqrt{R(R+4Z_C)}+4Z_C} \times \left[\frac{2Z_C}{2Z_C+R+\sqrt{R(R+4Z_C)}}\right]^{|x|}. \quad (21)$$

Replacing $\omega_i \times RC$ with β, the above equation can be manipulated to obtain (2).

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REFERENCES

[1] J. G. Maneatis and M. A. Horowitz, "Precise delay generation using coupled oscillators," *IEEE J. Solid-State Circuits*, no. 12, pp. 1273–1282, Dec. 1993.

[2] J.-T. Wu, H.-D. Chang, and P.-F. Chen, "A 2 V 100-MHz CMOS vector modulator," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf.*, Feb. 1997, pp. 80–81.

[3] S. Sidiropoulos and M. A. Horowitz, "A semidigital dual delay-locked loop," *IEEE J. Solid-State Circuits*, no. 11, pp. 1683–1692, Nov. 1997.

[4] B. W. Garlepp, K. S. Donnelly, J. Kim, P. S. Chau, J. L. Zerbe, C. Huang, C. V. Tran, C. L. Portmann, D. Stark, Y.-F. Chan, T. H. Lee, and M. H. Horowitz, "A portable digital DLL for high-speed CMOS interface circuits," *IEEE J. Solid-State Circuits*, no. 5, pp. 632–644, May 1999.

[5] K. Kattmann and J. Barrow, "A technique for reducing differential nonlinearity errors in flash A/D converters," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf.*, Feb. 1991, pp. 170–171.

[6] K. Bult and A. Buchwald, "An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm^2," *IEEE J. Solid-State Circuits*, no. 12, pp. 1887–1895, Dec. 1997.

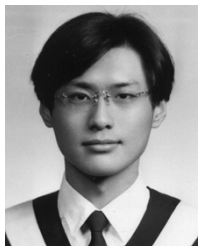
[7] H. Pan and A. A. Abidi, "Spatial filtering in flash A/D converters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 8, pp. 424–436, Aug. 2003.

[8] J.-M. Chou, Y.-T. Hsieh, and J.-T. Wu, "A 125 MHz 8b digital-to-phase converter," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf.*, Feb. 2003, pp. 436–437.

[9] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits*, no. 11, pp. 1723–1732, Nov. 1996.

[10] T. H. Lee, K. S. Donnelly, J. T. C. Ho, J. Zerbe, M. G. Johnson, and T. Ishikawa, "A 2.5 V CMOS delay-locked loop for 18 Mbit, 500 megabyte/s DRAM," *IEEE J. Solid-State Circuits*, no. 12, pp. 1491–1496, Dec. 1994.

[11] B.-S. Song, S.-H. Lee, and M. F. Tompsett, "A 10-b 15-MHz CMOS recycling two-step A/D converter," *IEEE J. Solid-State Circuits*, no. 12, pp. 1328–1338, Dec. 1990.



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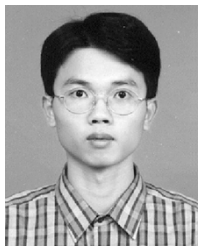

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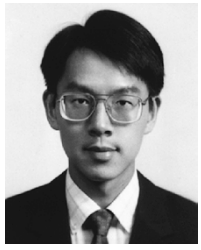

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