Effective Electrostatic Discharge Protection Circuit Design Using Novel Fully Silicided N-MOSFETs in Sub-100-nm Device era

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***Abstract*—In this paper, the floating charge effect is considered in the design of new fully silicided NMOSFETs for designing electrostatic discharge (ESD) protection circuit consisting of nanodevices. According to the designed, fabricated, and studied new fully silicided ESD protection nanodevices (e.g., 90-nm CMOS devices), our investigation demonstrates that there is a significant improvement in sustaining ESD robustness than that of the conventional fully silicided device. Furthermore, it has an excellent electrical efficiency compared with that of drain-ballast resistor-tied devices. Moreover, our novel design exhibits a higher driving current and better reliability without suffering the off-state current of the fully silicided devices. Those good characteristics are especially suitable for the output buffer design in which both driving capability and ESD robustness have to be considered.**

***Index Terms*—Circuit design, design, electrostatic discharge (ESD), fabrication, floating charge effect, fully silicided, measurement, nanodevice, semiconductor devices, silicide-blocked, simulation, ULSI.**

I. Introduction

RECENTLY, the susceptibility of integrated circuits (ICs) to electrostatic discharge (ESD) has warranted the use of dedicated on-chip ESD protection circuits. A great deal of attention was paid to solving the ESD issues; however, design of robust ESD circuits still remains challenging as critical devices dimensions are continuously shrinking [1]–[3]. It is known that the operation speed of ICs will become faster and faster when the geometry of devices gets smaller and smaller. Unfortunately, a high risk of the ESD damage has also been caused. The consequence mainly results from the fact that a thinning down of gate oxide will make the turn-on voltage of parasitic bipolar junction transistors (BJTs) higher than the breakdown voltage of the gate oxide; therefore, it increases the possibility of gate-oxide damage during ESD stressing.

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To enhance the robustness of the ESD protection circuit, the drain-ballast resistors made from the silicide-blocked diffusion region has long been designed between the drain contacts and polysilicon gates [4]–[7]. However, this approach requires an additional photo-mask, enlarges the device's area, and needs an extra device model in VLSI circuit design. The consequence will increase the process cost, lower the device's density, and degrade the circuit performance. Therefore, a fully silicided MOSFET device is an attractive candidate in ESD protecting circuits. Unfortunately, it suffers a low ESD robustness [8]–[11], in particular, for the sub-100-nm device era.

In this paper, we propose a novel fully silicided MOSFET structure for robust ESD protection circuit design consisting of sub-100-nm devices. This alternative lets the body electrode remain in a floating state under ESD stress. The experimental results show that the floating body effects reduce the turn0on voltage, improve the ESD performance, and have a better robustness for sub-100-nm device design. The test devices are fabricated with a standard CMOS process with a gate length of 90 nm and a gate-oxide thickness of 1.2 nm. The ESD characteristics are verified with the TLP systems with a pulsewidth of 100 ns [3], [12], [13]. It is found that the new fully silicided device has improved ESD robustness than the conventional one. Reliability of the new fully silicided device is also taken into consideration. We find that the new device has a relatively better reliability than the conventional approach does; moreover, the driving capability of the device is also enhanced. The achievement is significant and suitable for designing an output buffer in which all of the ESD strength, reliability, and driving capability are important elements.

The improvement is caused from the accumulation of impact ionization holes that build up an electrostatic potential at the substrate; consequently, it decreases the turn-on voltage of parasitic BJT. A decrease of turn-on voltages will suppress the damage of gate oxide and reduces the electric fields at the drain junctions. We indicate that a wider current path exists in the new devices; as a result, the device sustains a better ESD strength than the conventional one does. A constructive alternative is also demonstrated here for designing a fully silicided ESD protection circuit. It exhibits an excellent efficiency in both ESD protection and chip area and is very attractive to sub-100-nm CMOS circuit era.

This paper is organized as follows. In Section II, we state the experiment and characterization. In Section III, we report and discuss the results. Section IV draws the conclusion.

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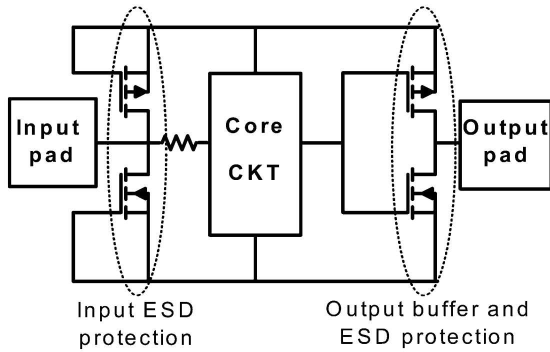


Fig. 1. Protection schematic used in the IC design.

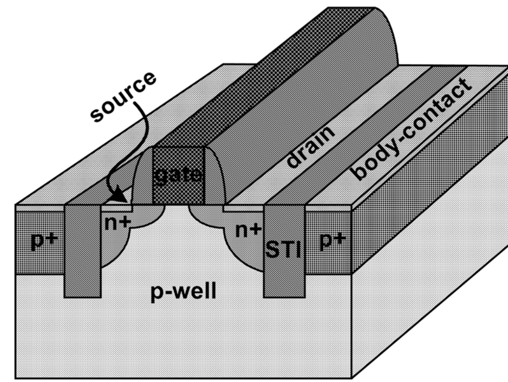
II. Experiment and Device Structure

The fully silicided and silicide-blocked devices are fabricated by using United Microelectronics Corporation (UMC) 90-nm CMOS technology. The manufacturing process has the following requirements: 1) the minimum feature size of the process is 90 nm; 2) the oxide thickness of the devices is 1.2 nm; 3) the silicide is formed by using a two-step self-align cobalt silicide process in which a 30-nm-thick cobalt-silicide is formed selectively on the source, drain, and gate regions; and 4) the drain-ballast resistor is formed by using a silicide-blocked process that is achieved by depositing a 100-nm-thick chemical vapor deposition oxide on the blocked regions prior to the formation of cobalt silicide.

TLP measurement is done by using the Barth Electronics Model 4002 TLP system. The pulsewidth of the measurement is 100 s, which is is highly correlated with the Human Body model (HBM). Finally, an HP 4156B semiconductor analyzer analyzes the quasi-static characteristics of the devices. An accelerated test is performed by applying 3.3 V on both gate and drain electrodes of the device for over 20 000 s. It should be noticed that the normal operation voltage of those devices is only about 1.2 V, thus we applied nearly three times the normal operation voltage at the accelerated tests. During the accelerated tests, the quasi-static current–voltage (I–V) characteristics are measured every 1000 s in calculating the transconductance (gm) degradation. Based on the numerical solution of a set of semiconductor device equations, the developed device simulator is applied to theoretically explain and investigate the floating charge effects in the proposed fully silicided device [14], [15]. The simulation model includes the Poisson equation, the electron–hole current continuity equations, the impact ionization, and the electron–hole energy conservation equations.

III. Results and Discussion

The pMOSFET and nMOSFET pairs are the most used ESD protection devices that prevent the input and output circuits from ESD current damage. The protection schematic is shown in Fig. 1, in which nMOSFETs and pMOSFETs are tied between the input/output pads to the ground and power lines, respectively. A more detailed observation could be drawn that the protection devices at the input pads are gate-grounded structures for leakage suppression. On the other hand, the protection devices are always functioning as an output buffer at the output pads to have a higher driving capability. According to the protection schematic, it will be summarized that an ideal protection device has to include several characteristics, which are the high ESD robustness, short response time, compatibility with the integration circuit process, and high driving capability.



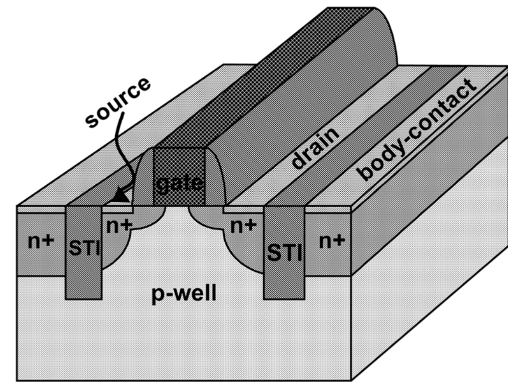


Fig. 2. (a) Conventional fully silicided N-MOSFET. (b) Proposed fully silicided floating-body NMOSFET.

When considering the ESD robustness, the fully silicided devices are conventionally not taken into account for ESD protection design because of their low ESD robustness. This is mainly because the gate-oxide and channel regions can be easily damaged by the over quantity of both current and voltage. Thus, in avoiding the undesired voltage and current distributions, the floating body design is taken into consideration in this study. The difference between the conventional fully silicided and our proposed fully silicided devices could be clearly found from the three-dimensional (3-D) topological views shown in Figs. 2 and 3, respectively. The pickup design is the only difference between the conventional device and our proposed device, i.e., the p^+ pickup drawn for the conventional device and the n^+ pickup designed for our proposal. The difference between the conventional and our proposed fully silicided devices is small, but the difference in the ESD robustness between these two structures is significant. The improvement of our proposed device can be easily investigated from Fig. 4, which presents I–V characteristics measured from the TLP. It is found that the floating body design sustains a much better ESD robustness than the grounding one. Shown in this figure, we can also demonstrate the problem of the conventional fully silicided device that failure at the mean

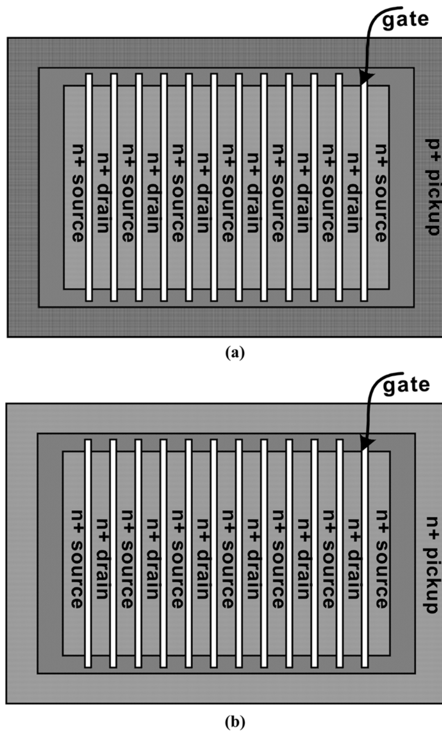


Fig. 3. Top view of (a) the conventional and (b) the floating body fully silicided N-MOSFET.

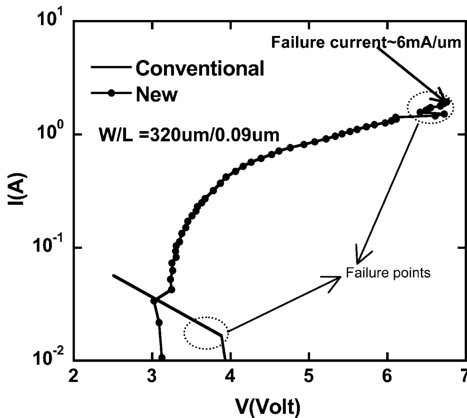


Fig. 4. Comparison of TLP I–V characteristics between the conventional (p^+ pickup) and new (n^+ pickup) devices.

time of device turning on. With this characteristic, we can conclude that an enlargement of device area will do nothing for the enhancement of ESD robustness. These results are match well with our theoretical analysis results.

The TLP I–V curve of the thin gate oxide is shown in Fig. 5 for ensuring whether or not the protection device can turn on prior to the oxide breakdown. A comparison between Figs. 4 and 5 shows that the proposed fully silicided devices have a turn-on voltage of about 3.0 V, which is 1.0 V lower than the breakdown voltage of the thin gate oxide. However, the silicide-blocked body-grounded devices have a turn-on voltage that is very close to the breakdown voltage of the thin gate oxide. Those results indicate that our proposed devices have a better ability to protect gate oxide from ESD damages. Based

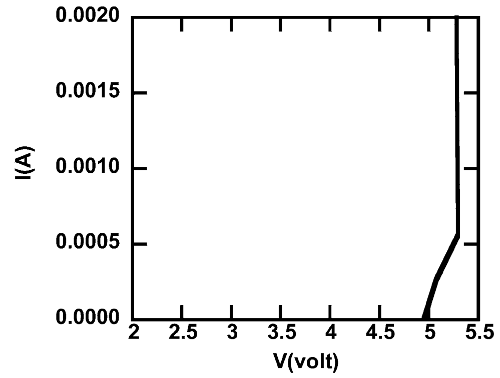


Fig. 5. TLP I–V characteristics of the thin oxides.

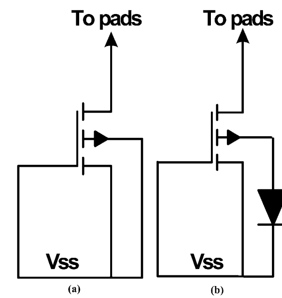


Fig. 6. Equivalent circuit of (a) the conventional and (b) the new fully silicided devices.

on our numerical simulation [3], [13]–[15], it is known that the improvement is due to the accumulation of impact ionization holes at substrate. Those accumulated holes will decrease the turn-on voltage of parasitic BJT and finally prevent the gate oxide from damage.

The holes accumulating in the floating-body device could be further explained by the equivalent circuit shown in Fig. 6. During ESD events, a diode series tied at the substrate will build up a potential and turn on the parasitic BJT earlier. Moreover, owing to a decrease in turn-on voltage, a reduction of the drain electric field could be also expected. It is even better that a wider current path should also exist in the floating-body devices and enhance the ESD strength.

Besides the much better ESD robustness, the quasi-static characteristics, shown in Fig. 7, show that our proposed device has a higher turn-on current than that of the traditional fully silicided devices. The increase of the turn-on current is also caused by the floating charge effects. The current enhancement does not affect the off-state current; this is different from conventional devices in that the leakage current will be increased at the same time. The improvement of the proposed device results from the fact that subthreshold swing is lowered by the floating charge. On the other hand, without the floating charge, the subthreshold swing of the traditional devices remains unchanged when an increase in on-current should degrade leakage current simultaneously.

The accelerated stress measurement is also performed to investigate the reliability of the floating-body devices. It is easily observed from Fig. 8 that the floating-body devices have a smaller gm gradation during the hot carrier stress process. It

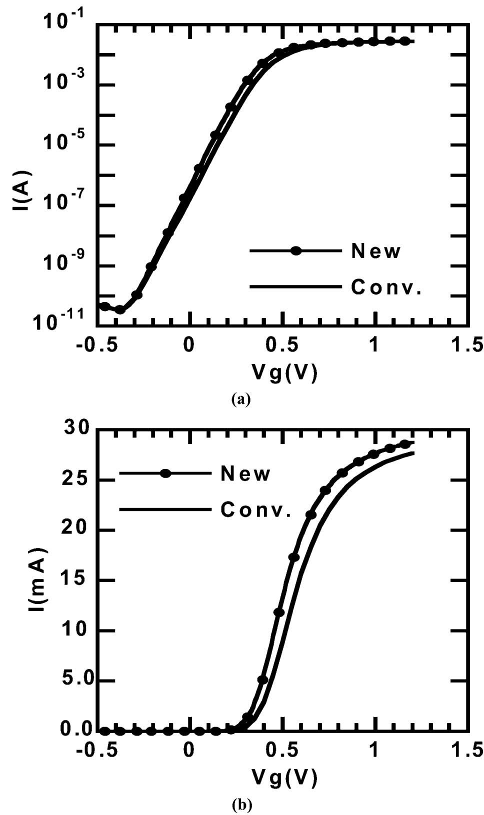


Fig. 7. Comparison of the quasi-static transfer characteristics between the conventional (solid line) and floating-body (line-symbol) devices. The plots are in (a) the log and (b) the linear scales, respectively.

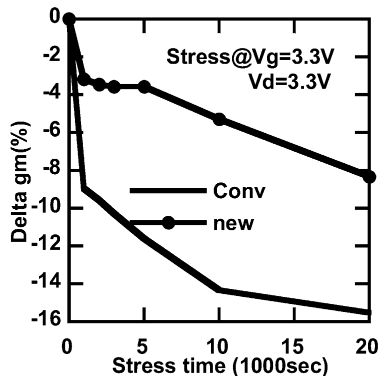


Fig. 8. Comparison of the reliability characteristics between the conventional (solid line) and the new (line-symbol) devices.

is to say that the floating charge effect does not lower the reliability of the floating-body devices but improves the robustness instead. The significance is simply caused by the decrease of the electric field at the drain region. This could be summarized by saying that the excellence will further make the floating-body design more valuable. Due to the success of the fully silicided ESD protection structure, device area could be greatly saved. The area reduction is shown in Table I. The new design requires only about one-third of the conventionally used silicide-blocked ESD device. This is very important for the sub-100-nm device and circuit design, because each micrometer of chip area is extremely valuable for modern gigascale IC design.

TABLE I

COMPARISON OF DIFFERENT AREAS (μm) BETWEEN THE BODY-SWITCHABLE FULLY SILICIDED DEVICES AND CONVENTIONALLY USED SILICIDE-BLOCKED DEVICE. S IS EQUAL TO THE SUMMATION OF DRAIN, SOURCE, AND GATE. R IS THE NORMALIZED RATIO WITH RESPECT TO THE AREA OF THE FULLY SILCIDED DEVICE

Device type	Drain	Source	Gate	S	R
Fully-silcided	0.4	0.4	0.09	0.89	1.0
Silicide blocked	2.0	0.4	0.09	2.49	2.79

In order to efficiently protect the I/O circuit, the turn-on voltage of the protection circuit has to be lower than the breakdown voltage of the gate oxide. However, it is becoming more and more difficult for the conventionally used silicide-blocked ESD devices to protect the gate oxide since its thickness is being reduced rapidly. As we have mentioned above, the turn-on voltage of the parasitic BJT is very close to the breakdown voltage of the gate oxide. Therefore, when considering process variation, the silicide-blocked ESD protection devices will have a high risk in ESD failure. The proposed structure is expected to have an improved efficiency in protection circuit from ESD damages.

Except for the device area and response time, the driving capability is also an important issue when designing the output buffers. The output buffers conventionally are fabricated by using the silicide-blocked devices for ESD robustness. However, the silicide-blocked region will produce a parasitic resistor and lower the driving capability. Our proposed device has a much better driving capability than the conventionally used silicide-blocked ESD protection devices. Furthermore, unlike the silicide-blocked ESD protection devices that require an additional mask and several fabrication processes, the proposal discussed here is totally compatible with the processes of the integrated circuit. A brief summary is drawn that the proposed ESD protection device has a high ESD robustness, low turn-on voltage, high driving capability, superior device reliability, and small device area. This promising technique is compatible with the VLSI process using sub-100-nm CMOS devices.

IV. CONCLUSION

In this paper, the floating charge effect has been considered in the design of new fully silicided NMOSFETs for designing ESD protection circuits consisting of nanodevices. Our investigation into the new fully silicided ESD protection nanodevices has demonstrated that there is a significant improvement in ESD robustness compared with the conventional structures. Furthermore, it has an excellent electrical efficiency when compared with that of drain-ballast resistor-tied devices. Moreover, the proposed methodology has exhibited a higher driving current and better reliability without suffering the off-state current of the fully silicided devices. These electrical characteristics are suitable for the output buffer design in which both driving capability and ESD robustness have to be considered. Additionally, it reduces processes in IC fabrication. The design is useful in novel IC design, in particular, for high-density and high-speed circuits.

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