10-Gb/s Modulator Drivers With Local Feedback Networks

Day-Uei Li and Chia-Ming Tsai

***Abstract*—A novel intrinsic collector-base capacitance (C_{CB}) feedback network (ICBCFN) was incorporated into the conventional cascode and series-connected voltage balancing (SCVB) circuit configurations to implement 10-Gb/s modulator drivers. The drivers fabricated in 0.35-μm SiGe BiCMOS process could generate 9 V_{PP} differential output swings with rise/fall time of less than 29 ps. Also, the ICBCFN was modified as an intrinsic drain-gate capacitance feedback network (IDGCFN) to implement drivers with differential output swing of 8 V_{PP} in 0.18-μm CMOS process. The power consumption is as low as 0.6 W. The present work shows that the driving capability is greater than that of the currently reported Silicon-based drivers.**

***Index Terms*—Intrinsic collector-base capacitance, intrinsic drain-gate capacitance, laser drivers, modulator drivers, silicon-based, 10 Gb/s.**

I. Introduction

EXTERNAL modulators are preferably used to modulate light intensity in long-haul 10-Gb/s fiber-optic communication systems. To ensure sufficient extinction ratio, modulator drivers are required to supply an output swing higher than 3 V_{pp}. Over the past decade, most modulator drivers have been fabricated in compound semiconductors owing to their high-breakdown and high-speed characteristics [1]–[7]. However, most of them are quite inefficient both in the die area and power consumption. To achieve low cost system integration with other digital functional blocks, a driver circuit realized by high-speed transistors with lower breakdown voltage is required. 10–14 Gb/s SiGe HBT drivers with output swings over 3 V_{pp} and 10-Gb/s CMOS drivers with 2.5 V_{pp} output swings have been reported in [8] and [9], respectively. However, it is difficult for such single transistor topology to generate a voltage swing larger than 3.5 V_{pp}. To solve this problem, a series connected voltage balancing (SCVB) topology [4], [10] was introduced to double the breakdown voltage. Mandegaran and Hajimiri [11] modified the SCVB and implemented the driver in 0.18-μm SiGe BiCMOS technology to give a differential output swing of 8 V_{pp}. However, there existed two drawbacks for this design: first, the sophisticated analysis of large signal driver, and second, the power inefficiency.

In this paper, we demonstrate how to implement 10-Gb/s modulator drivers effectively and efficiently in Silicon-based process technology. A novel intrinsic collector-base capacitance feedback network (ICBCFN) was incorporated into the conventional cascode and SCVB circuit configurations at the output stage to implement drivers in 0.35-μm SiGe BiCMOS technology, whereas an intrinsic drain-gate capacitance feedback network (IDGCFN) modified from ICBCFN was used to implement drivers in 0.18-μm CMOS technology. The performances, compared with previous works, are shown in Table I. To illustrate the efficiency of the ICBCFN, the driver

TABLE I
COMPARISON OF MODULATION DRIVERS

Ref.	Tech.	Freq. (Gb/s)	Output Swing (V_{PP})	Supply Voltage (V)	Power (W)	Edge Speed (ps)	Die Area (mm^2)
[1]	AlGaAs/ InGaAs pHEMT 0.2μm	10	6	5.2	1	N/A	7.5
[2]	Ku-pHEMT 0.25 μm	10	14	N/A	2	N/A	7.2
[3]	GaAs pHEMT 0.15 μm	10	14.8	5/ (-3.3)	2.6	N/A	2.1
[4]	InP HEMT 0.1 μm	10	7.2	3.4/ (-7.3)	3.5	16/16	3.4
[5]	InGaP/ GaAs HBT	10	10	10	2.4	50/50	2.4
[6]	InP/ InGaAs DHBT	12	7	5.9	1.6	60/60	1.1
[7]	InP SHBT	12.5	6.2	5.2	1.4	20/18	0.91
[8]	Si HBT f_t = 25 GHz	10–14	7.2	5.2	2.2	N/A	1.32
[9]	CMOS 0.18 μm	10	5	1.8	0.7	N/A	1.62
[11]	SiGe BiCMOS 0.18 μm	10	8	6.5	3.6	40/35	N/A
[12]	CMOS 0.13 μm	20	<1	2.5/3.3	0.12	23/25	N/A
Driver 1	**SiGe BiCMOS 0.35 μm**	**10**	**9**	**3.3/6**	**0.8**	**27/29**	**0.56**
Driver 2	SiGe BiCMOS 0.35 μm	10	6	5	1	26/28	0.80
Driver 3	**CMOS 0.18 μm**	**10**	**8**	**1.8/4**	**0.6**	**42/42**	**0.68**
Driver 4	**CMOS 0.18 μm**	**10**	**6.8**	**1.8/3.5**	**0.4**	**41/41**	**0.4**
Driver 5	**SiGe BiCMOS 0.35 μm**	**10**	**9**	**5/6**	**1**	**25/27**	**0.56**
Driver 5 w/o ICBCFN	SiGe BiCMOS 0.35 μm	10	9	5/6	2	27/29	0.56

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D.-U. Li is with the Industrial Technology Research Institute, 310 Taiwan, R.O.C. (e-mail: davidli@itri.org.tw).

C.-M. Tsai is with the National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

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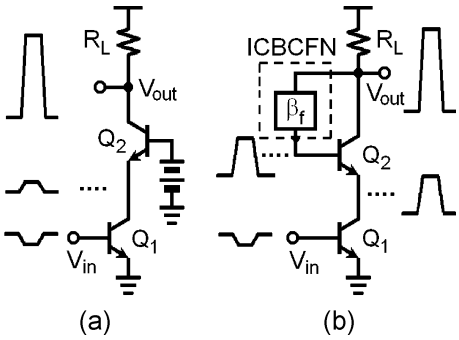

Fig. 1. (a) Conventional cascode driver and (b) that with proposed ICBCFN.

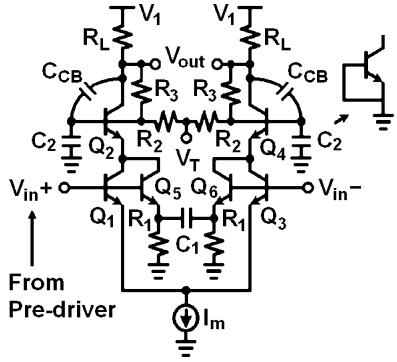

Fig. 2. Proposed driver, driver 1, with ICBCFN.

with SCVB only is also implemented in SiGe BiCMOS technology and the results are also compared. With the advantage of ICBCFN, the power consumption is greatly reduced from 2 W to 1 W. The present work shows the smallest die area with a driving capability greater than the previously reported silicon-based drivers.

II. Circuit Design and Implementation

A. Design Concept

In conventional driver design for large output signals, the output transistor has to sustain the whole output voltage and its size is therefore very large. This limits the achievable output swing and operation speed due to the large parasitic capacitance. One might consider a conventional cascode circuit topology shown in Fig. 1(a) to solve the problem. However, the fixed base voltage of the transistor Q_2, V_{b2}, confines the signal magnitude at the collector of the transistor Q_1. As a result, the output transistor, again, sustains almost the whole output voltage and this also limits the achievable output swing with low breakdown-voltage devices. Fig. 1(b) illustrates the proposed circuit diagram incorporating ICBCFN into a cascode configuration. The design concept is to designate the base voltage V_{b2}, so that it can bear the same phase with the output voltage rather than just being fixed. This goal can be achieved by providing a path to feedback the output voltage to give a proper V_{b2}. Thus, the emitter voltage of the transistor Q_2 follows V_{b2} (characteristics of emitter followers) and its signal magnitude is larger than that of the conventional circuit topology. If the feedback network β_f is properly designed, the two transistors, Q_1 and Q_2, will evenly share the output swing. Therefore, the achievable output swing doubles without compromising the speed. A further advantage of this circuitry compared with a single transistor topology is that it is able to reduce Miller effect due to the lower signal magnitude at collector of Q_1. Thus, a low-power pre-driver can be achieved.

B. Circuit Implementation on SiGe BiCMOS Process

Fig. 2 shows the proposed driver, denoted as Driver 1 hereafter. It comprises a differential cascode output stage, a bandwidth enhancing circuit composed of Q_5, Q_6, R_1, and C_1, and a feedback network composed of C_{CB}, C_2, R_2, and R_3. The resistive feedback comprising R_2 and R_3 is used to provide the low-frequency feedback control, and the capacitive feedback comprising C_{CB} and C_2 is used for the high-frequency part. The choice of C_2 is quite important. Fig. 3 shows how this parameter affects the waveform at the base of Q_2. The quality of the output waveform is acceptable as long as the value of C_2 does not deviate from its optimized window $(0.2C_{2opt} < C_2 < 5C_{2opt})$. A better way to implement $C_2 = C_{2opt}$ to avoid process and temperature variations is to employ a transistor with its base and emitter connected and its size a little bit larger than that of Q_2. Once C_2 is optimized, R_2 and R_3 can be determined to make both high- and low-frequency parts of an output swing shared evenly between Q_1 and Q_2. R_2 and R_3 can be kept much larger for power-saving considerations. In addition, this resistive feedback network can also be properly designed to serve as a back termination network. Thus, the influence of the capacitive feedback becomes negligible due to the resulting wideband characteristic of the resistive feedback. Fig. 4 shows the collector-emitter voltage of Q_1 and Q_2, respectively, in conventional cascode topology with and without ICBCFN. It is clear that in our proposed driver Q_1 and Q_2 share equal voltage swing, whereas in conventional cascode driver Q_2 shares most of the swing. The conventional cascode topology is just like another single-transistor type driver and it is not reliable to implement modulator drivers. The bandwidth enhancing circuit not only enhances the bandwidth but also provides appropriate bias currents to both Q_2 and Q_4. Finally, V_T is used for DC control and can be simply connected to the same supply voltage used for pre-driver for convenience. In this design, V_T is 3.3 V. To illustrate the efficiency of the cascode configuration with ICBCFN, we have also implemented a single-transistor topology driver,

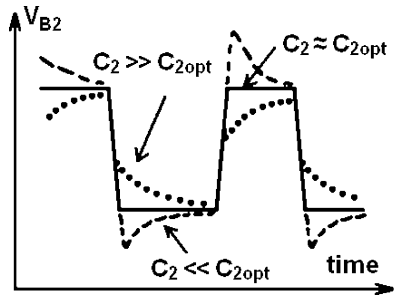

Fig. 3. Base voltage of Q_2 for different values of C_2 with R_2 and R_3 fixed.

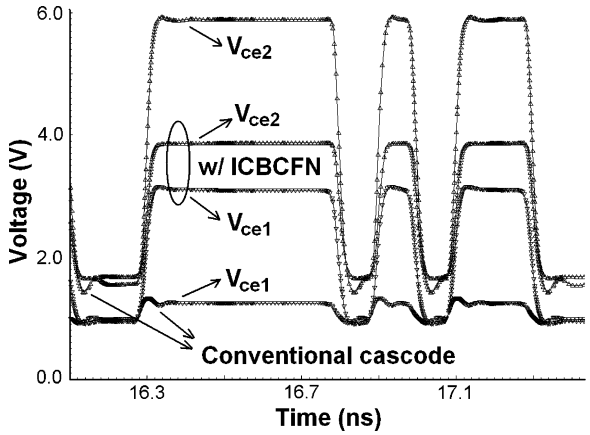

Fig. 4. Collector-emitter voltage of transistors Q_1 and Q_2 with and without ICBCFN.

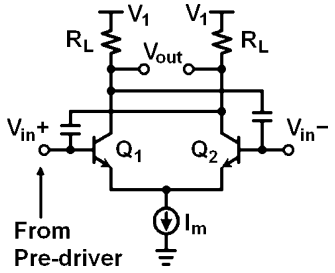

Fig. 5. Single-transistor type driver, driver 2.

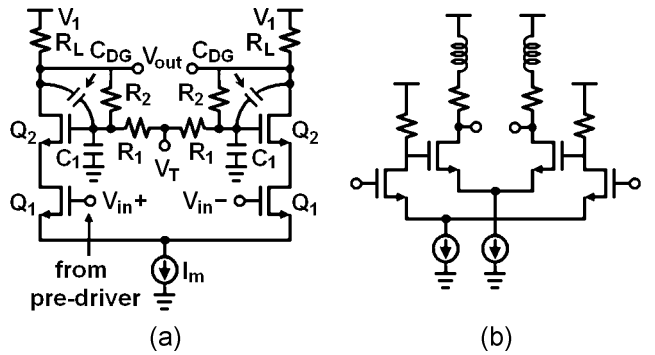

Fig. 6. (a) Proposed CMOS driver, driver 3 with IDGCFN and (b) pre-driver with peaking inductors.

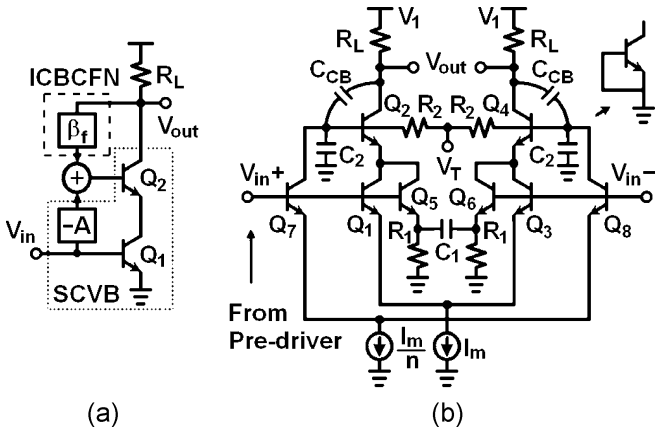

Fig. 7. (a) ICBCFN incorporated into SCVB and (b) driver 5.

denoted as Driver 2 hereafter, in 0.35-μm SiGe BiCMOS technology as shown in Fig. 5.

C. Circuit Implementation on CMOS Process

The concept of ICBCFN is also applicable to implementing drivers in CMOS technology. Fig. 6(a) shows the proposed CMOS driver, denoted as Driver 3 hereafter. However, the breakdown-voltage of CMOS devices shrinks as the size of transistors scales down. Therefore, we have to modify the designing procedure used in SiGe BiCMOS technology by sharing the output swing between the two transistors, $\mathrm{Q_1}$ and $\mathrm{Q_2}$, in proportion to their breakdown voltages $\mathrm{V_{br1}}$ and $\mathrm{V_{br2}}$, respectively. To generate a higher voltage swing, the transistor $\mathrm{Q_2}$ should be a high-voltage device sustaining a higher voltage swing, while the transistor $\mathrm{Q_1}$ is a low-voltage device sustaining a lower voltage swing for a smaller Miller effect, thus maintaining the speed. The key point of the design concept is to focus on controlling a proper $\mathrm{V_{g2}}$. The driver circuit comprises a differential cascode output stage and a feedback network composed of $\mathrm{C_{DG}}$, $\mathrm{C_1}$, $\mathrm{R_1}$, and $\mathrm{R_2}$. Again, the quality of the output waveform is acceptable as long as the value of $\mathrm{C_1}$ does not deviate from its optimized window. Once $\mathrm{C_1}$ is optimized, $\mathrm{R_1}$ and $\mathrm{R_2}$ can be determined to make both high- and low-frequency parts of an output swing shared proportionally between $\mathrm{Q_1}$ and $\mathrm{Q_2}$. Fig. 6(b) shows the pre-driver. To have a better speed performance, an inductor is inserted between the load and the power supply for peaking.

In this design, $\mathrm{V_T}$ is 1.8 V. For comparison, we also implement a driver, denoted as Driver 4 hereafter, in which both the transistors $\mathrm{Q_1}$ and $\mathrm{Q_2}$ are low-voltage devices. The output swing is predicted to be less than that of Driver 3, but the power consumption is lower.

D. ICBCFN Incorporated Into SCVB

Fig. 7(a) illustrates the proposed design concept that incorporates ICBCFN into the SCVB configuration. Both a feed-forward gain stage and an output feedback network are used to generate a proper base voltage $\mathrm{V_{b2}}$. Fig. 7(b) shows the proposed driver, denoted as Driver 5 hereafter. It comprises a differential cascode output stage, a differential gain stage, a bandwidth enhancement circuit, and a capacitive feedback network. The differential gain stage, which comprises $\mathrm{Q_7}$, $\mathrm{Q_8}$ and $\mathrm{R_2}$, is designed to provide the drive voltage with magnitude one half of the output swing $\mathrm{R_2 \cdot I_m}/n = \mathrm{R_L \cdot I_m}/2$, where $\mathrm{I_m}$ is the modulation current and n is the current ratio. In addition, owning to the large size of $\mathrm{Q_2}$ and $\mathrm{Q_4}$, $\mathrm{R_2}$ must be kept small to ensure that the drive signal is fast enough to track the output response. Thus, it demands large devices for both $\mathrm{Q_7}$ and $\mathrm{Q_8}$ to provide a large current drive capability. As a result, the power dissipation in both of the pre-driver and the differential gain stage significantly increases. A simple approach to alleviate the problem is to utilize the high-frequency feedback network comprising $\mathrm{C_{CB}}$ and $\mathrm{C_2}$. With this high-frequency signal path, the differential gain stage can be treated as just a low-frequency signal generator. As a result, $\mathrm{R_2}$ can be much larger and the current consumption of the gain stage can thus be greatly reduced from 90 mA to only 7.5 mA (n from 1 to 12), and that of the pre-driver can be

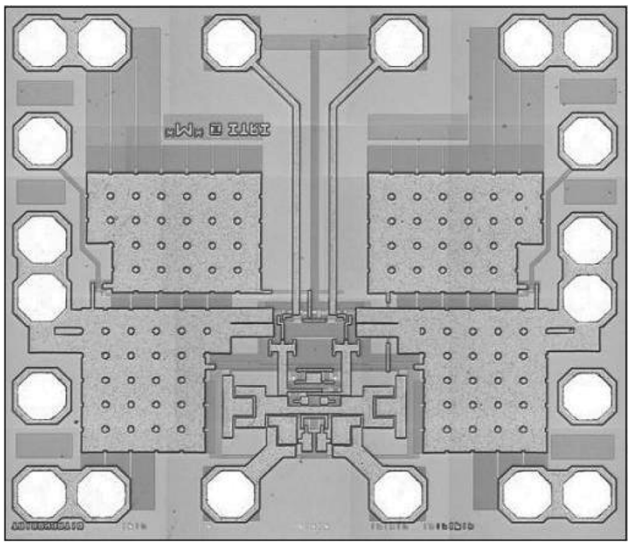

Fig. 8. Die photomicrograph of driver 1.

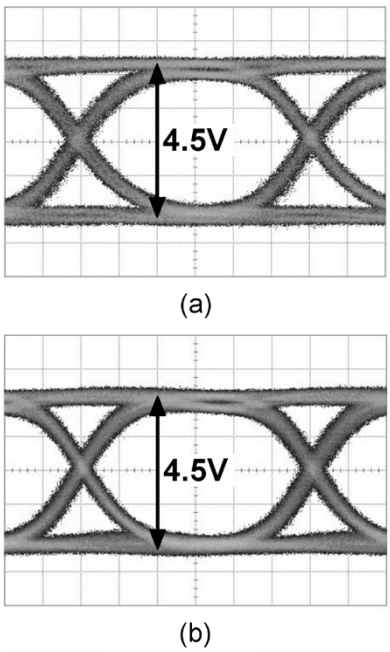

Fig. 9. Measured eye diagrams for (a) driver 1 and (b) driver 5 at 10 Gb/s. Vertical: 1 V/div; horizontal: 16 ps/div.

reduced to half of its original value. The total power consumption therefore is reduced from 2 W to 1 W. To avoid process and temperature variations, the capacitor C_2 is implemented by employing a transistor with its base and emitter connected together and its size a little larger than that of Q_2. In this design, V_T is 5 V.

III. Chip-on-Board Test Results

Driver 1, Driver 2, and Driver 5 were implemented in 0.35-μm SiGe BiCMOS technology, whereas Driver 3 and Driver 4 were in 0.18-μm CMOS technology. All drivers were tested in chip-on-board assemblies at 10-Gb/s. Each driver IC included a pre-driver with optimized performance. The output load for all drivers was 50 Ω. A 20-dB attenuator was

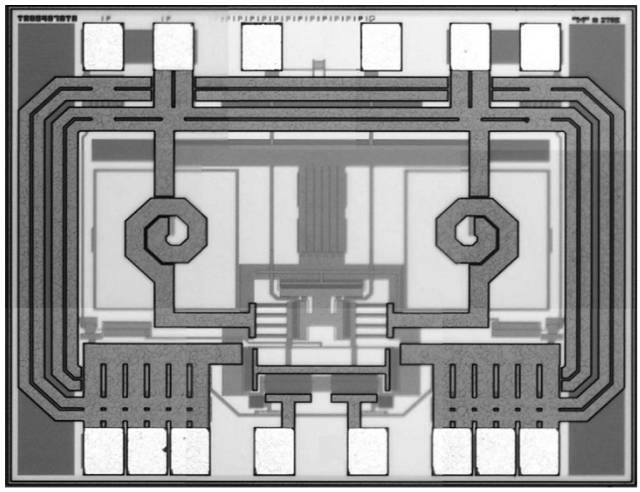

Fig. 10. Die photomicrograph of driver 3.

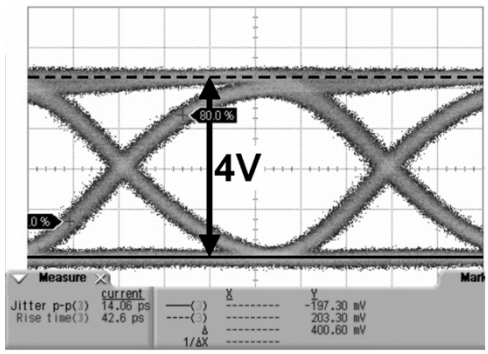

Fig. 11. Measured eye diagram of driver 3 at 10 Gb/s.

added to avoid overloading the high-speed oscilloscope. Fig. 8 shows the die micrograph of Driver 1. The IC occupies a chip area of 800×700 μm^2 and the active die area is smaller than 300×200 μm^2. The input data stream was a 500 $\mathrm{mV_{PP}}$ $2^{31}-1$ non-return-to-zero (NRZ) pseudorandom bit sequence (PRBS). A wideband bias-T was employed to establish a common-mode level of 6–7 V at the driver output. Fig. 9(a) and (b) show the measured electrical eye diagrams of Driver 1 and Driver 5, respectively. They both showed good characteristics at 10 Gb/s.

Both driver ICs achieved a single-ended output swing of 4.5 $\mathrm{V_{PP}}$. The rise/fall times of Driver 1 and Driver 5 were 27/29 ps and 25/27 ps, with jitters of 15 $\mathrm{ps_{PP}}$ and 13 $\mathrm{ps_{PP}}$, and power consumptions of 0.8 W and 1 W, respectively. The measured BER at single-ended input amplitude larger than 100 $\mathrm{mV_{PP}}$ is less than 10^{-11}. Fig. 10 shows the die micrograph of Driver 3. The IC occupies a chip area of 900×750 μm^2. The input data stream was an 800 $\mathrm{mV_{PP}}$ $2^{31}-1$ NRZ PRBS. A wideband bias-T was employed to establish a common-mode level of 4–5 V at the driver output. Fig. 11 shows the measured electrical eye diagram at 10 Gb/s. A single-ended (S.E.) output swing of 4 $\mathrm{V_{PP}}$ was achieved with power consumption as low as 0.6 W. The jitter was 14 $\mathrm{ps_{PP}}$. The measured BER at input amplitude larger than 800 $\mathrm{mV_{PP}}$ is less than 10^{-11}. A comparison with some previously reported silicon-based modulator drivers is given in Table I. Driver 3 could be used as a laser driver when a 75-Ω off-chip termination resistor was connected from the

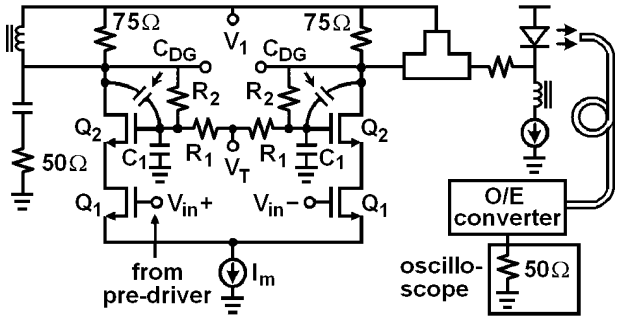

Fig. 12. Optical measurement setup block diagram.

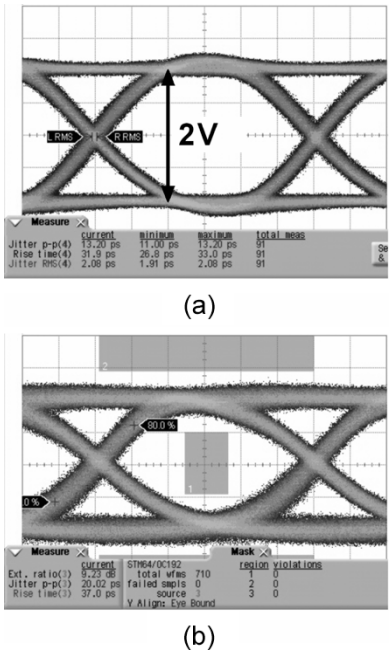

Fig. 13. (a) Electrical and (b) filtered optical eye diagrams for driver 3 for 10 Gb/s.

output end to common-mode level V_1. Fig. 12 shows the block diagram of 10-Gb/s optical measurement setup. The driver directly modulates a commercial 1310-nm-wavelength MQW DFB laser diode. A golden 1310-nm O/E converter receives optical data streams emitted from the laser. Fig. 13(a) shows the electrical eye diagram for single-ended output swing of 2 V_{PP} at 10 Gb/s. Fig. 13(b) shows the corresponding optical eye diagram filtered with a 10-Gb/s fourth-order Bessel–Thomson filter, overlaid with the STM-64/OC-192 transmitter optical eye mask. It is clear that the optical eye stays well within the STM-64/OC-192 transmitter mask.

IV. Jitter Analysis

Theoretical random jitter analysis for broadband amplifiers has been derived in [13]. However, to measure an accurate random jitter data, we need an elaborate process to exclude the oscilloscope trigger-delay jitter. From [14], the more accurate signal voltage is equal to $V_{signal} - SR_{signal} \cdot (V_{clk} - V_{clk\_AVG})/SR_{clk}$, where V_{signal} and SR_{signal} represent the measured voltage and the slew rate of the output signal of the drivers, and V_{clk}, V_{clk_AVG}, and

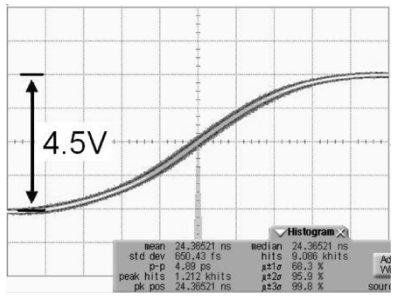

Fig. 14. Measured output signal histogram of driver 1.

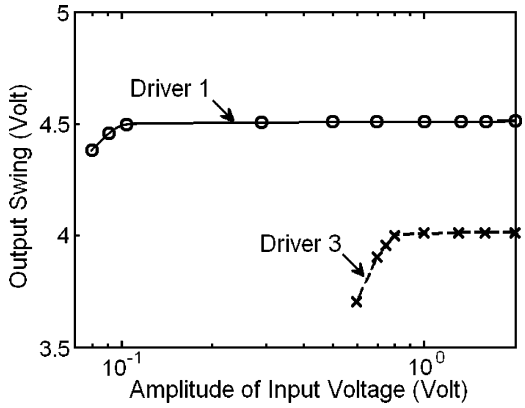

Fig. 15. Measured output amplitude.

SR_{clk} represent the measured voltage, the measured voltage in average mode, and the slew rate of the reference clock used to exclude to trigger-delay jitter, respectively. Choosing the data out of the pattern generator to be a one zero pattern, and after a process described in [14], the device-under-test (DUT) signal without any trigger-delay jitter is obtained. Fig. 14 shows a measured output signal histogram of Driver 1. From this oscilloscope reading the random jitter measurement of the DUT signal is about 0.65 ps_{RMS} and 4.9 ps_{PP}. This measurement has trigger-delay jitter removed.

Fig. 15 shows the measured (S.E.) output amplitudes versus amplitude of input voltage. It is clearly that Driver 1 has wider input dynamic range and has better sensitivity owning to the larger g_m of SiGe BiCMOS devieces.

Fig. 16 shows the measured rms output jitter of Driver 1 and Driver 3 versus the amplitude of input voltage with one zero pattern. The Driver 1 maintains a 4.5 V_{PP} S.E. output amplitude across a wide range of input signal levels (100 mV_{PP} to 2 V_{PP}), whereas the Driver 3 maintains 4 V_{PP} S.E. output amplitude in range from 800 mV_{PP} to 2 V_{PP}. The random jitters of both drivers are less than 0.7 ps_{RMS} within the valid input range.

V. Conclusion

In this paper, 0.35-μm SiGe BiCMOS and 0.18-μm CMOS modulator drivers with low power and high output swings were proposed. The measured eye diagram shows good characteristics at 10 Gb/s. The novel ICBCFN and the advantage of cascode topology allows the power consumption to be only 0.8 W and the differential output swing to be 9 V_{PP} with a jitter less than 15 ps_{PP}. It can also be applied to the SCVB circuit topology to

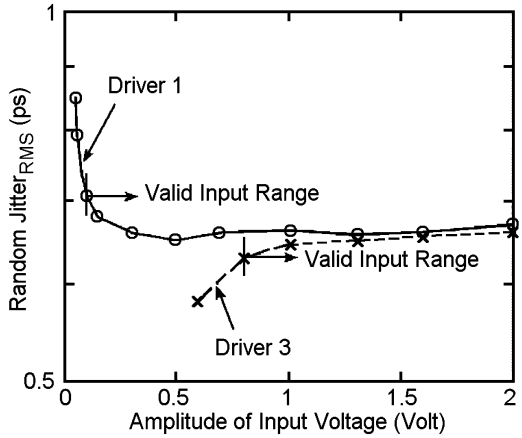

Fig. 16. Measured rms output jitter of driver 1 and driver 3 versus the amplitude of input voltage.

implement drivers with a differential output swing of 9 V_{PP} and a jitter less than 13 ps_{PP}. The power consumption is greatly reduced from 2 W with SCVB to only 1 W. The ICBCFN was modified as an IDGFN to implement drivers in CMOS technology. The power consumption is only 0.6 W and the differential output swing is 8 V_{PP} with a jitter less than 14 ps_{PP}. The random jitters for both type of drivers are less than 0.7-ps_{RMS}. The drivers could be used as a laser driver when a 75-Ω off-chip termination resistor was used. The measured BERs are less than 10^{-11} within the valid input range. The measured optical eye diagram stays well within the 10-Gb/s Ethernet transmitter mask. To the knowledge of the authors, the proposed drivers consume the lowest power and occupy small areas with a differential output swing of over 8 V_{PP}, and the output swing spans more widely than the previously reported silicon-based modulator drivers.

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Day-Uei Li was born in Chiayi, Taiwan, R.O.C., on May 6, 1970. He received the B.S. degree from the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, in 1992, and the Ph.D. degree from the same university in 2000.

In 2001, he joined SoC Technology Center, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, where he is presently working on high-speed physical layer circuits for fiber-optic communication systems and high-speed A/D converters for ultra-wideband communication systems. His current research interests include finite element methods, the development of numerical methods for modeling optical waveguides and waveguide devices, and mixed-signal IC design.

Chia-Ming Tsai was born in Tainan, Taiwan, R.O.C., in 1967. He received the M.S. and Ph.D. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1991 and 1997, respectively.

He then joined the Opto-Electronics and Systems Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, as a designer for optoelectronic devices. In 2000, he joined the SoC Technology Center, ITRI, as an analog IC designer. Since July 2005, he has been with the Department of Electronics Engineering of National Chiao-Tung University as an Assistant Professor. His research interests are in the area of high-speed integrated circuits and optoelectronic devices. He is currently working on analog front-end design for fiber communication applications.