High-Performance Poly-Silicon TFTs Using HfO_2 Gate Dielectric

Chia-Pin Lin, *Student Member, IEEE*, Bing-Yue Tsui, *Senior Member, IEEE*, Ming-Jui Yang, Ruei-Hao Huang, and Chao-Hsin Chien, *Associate Member, IEEE*

***Abstract*—High-performance low-temperature poly-Si thin-film transistors (TFTs) using high-κ (HfO_2) gate dielectric is demonstrated for the first time. Because of the high gate capacitance density and thin equivalent-oxide thickness contributed by the high-κ gate dielectric, excellent device performance can be achieved including high driving current, low subthreshold swing, low threshold voltage, and high ON/OFF current ratio. It should be noted that the ON-state current of high-κ gate-dielectric TFTs is almost five times higher than that of SiO_2 gate-dielectric TFTs. Moreover, superior threshold-voltage (V_{th}) rolloff property is also demonstrated. All of these results suggest that high-κ gate dielectric is a good choice for high-performance TFTs.**

***Index Terms*—Hafnium dioxide (HfO_2), high dielectric-constant dielectric, thin-film transistors (TFTs).**

I. Introduction

LOW-TEMPERATURE poly-Si (LTPS) thin-film transistors (TFTs) have been used as pixel and driving ICs in active-matrix liquid crystal displays (AMLCDs) [1]. Recently, to realize system-on-panel (SOP), integrating driving ICs on the glass substrate are required [2]. However, it is a challenge to develop high-performance TFTs for both pixel TFTs and driving circuits [3]. To drive the liquid crystal, pixel TFTs operate at high voltages with low gate-leakage currents. In contrast, high-speed display driving circuits require TFTs to operate at low voltages and high driving currents, with a low threshold voltage. Using a thin gate oxide can increase the driving current of TFTs. Unfortunately, for a conventional gate dielectric (i.e., SiO_2 or Si_3N_4), a thinner gate dielectric may induce higher gate-leakage current and degrade the TFT characteristics significantly [4]. In the previous studies, to preserve the physical gate-dielectric thickness while increasing the gate capacitance density and then improving the mobile carrier density in the channel region, several new high-κ gate-dielectric materials including Al_2O_3 and Ta_2O_5 were suggested [5], [6]. However, the κ value of Al_2O_3 is 9–10 and is not high enough, and the improvement of the device performance is not apparent [7]. On the other hand, due to narrowbandgap, it is necessary to use a thick Ta_2O_5 as gate dielectric in TFTs to reduce the gate-leakage current [8]. Therefore, the increase of gate capacitance density is limited. Recently, hafnium dioxide (HfO_2) becomes a candidate of future high-κ gate-dielectric material in MOSFET due to its high-κ value (~ 25), widebandgap, acceptable band alignment, and superior thermal stability with poly-Si [9], [10]. In this paper, we integrated high-κ HfO_2 gate dielectric with TFTs for the first time.

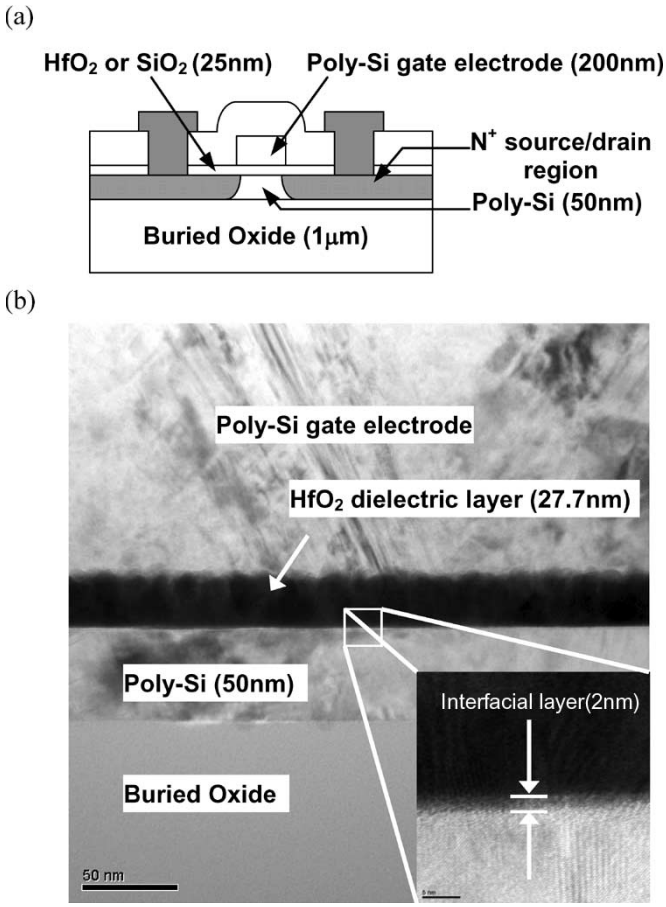

Fig. 1. Cross-sectional (a) drawing and (b) TEM of the proposed high-κ HfO_2 gate-dielectric TFT structure.

II. Device Fabrication

Fig. 1(a) and (b) shows the schematic drawing of the HfO_2 gate-dielectric TFT and the cross-sectional transmission electron microscopy (TEM) micrograph of the gate structure, respectively. The fabrication started by depositing a 50-nm amorphous Si (α-Si) layer at 550 °C in a low-pressure

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C.-P. Lin and B.-Y. Tsui are with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: cplin.ee90g@nctu.edu.tw).

M.-J. Yang, R.-H. Huang and C.-H. Chien are with the National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C.

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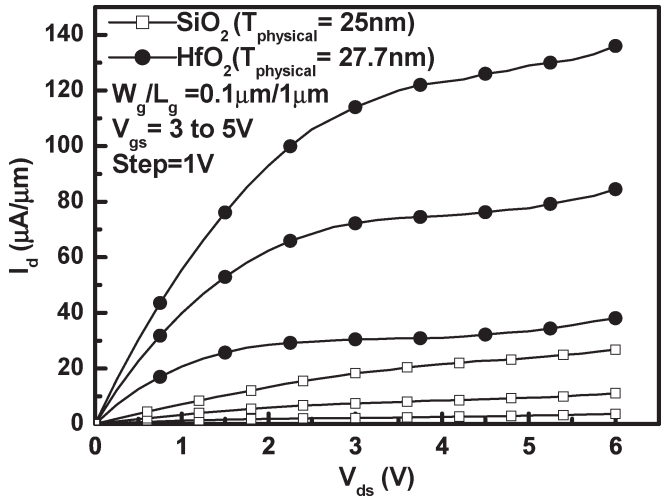

Fig. 2. Output characteristics of the TFTs using HfO_2 or SiO_2 as gate dielectric.

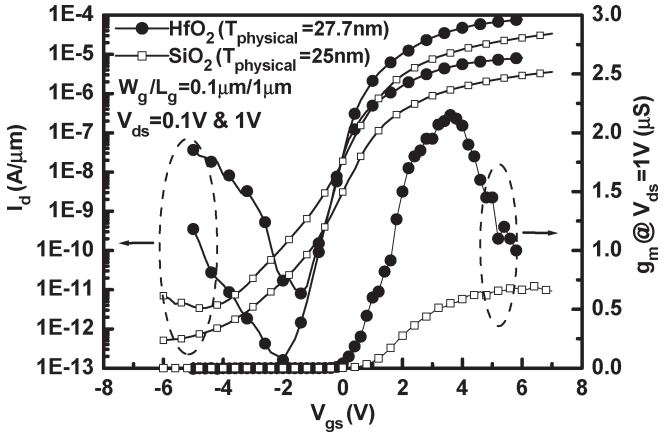

Fig. 3. Transfer characteristics of the TFTs using HfO_2 or SiO_2 as gate dielectric.

TABLE I
DEVICE PARAMETERS OF TFTS WITH 27.7-nm HfO_2 OR 25-nm SiO_2 AS GATE DIELECTRIC AT $V_{\rm ds} = 0.1$ V

Gate dielectric	V_{th}(V)	S.S. (V/Dec)	μ_{FE}(cm^2/V-sec)	I_{on}/I_{off} (@ V_{ds}=1V)
HfO_2 ($T_{physical}$=27.7 nm) (EOT=7.3 nm)	0.3	0.28	39	9.7x10^6
LPCVD SiO_2 ($T_{physical}$=25 nm) (EOT=31 nm)	1.2	0.64	50	5.4x10^6

chemical vapor deposition (LPCVD) system on Si wafers capped with a 1-μm thick thermal oxide layer. The deposited α-Si layer was then recrystallized by solid phase crystallization (SPC) process at 600 °C for 24 h in a N_2 ambient. Next, in order to fabricate narrow-width devices to enhance the gate controllability and reduce the influence of grain-boundary defects, electron beam lithography (EBL) and reactive ion etching (RIE) were used to pattern the device active islands [11], [12]. The narrowest channel width is 0.1 μm. Then, after removing the native oxide by dipping in diluted hydrofluoric acid (HF) solution, an HfO_2 thin film was deposited in a metal–organic CVD (MOCVD) system at 400 °C as gate dielectric. Oxygen and Argon were used as reactant and transmission gases with flow rates of 1000 and 200 sccm, respectively. The total pressure in the chamber is fixed at 5 mbar and the injection frequency is 3 Hz. Another 200-nm α-Si layer was deposited at 550 °C in an LPCVD system and then was patterned to form gate electrode. Because of the thermal budget during the α-Si gate deposition, the thick amorphous HfO_2 layer became polycrystalline structure, and then formed the rough top interface between gate electrode layer and HfO_2 film. Next, a self-aligned phosphorous ion implantation was performed at 60 keV to a dose of 5×10^{15} cm^{-2} to dope source/drain region and gate electrode. After a 300-nm-thick HF passivation layer was deposited by a plasma-enhanced CVD (PECVD) system at 300 °C, the contact holes were patterned by a two-step wet-etching process. First, the 300-nm oxide layer was etched by buffered oxide etch (BOE) solutions. Then, to raise the HfO_2/SiO_2 selectivity, the HfO_2 films were etched by an isopropyl alcohol (IPA):HF mixture [13]. Additional annealing for dopants' activation was performed at 600 °C for 12 h in an N_2 ambient. Finally, typical Al metallization completed the fabrication process. In order to enhance the device performance, an NH_3 plasma treatment at 350 °C for 30 min was performed to passivate the defect states before measurements [14]. For comparison, poly-Si TFTs with a 25- and 45-nm tetra-ethoxysilane (TEOS) SiO_2 deposited by an LPCVD system were also fabricated with the same process flow.

Device performance was measured using an Agilent 4156 C semiconductor parameter analyzer and an Agilent 4284 A impedance analyzer. The threshold voltage is defined as the gate voltage at which the drain current reaches 100 nA $* W_g/L_g$, where L_g is the drawn channel length and W_g is the drawn channel width. Effective mobility is extracted from the maximum transconductance (g_m).

III. RESULTS AND DISCUSSION

According to Fig. 1(b), the physical thickness of HfO_2 films is equal to 27.7 nm, and the interfacial SiO_2-like layer is about 2 nm [15]. The equivalent-oxide thickness (EOT) and the effective dielectric constant of HfO_2 are extracted to be 7.3 and 20.4 nm, respectively [16]. Fig. 2 shows the typical $I_d - V_{\rm ds}$ for the HfO_2 and SiO_2 TFTs with the same physical gate-dielectric thickness $(T_{\rm physical})$ of 27.7 and 25 nm, respectively. The drawn channel length (L_g) and channel width (W_g) are 1 μm and 0.1 μm, respectively. Obviously, the driving current of HfO_2 TFT (about 136 μA/μm) is five times higher than that of SiO_2 TFT (about 26.7 μA/μm) at $V_{\rm ds} = 6$ V and $V_{\rm gs} = 5$ V. Fig. 3 depicts the transfer characteristics of HfO_2 and SiO_2 TFTs at $V_{\rm ds} = 0.1$ and 1 V. The measured as well as extracted device parameters are summarized in Table I. As the gate dielectric of SiO_2 is replaced by HfO_2, $V_{\rm th}$ decreases from 1.2 to $\sim$ 0.3 V, S.S. decreased from 0.64 to 0.28 V/Dec,

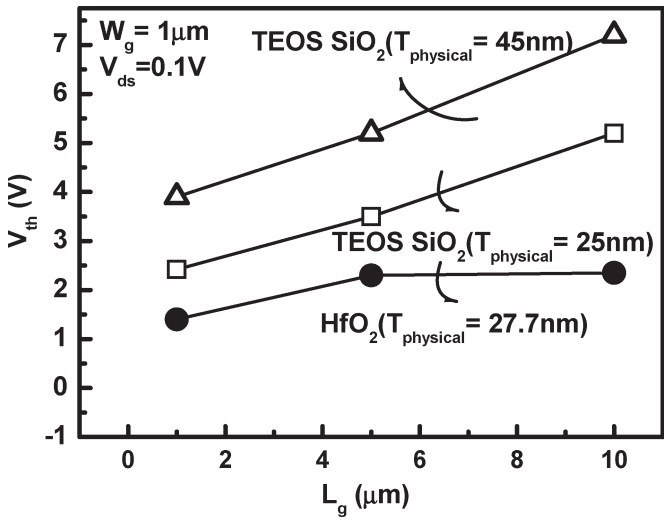

Fig. 4. Threshold-voltage rolloff of poly-Si TFTs with HfO_2 ($T_{\rm physical} = 27.7$ nm) and SiO_2 ($T_{\rm physical} = 25$ or 45 nm) at $V_{\rm ds} = 0.1$ V.

and $I_{\rm on}/I_{\rm off}$ increased from 5.4×10^6 to 9.7×10^6. The gate-leakage current density of HfO_2 TFTs is about 1 μA/cm^2 at $V_{\rm gs} = 5$ V and is lower than that of SiO_2 TFTs by more than two times. The high gate capacitance density resulted from the high-κ gate dielectric could effectively improve the performance of HfO_2 TFTs. Moreover, for devices with the same EOT, the drawback of high gate-leakage current density of HfO_2 devices could be improved more effectively than that of SiO_2 ones because of the thicker physical thickness of HfO_2 [17], [18]. The EOT of HfO_2 TFTs at ON-state is only 7.3 nm. Possible reasons for the slightly low-κ value of 20.4 are the poly-Si gate depletion owing to the low activation temperature and the interfacial layer between HfO_2 and Si channel [19], [20]. The slightly lower effective mobility of HfO_2 TFTs may be due to the additional scattering from HfO_2 dielectric. The OFF-state current of the HfO_2 TFTs increases more rapidly than that of the SiO_2 TFTs as the gate voltage decreases continuously. This phenomenon is explained by the higher electric field near the drain side due to thinner EOT of the HfO_2 TFTs. It could be relaxed by lightly doped drain (LDD) or gate overlapped lightly doped drain (GOLDD) structures [21], [22].

To examine the short-channel effect of TFTs with different gate dielectrics, the threshold-voltages ($V_{\rm th}$) rolloff of HfO_2 and SiO_2 TFTs are compared in Fig. 4. For poly-Si TFTs, the threshold-voltage rolloff is dominated by the decreasing of number of grain boundary as the devices scale down [23]. For the long-channel poly-Si TFTs, the large number of grain boundaries in the channel raises the threshold voltage and degrades the effective mobility [24]. The HfO_2 TFTs with ultrathin EOT and large gate capacitance density can speedily fill the trap states at grain boundary and turn on the devices fast; therefore, not only release the grain-boundary effect but also lower the threshold voltage effectively.

IV. Conclusion

High-performance TFTs with HfO_2 as gate dielectric, which provide thin EOT and high gate capacitance density are demonstrated for the first time. Compared to the TFTs with SiO_2 as gate dielectric, the electrical characteristics including the threshold voltage, subthreshold swing, ON/OFF current ratio, carrier mobility, as well as $V_{\rm th}$ rolloff are effectively improved. These results suggest that HfO_2 is a good candidate to serve as a gate-dielectric material for high-performance poly-Si TFTs.

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