Two-Frequency C–V Correction Using Five-Element Circuit Model for High-k Gate Dielectric and Ultrathin Oxide

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***Abstract*—A new circuit model of five elements has been proposed for the two-frequency capacitance–voltage (C–V) correction of high-k gate dielectric and ultrathin oxide. This five-element circuit model considered the static and dynamic dielectric losses in a lossy MOS capacitor, the parasitic well/substrate resistance, and the series inductance in the cables and probing system. Each of the circuit elements could be easily extracted from the two-frequency C–V and static current–voltage (I–V) measurements if some criteria are well satisfied. In addition, this model can also be transformed into another two four-element circuit models to simplify the analysis and calculations, depending on the gate leakage current.**

***Index Terms*—High-k dielectric, MOS capacitor, two-frequency capacitance–voltage (C–V) correction, ultrathin oxide.**

I. Introduction

With the rapid progress of very large scale integration (VLSI) technologies, the gate dielectric thickness continues to scale down to ensure the device performance in great advance. The gate dielectric capacitance of advanced devices is of great importance for obtaining the equivalent oxide thickness (EOT), inversion layer charge, and interface state density. However, the tunneling current through ultrathin gate oxides may lead to difficulties in performing the quasi-static and typical 100-kHz capacitance–voltage characterizations. Although the problem of severe capacitance drop under large tunneling current can be improved by measuring at higher frequencies ($\geq$ 1 MHz), the influences of parasitic components on the measured capacitance must be taken into account at such high frequencies.

The series resistance R_s arising from the well/substrate and the contact resistance was first added to the parallel circuit model (C_p–G), and a two-frequency capacitance–voltage (C–V) correction method was proposed to extract the accurate dielectric capacitance from this three-element circuit model [1], [2]. In practice, the validity of this correction method seems to depend upon the two frequencies adopted and the device area. The applicability limits of this two-frequency C–V correction method had been further examined in terms of frequency and device area selection guidelines [3]. Later, some researchers recommended that the dielectric energy absorption and other parasitic components should be considered as well. An improved two-frequency method of capacitance measurement using a four-element circuit model was proposed for the $SrTiO_3$ high dielectric constant (high-k) dielectrics [4]. The shunt resistance was replaced by the loss tangent $\tan\delta$ (or called the dissipation factor) due to the dynamic dielectric loss of high-k dielectrics, and series inductance was added due to cables and the probing system. In addition, a new C–V correction method using another four-element circuit model to extract the EOT of ultrathin gate dielectrics with high gate leakage current was also proposed [5]. The shunt resistance was to simulate the static dielectric loss from the gate leakage current, and the parasitic capacitance in parallel with R_s was added due to the device structure, probe contact arrangement, and stray cable capacitance. In this work, a new five-element circuit model has been proposed to consider both the dielectric imperfections and the parasitic components, and this circuit model could also be transformed into another two four-element circuit models to simplify the analysis and calculations, depending on the gate leakage current.

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II. General Circuit Model of Five Elements

Fig. 1(a) shows the two-element parallel circuit model used for a typical C–V characterization in an impedance meter. However, this simple parallel circuit model may not be enough to describe the behavior of the small-signal frequency response of ultrathin oxides and high-k gate dielectrics in various situations. Therefore, a more general circuit model of five elements as shown in Fig. 1(b) is proposed to be employed in the two-frequency C–V correction. In this five-element circuit model, C_0 is the ideal dielectric capacitance, R_p is the shunt resistance due to gate leakage current, $\tan\delta$ is the loss tangent due to dielectric energy absorption, R_s is the series resistance due to well/substrate and contact resistance, and L_s is the series inductance due to extension cables and the probing system. It seems to have two types of dielectric losses in a lossy MOS capacitor, namely, 1) the static dielectric loss due to the actual flow of charge carriers, and 2) the dynamic dielectric loss due to the local movements of atoms or molecules in an alternating electric field.

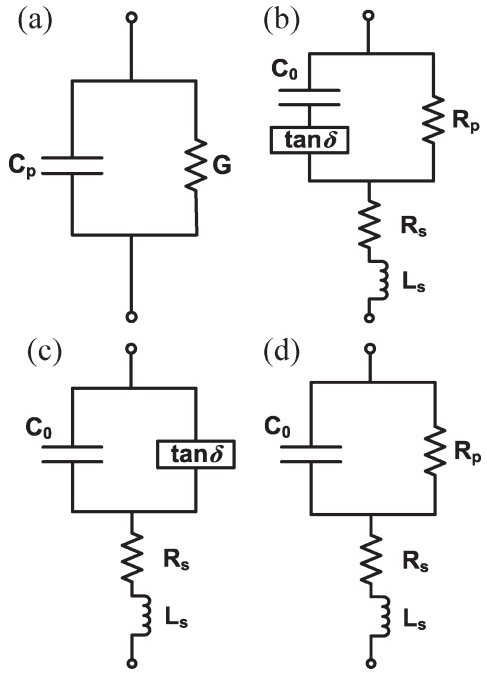

Fig. 1. Small-signal equivalent circuit models of MOS capacitors. (a) Simple parallel circuit model. (b) New five-element circuit model. (c) Four-element circuit model for low leakage high-k dielectrics. (d) Four-element circuit model for ultrathin oxides and leaky high-k dielectrics.

Equating the real and imaginary parts of the total impedance in Fig. 1(a) and (b) results in

$$\text{Real}: \quad \frac{G}{G^2+\omega^2C_p^2} = R_s + \frac{R_p(1+\tan^2\delta+\omega C_0R_p\tan\delta)}{1+(\omega C_0R_p+\tan\delta)^2} \tag{1}$$

$$\text{Imaginary}: \quad \frac{C_p}{G^2+\omega^2C_p^2} = -L_s + \frac{C_0R_p^2}{1+(\omega C_0R_p+\tan\delta)^2}. \tag{2}$$

The above two equations could be simplified for easy algebraic operations if the criteria $\tan^2\delta \ll 1 \ll (\omega C_0R_p)^2$ are satisfied, i.e.,

$$\text{Real}: \quad \frac{G}{G^2+\omega^2C_p^2} = R_s + \frac{\tan\delta}{\omega C_0} + \frac{1}{\omega^2C_0^2R_p} \tag{3}$$

$$\text{Imaginary}: \quad \frac{C_p}{G^2+\omega^2C_p^2} = -L_s + \frac{1}{\omega^2C_0}. \tag{4}$$

If R_p is defined as V_g/I_g from the static I_g-V_g measurement since $R_p \gg R_s$ is valid in most cases, the above criteria could be rearranged as $\tan\delta < 0.1$ and $J_g < 0.01$ A/cm^2 for quick verification. In addition, C_0 and the other three circuit elements could be easily solved from (3) and (4) with the known R_p by measuring C_p and G in parallel mode at two different frequencies, i.e.,

$$C_0 = \frac{\left(\omega_2^2-\omega_1^2\right)\left(G_1^2+\omega_1^2C_{p1}^2\right)\left(G_2^2+\omega_2^2C_{p2}^2\right)}{\omega_1^2\omega_2^2\left[C_{p1}\left(G_2^2+\omega_2^2C_{p2}^2\right)-C_{p2}\left(G_1^2+\omega_1^2C_{p1}^2\right)\right]}. \tag{5}$$

When it comes to the high-k dielectrics with low gate leakage current, R_p could almost be regarded as infinity (open circuit), and $\tan\delta$ in series with C_0 could be transformed into the equivalent one in parallel. This four-element circuit model, as shown in Fig. 1(c), is the one proposed by Lue *et al.* for $SrTiO_3$ high-k dielectrics [4]. Equations (3) and (4) can be applied to their model if the $1/\omega^2C_0^2R_p$ term in (3) is deleted, and the same results were obtained from Lue *et al.*'s and our equations.

When it comes to ultrathin oxides or leaky high-k dielectrics, the static dielectric loss due to tunneling leakage current is much more significant than the dynamic one. This is the four-element circuit model for leaky MOS capacitors as shown in Fig. 1(d) [6]. Equations (3) and (4) can also be applied to this model if the $\tan\delta/\omega C_0$ term in (3) is deleted. Sometimes, if the dielectric is too leaky, the criteria $1 \ll (\omega C_0R_p)^2$ and $R_p \gg R_s$ may not be valid. The two equations from just equating the total impedance in Fig. 1(a) and (d) without any reduction should be employed to obtain C_0R_p first in similar ways above and then use this C_0R_p to obtain C_0 and the other circuit elements, i.e.,

$$C_0R_p = \frac{C_{p1}\left(G_2^2+\omega_2^2C_{p2}^2\right)-C_{p2}\left(G_1^2+\omega_1^2C_{p1}^2\right)}{G_1\left(G_2^2+\omega_2^2C_{p2}^2\right)-G_2\left(G_1^2+\omega_1^2C_{p1}^2\right)}. \tag{6}$$

III. Results and Discussion

The test structures used in this study are simple MOS capacitors with two-terminal top gate and wafer backside contacts, and all the C–V measurements were performed using the Agilent 4284A precision LCR meter in parallel mode. Figs. 2 and 3 show the measured and two-frequency-corrected C–V curves of the TiN/ALD HfO_2/SiO_2/p-Si MOS capacitors with gate area $= 10\,000$ and 400 μm^2, respectively. The details of the fabrication process could be found elsewhere [7], and the EOT was extracted as 1.38 nm using the C–V simulation program that has taken the quantum effect into account [8]. It has been demonstrated that the frequency dispersion of the clamped and amplified C–V curves at high frequencies ($>$ 500 kHz) can be effectively eliminated when considering the influences of the parasitic components R_s and L_s and that the value of each circuit element at a specific applied gate voltage could be independently obtained from (3) and (4) for the given device as listed in the figures. Note that $\tan\delta$ is $\sim$ 0.3%–0.35% and is independent of the gate area, and this dynamic dielectric loss might be a materials issue. It has been reported that $\tan\delta$ is $\sim$ 3% in $BaSrTiO_3$ high-k dielectrics and can be improved to 1% with the appropriate doping of Al_2O_3 [9]. In addition, the parasitic components R_s and L_s exhibit significant area dependences ($R_s \sim 1/\text{area}^{1/2}$ [10] and $L_s \sim 1/\text{area}$) as shown in the two insets. These findings could be explained by considering the electric flow lines from the small top gate electrode on a flat surface of a semi-infinite substrate to the wafer backside contact (similar to measuring the spreading resistance) and the phase compensation problems between the measurement signal voltage and signal current when the connection scheme of probing through the chuck with switch matrix (Agilent E5250A) is employed in the probing system.

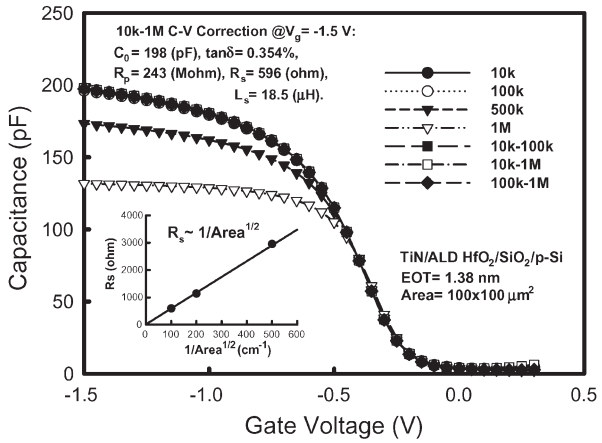

Fig. 2. Measured and two-frequency-corrected C–V curves of the TiN/ALD HfO_2/SiO_2/p-Si MOS capacitor with gate area $= 10\,000\ \mu m^2$. The frequency dispersion of clamped C–V curves could be observed at high frequencies (> 500 kHz).

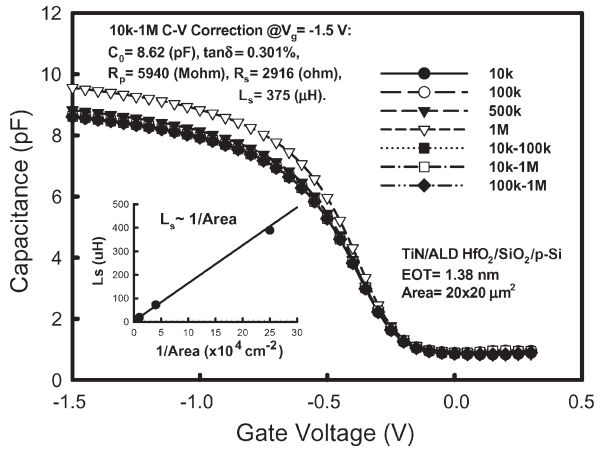

Fig. 3. Measured and two-frequency-corrected C–V curves of the TiN/ALD HfO_2/SiO_2/p-Si MOS capacitor with gate area $= 400\ \mu m^2$. The frequency dispersion of amplified C–V curves could be observed at high frequencies (> 500 kHz).

Fig. 4 shows the measured, two-frequency-corrected, and theoretical C–V curves of the ultrathin oxynitride with EOT $= 1.65$ nm. Although the severe capacitance drop could not be completely recovered, adopting two high frequencies in the two-frequency C–V correction using (6) could obtain the corrected C–V curve more close to the theoretical one. Then, use the C–V simulation program considering both poly-depletion and quantum effects [8] to perform the curve fitting at the overlapping transition region. This may provide a simple and practical approach to extract the EOT of ultrathin oxides. In addition, radio frequency (RF) C–V measurement and short channel devices are highly suggested to be accompanied with the above method [11], [12].

IV. Conclusion

The two-frequency C–V correction using adequate circuit models can effectively eliminate the frequency dispersion of clamped and amplified C–V curves for low leakage high-k dielectrics, and this C–V correction method can also improve the capacitance drop of ultrathin oxides to an acceptable level

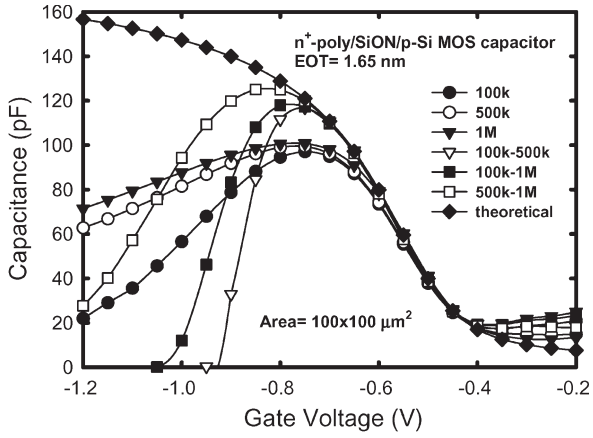

Fig. 4. Measured, two-frequency-corrected, and theoretical C–V curves of the ultrathin oxynitride with EOT $= 1.65$ nm. Adopting two high frequencies in the two-frequency C–V correction and then using the C–V simulation program to perform the curve fitting may provide a simple and practical way to extract the EOT of ultrathin oxides.

in order to perform the curve fitting using a C–V simulation program. This technique could be readily integrated into the routine C–V measurements since only simple algebraic operations are needed.

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