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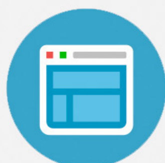
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Annealing temperature effect on the performance of nonvolatile HfO_2 Si-oxide-nitride-oxide-silicon-type flash memory

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In this article, we demonstrate the effect of the postdeposition annealing for the HfO_2 trapping layer on the performance of the Si-oxide-nitride-oxide-silicon-type flash memories. It was found that the memory window becomes larger while the retention and endurance characteristics get worse as the annealing temperature increases. This was ascribed to the larger amount and the shallower energy levels of the crystallization-induced traps as compared to the traps presented in the as-fabricated HfO_2 film. Finally, in the aspect of disturbances, we show only insignificant read, drain, and gate disturbances presented in the three samples in the normal operation. © *2006 American Vacuum Society.* [DOI: 10.1116/1.2174021]

I. INTRODUCTION

Poly-Si-oxide-nitride-oxide-silicon (SONOS)-type flash memories have recently attracted much attention for the application in the next-generation nonvolatile memories.[1] Based on discrete storage nodes, the SONOS-type flash memories have the potential for achieving high program/erase speed, low programing voltage, low-power performance, large memory window, excellent retention, endurance, and disturbance characteristics.[2–6] Hafnium oxide (HfO_2) is considered to be a promising candidate for the charge trapping layer for the SONOS-type flash memory instead of Si_3N_4 film.[7] The high-κ dielectric film, HfO_2, is expected to have better charge trapping characteristics than the conventional Si_3N_4 films for sufficient density of trap states and deep trap energy level to achieve longer retention time.[8,9] This feature makes HfO_2 be more helpful in scaling the tunnel oxide for enhancing the performance and more suitable for the development of the SONOS-type memory with multibit operation.[10,11] However, using HfO_2 film as the trapping layers has the issue of lateral migration of trapped electrons and then leads to degraded retention.[12]

In this article, we investigated the performances of the HfO_2 SONOS-type flash memories by changing postdeposition annealing temperatures for the HfO_2 trapping layer. Besides, we show that the high-κ dielectric film such as HfO_2 can trap electron and hole for the trapping characteristics.

II. DEVICES FABRICATION

The fabrication process of the HfO_2 SONOS-type flash memory is shown in Fig. 1. A 2 nm direct tunneling oxide was thermally grown on a (100)-oriented p-type Si substrate. A 5 nm amorphous HfO_2 layer was subsequently deposited by electron beam evaporation method with pure HfO_2 (99.9% pure) targets. Next, the samples were subject to rapid thermal annealing (RTA) through N_2 gas at 600 and 900 °C for 1 min. A blocking oxide of about 8 nm was then deposited by plasma-enhanced chemical vapor deposition (PECVD) followed by poly-Si deposition and gate patterning to complete the gate stack formation of the HfO_2 SONOS-type flash memory devices.

III. CHARACTERIZATION RESULTS AND DISCUSSION

A. Devices operation

Figures 2 and 3 show the programing and erasing characteristics, respectively, with different pulse widths for the HfO_2 SONOS-type flash memories with different post-HfO_2-deposition annealing temperatures. All devices described in this article had dimensions of $L/W=1/2\ \mu$m. We used channel hot-electron injection for the programing with the bias condition at $V_g-V_t=7$ V and $V_d=6$ V and band-to-band hot-hole injection for erasing with the bias condition at $V_g-V_t=-6$ V and $V_d=8$ V.[13] Based on the discrete charge storage of HfO_2 trapping layer, the feasibility of 2 bit operation can be achieved with proper bias scheme. We can employ forward and reverse reads to detect the information stored in the programed bit 1 and bit 2, respectively. This means that we can program 1 bit and read the information using a reverse read scheme. We have added Table I to summarize the bias conditions for 2 bit operation. For the temperature effect, it was clearly observed that the programing

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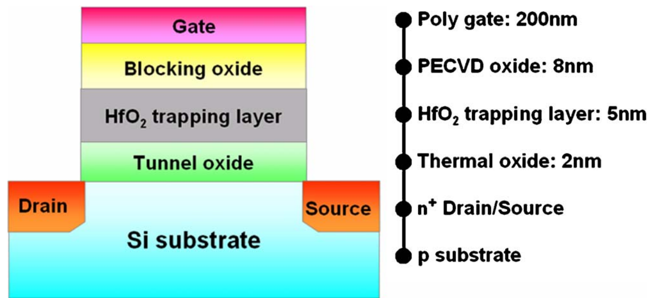

FIG. 1. Schematic cross section and process flow of the HfO_2 SONOS-type flash memory device.

TABLE I. Summary of the bias conditions for two-bit operation in the memory cell.

		Program (V)	Erase (V)	Read (V)
Bit 1	$V_g - V_t$	7	−6	3
	V_d	6	8	0
	V_s	0	0	>2
Bit 2	$V_g - V_t$	7	−6	3
	V_d	0	0	>2
	V_s	6	8	0

speed and the memory window increase when the annealing temperature increases. In addition, with the annealing temperature increases, the erasing speed increases but slight overerasure can be observed.[14] We speculate that this is due to the crystallization-induced trap generation. As well known, the HfO_2 trapping layers will crystallize after high temperature annealing. The defects along the grain boundaries are thought being able to act as the extra trapping sites and, therefore, larger memory window can be obtained.[15] From the results of x-ray diffraction (XRD) analysis, we did see that the degree of crystallization becomes more significant upon increasing temperature (not shown). Since the V_t are 2.7, 2.2, and 1.8 V for the as-deposited, 600 and 900 °C-annealed devices, respectively, we then conclude that the generated crystallization-induced traps inside the HfO_2 trapping layer are hole-trap-like, which fact can explain the result shown in Fig. 3 that the more severe overerasure upon increasing annealing temperature has been Owing to the nature of discrete charge storage sites in the high-κ gate dielectrics, we can easily achieve 2 bit storage in one single memory device by just reversing source and drain.[16]

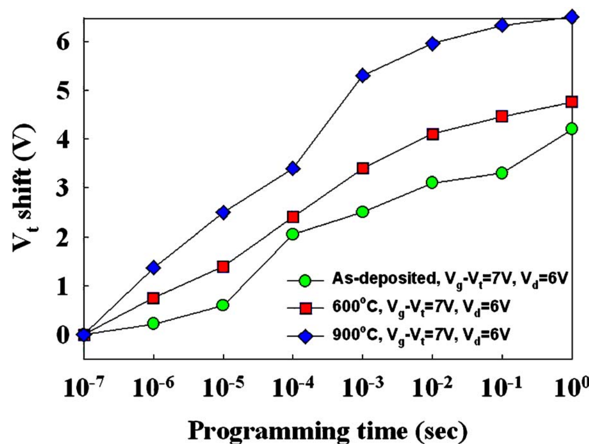

FIG. 2. Programing characteristics of the HfO_2 SONOS-type flash memories. It was clearly observed that the programing speed and the memory window increase when the annealing temperature increases.

Figure 4 illustrates the retention characteristics for all HfO_2 SONOS-type flash memories. The retention time of the memory with as-deposited HfO_2 trapping layer can be up to 10^8 s for 10% charge loss. However, it was significantly degraded as the annealing was employed and the situation became worse as the temperature increased. We have calculated the activation energy of the traps in the HfO_2 nanocrystals for the fresh device. Activation energy tracing is used widely to characterize the Arrhenius relation extracted from the temperature dependence of charge loss in a nonvolatile memory as a function of time. For a given charge-loss threshold criterion (in our case, 20%), the failure rates obtained at higher

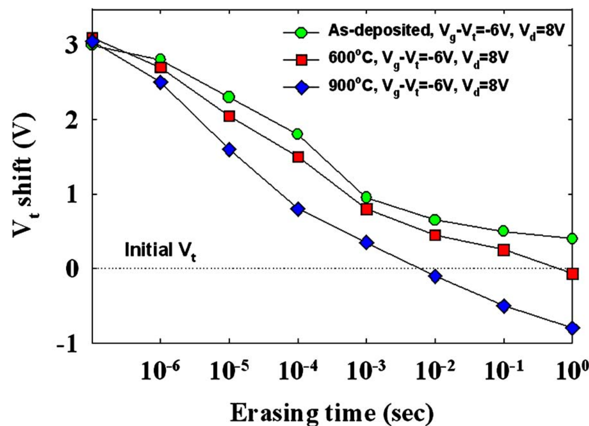

FIG. 3. Erasing characteristics of the HfO_2 SONOS-type flash memories. With the annealing temperature increases, the erasing speed increases and shows little overerasure.

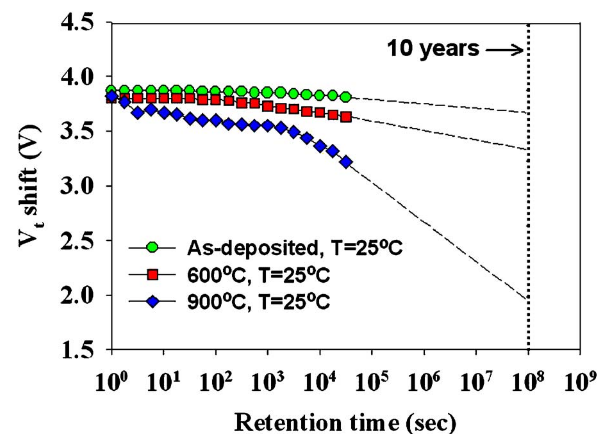

FIG. 4. Erasing characteristics of the HfO_2 SONOS-type flash memories at room temperature T=25 °C. The 900 °C-annealed device shows the worst retention performance.

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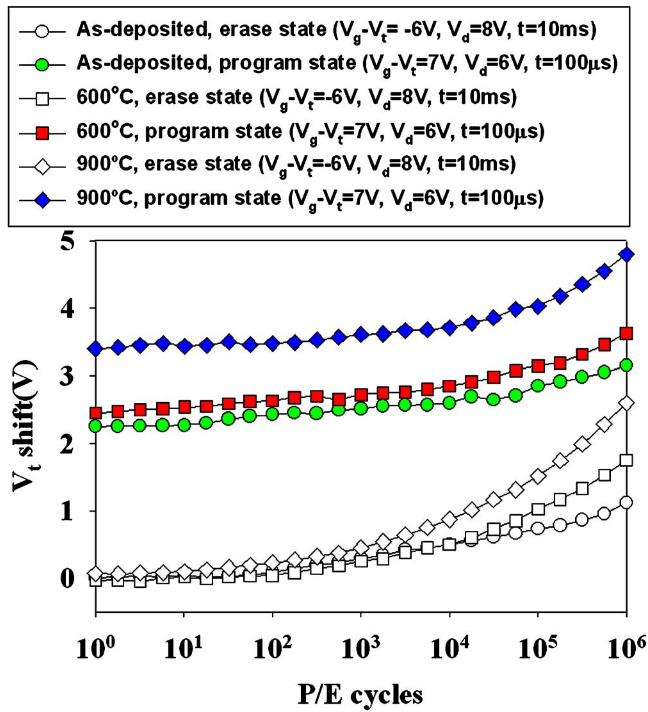

FIG. 5. Endurance characteristics of the HfO_2 SONOS-type flash memories. The 900 °C-annealed device shows larger memory window but worse endurance performance in the same condition.

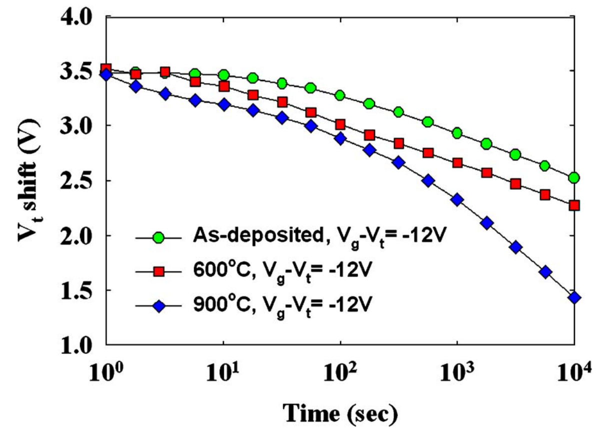

FIG. 6. Vertical migration characteristics of HfO_2 SONOS-type flash memories. Consistent with the former result, the vertical charge migration is exacerbated by increasing annealing temperature.

temperatures (125–200 °C), and five numbers for every temperature, can then be extrapolated to the nominal operating condition. The extracted activation energies are 2.45, 1.78, and 0.96 eV for the as-deposited, 600 and 900 °C-annealed samples, respectively.[17] Therefore, we thought that the post-deposition annealing will induce more traps with shallower energy level in the trapping layer, which give rise to larger memory window and poor charge retention.

The endurance performances after 10^6 P/E cycles are shown in Fig. 5. Again, the rate of memory window narrowing increases upon increasing annealing temperature. As we know, the narrowing is mainly coming from charge gain. Because of the use of ultrathin tunnel oxide, there is only very minute amount of trapped charges generated during operation in the tunnel oxide.[18] Hence, we attribute this to the residual charges along the grain boundaries because these highly localized induced traps are more difficult to remove unless their positions are coincided to overlap with the hot-hole injection. Figure 6 shows the vertical charge migration characteristics with applying V_g-V_t=−12 V at room temperature 25 °C. Consistent with the former result, the vertical charge migration is exacerbated by increasing annealing temperature. With the annealing temperature increases, the more vertical charge loss was found. It can be explained by more leakage path in the grain boundary of crystallized HfO_2 in the high annealing temperature.

B. Disturbances

Figure 7 shows the read disturb induced erase-state threshold voltage instability in a localized HfO_2 SONOS-type flash memory cell for three samples. To allow for 2-bit operation, the applied bitline voltage in a reverse-read scheme must be sufficiently large (>1.5 V) for being able to "read through" the trapped charge in the neighboring bit. Relatively large read bitline voltage may cause unwanted electron injection and then results in a significant threshold voltage shift of the neighboring bit. For our measurement, the gate and drain biases were applied and the source was grounded. The results clearly show that almost no read disturbance appears for the low voltage reading operation of V_g-V_t=3 V and V_d=2.5 V in our HfO_2 flash memory.

Figure 8 shows the programing drain disturbance of our HfO_2 SONOS-type flash memories. The same drain voltages (V_d=8 V) were applied in the programing drain disturbance measurements at room temperature (T=25 °C). Upon the increasing annealing temperature, the more drain disturbances were observed. The storage charge leakage path along the grain boundaries induces more drain disturbances for the annealed devices. After 1000 s at 25 °C, we have sufficiently drain the disturb margin (<0.3 V) for the three annealed samples.

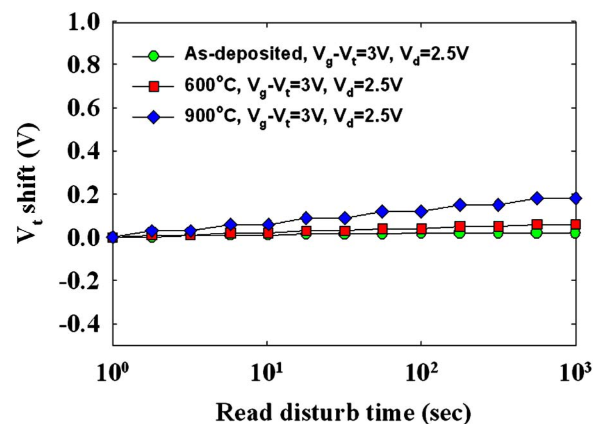

FIG. 7. Read disturbance characteristics of HfO_2 SONOS-type flash memories. No significant V_t shift for all samples even after 1000 s at 25 °C.

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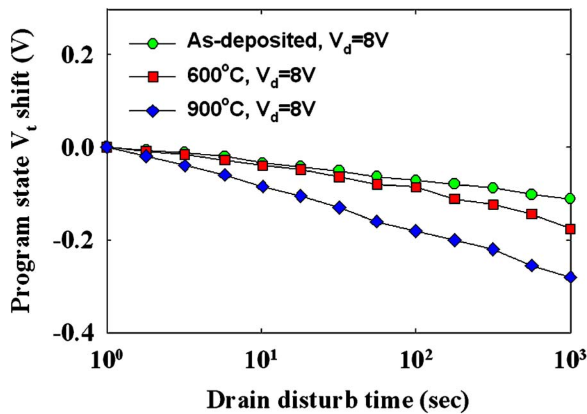

FIG. 8. Drain disturbance characteristics of HfO_2 SONOS-type flash memories. After 1000 s at 25 °C, only 0.4 V drain disturb margin is observed for the 900 °C-annealed devices.

Figure 9 shows the gate disturb characteristics in the erasing state. Gate disturbance may occur during programing for the cells sharing a common wordline while one of the cells is being programed. We measured the gate disturbance with the condition at V_g-V_t=7 V and V_d=V_s=V_{sub}=0 V for the three annealed samples. With the annealing temperature increases, the more gate disturbances were observed. A large amount of trap generates in the high temperature annealing that induces more gate disturbances for the annealed devices. Only 0.5 V threshold voltage shift has been observed for the 900 °C annealed devices after 1000 s stressing. Such good gate disturb characteristic with such thin tunnel oxide can be explained by using the serial capacitor voltage divider model with small voltage drop at the tunnel oxide. In summary, we have good read, drain, and gate disturbances for the as-deposited, 600 and 900 °C-annealed samples.

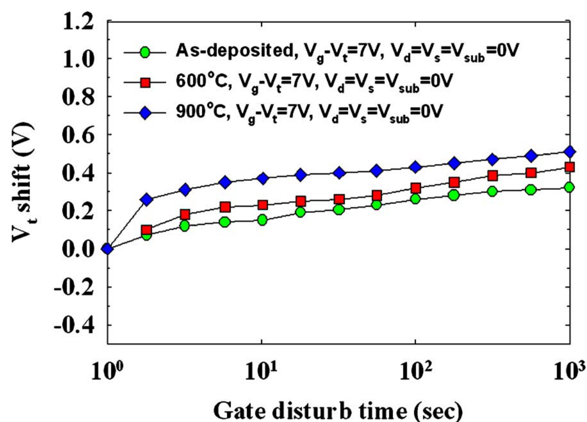

FIG. 9. Gate disturbance characteristics of HfO_2 SONOS-type flash memories. Only 0.5 V threshold voltage shift has been observed for the 900 °C-annealed devices after V_g-V_t=7 V and V_s=V_d=V_{sub}=0 V, 1000 s stressing.

IV. CONCLUSION

In this article, we have investigated the effect of post-deposition annealing temperature on the performance of the resultant HfO_2 SONOS-type flash memories. Higher temperature treatment can have large memory windows due to the crystallization-induced trap generation, but can lead to poorer retention and endurance performances. Moreover, we found that the HfO_2 trapping layer can trap both electrons and holes. No significant read, drain, and gate disturbances were observed for the three samples. HfO_2 SONOS-type flash memory is considered to be a promising candidate for the flash memory devices application.

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