High Efficiency MOS Charge Pumps Based on Exponential-Gain Structure With Pumping Gain Increase Circuits

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***Abstract*—Novel MOS charge pumps utilizing an exponential-gain structure and pumping gain increase (PGI) circuits with high voltage transfer efficiency to generate boosted output voltages are described. By using the PGI circuits, the threshold voltage problem of the MOSFET used as a switch is solved, and the limitation of the diode-configured output stage is removed. Thus, the boosted output voltage increases linearly as compared to the pumping stage number. An exponential-gain structure is also presented as a further application of the PGI circuit. By using this structure, fewer voltage pump stages are needed to obtain the required output voltage. For 1.5-V supply voltage operation, a four-time series (1.5 V-to-6 V) is demonstrated using the new techniques. Simulation and experimental results have shown that this design has good efficiency with a low-input supply voltage such as a one battery cell.**

***Index Terms*—Charge pump, dc/dc converter, high-voltage generator, voltage multiplier.**

I. Introduction

In RECENT years, progress has been made towards small, inexpensive, and mobile equipment. The growing portable equipment market has created a strong demand for dc/dc converters which can fit the size of the equipment. A charge pump circuit (CPC) is a kind of dc/dc converter and has been shown to be an effective technology to pump charge upward to produce a voltage higher than the regular supply voltage or downward to generate a negative voltage on a chip. Charge pump technology does not require magnetic components, so it's amenable to compact and lower cost designs. CPCs have been widely used in nonvolatile memories for many years, such as EEPROM and Flash memories that require a high voltage to program floating-gate devices for rewriting data [1]. In addition, they can also be used in power ICs or low-supply-voltage switched-capacitor systems for generating high voltages to switch metal-oxide-semiconductor (MOS) transistors.

Most MOS charge pumps are based on the circuit proposed by Dickson [2], [3] that uses diode-connected metal-oxide-semiconductor field-effect transistors (MOSFETs) as the charge transfer devices. However, the diode-connected MOSFETs, as shown in Fig. 1, have an augmented threshold voltage $V_{\rm t}$ due to the body effect. When more pumping stages are used, the $V_{\rm t}$ augmentation problem will be more serious and will result in the degradation of the output voltage. Thus, the output voltage cannot be maintained as a linear function of the number of stages, and the pumping efficiency will be highly degraded as the number of stages increases. Due to the limitation of $V_{\rm t}$, the Dickson CPC fails to operate with a low supply voltage.

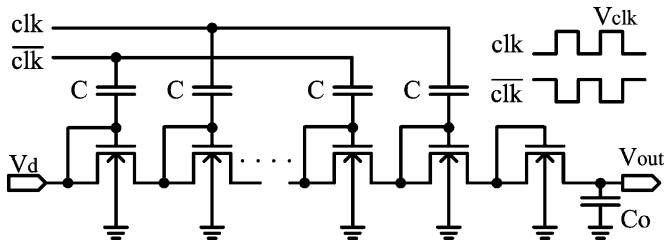

Fig. 1. Dickson charge pump circuit.

In recent years, several modifications of the Dickson CPC have been proposed to alleviate the $V_{\rm t}$ problem. It is possible to use a floating-well configuration [4] to eliminate the body effect, but that may generate substrate current [5], [6]. The four-phase pulse CPC is favored in the electronics market [7]. However, this circuit uses a more complicated timing control scheme. The new charge pump (NCP) design [6] uses the boosted voltage of the succeeding stage to backward control the charge transfer switches (CTSs). Although the CTSs in the inner stages have high transfer efficiency, the last stage still has low transfer efficiency. Another design uses an isolated body technique and additional gate-biasing circuits [8], [9]. This technique requires extra cost due to its use of triple-well technology that increases the layout and process complexity. In addition, the pumping gain is still degraded by the $V_{\rm t}$ problem in some of these circuits [8], [9]. Another voltage drop problem also exists at the output stage and further degrades the total pumping efficiency.

The above circuits are all based on the Dickson configuration. As long as the $V_{\rm t}$ problem exists, the voltage gain cannot be maintained to keep the output voltage proportional to the number of the pump stages. Thus, more pumping stages should be used to obtain the required high output voltage. This letter presents a series of new charge pump circuits that offer high pumping gain in the inner stages and a very low voltage drop at the output stage. In practice, the output voltages of the proposed pump circuits are almost perfectly proportional to the number of stages. In Section II, the configuration and operating principle of the proposed circuits denoted by pumping gain increase (PGI) circuits are described, and the performance improvement is verified by both simulation and measurement results. In Section III, the exponential-gain architecture for reducing the number of stages and simplifying the complexity of the circuit is proposed [10]. With i cascaded voltage multipliers, each supporting a gain of n, the output voltage can be increased by a factor of n^i by using the exponential-gain pump structure. Measurements taken from test chips that were fabricated using a standard 0.35-μm CMOS technology are also demonstrated in Sections II and III. Conclusions are given in Section IV.

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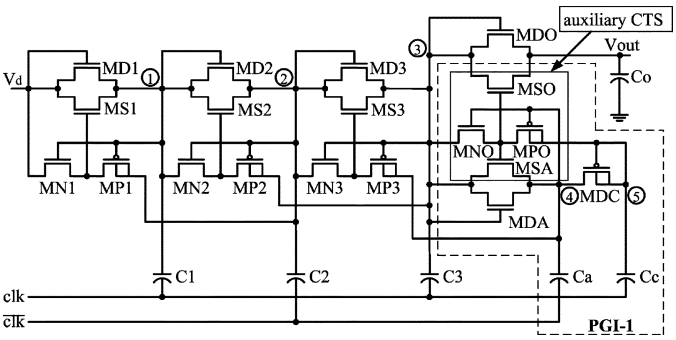

Fig. 2. Three-stage NCP2 using PGI-1 as its output stage.

II. Pumping Gain Increase Circuit

Charge pump circuits always suffer from increased drain-source voltage drop (V_{ds}) across every charge transfer MOS switch where V_{ds} is affected by the augmented threshold voltage V_t. The pumping efficiency becomes worse as the stage number of CPC increases. The PGI circuits detailed in this section are being proposed to increase the total pumping efficiency by solving the V_{ds} problems in the inner CTSs and the switch of the output stage.

A. PGI-1

The NCP2 circuit utilizes dynamic CTSs to assign the gate control input of each transfer switch to the higher voltage level provided by the next pump stage [6]. With the increasing pump voltage at the source terminal of each CTS, V_t still unavoidably grows along with the increased source-body voltage (V_{sb}). In the last CTS, there is no succeeding stage to generate higher voltage. When the pumping stage number increases to a value such that the gate control voltage (V_{gs}) of the last CTS cannot exceed the increased V_t, the pumping output voltage will arrive at the saturation level. In addition, NCP2 uses a MOS-diode in the output stage, and a large voltage will be dropped across the diode due to the augmented threshold voltage.

Instead of using the diode-configured MOS switch at the output stage in NCP2, a pumping gain increase circuit denoted by PGI-1 is proposed. Fig. 2 shows a CPC circuit built by a three-stage NCP2 circuit with a PGI-1 circuit as the output stage. The objective is to increase the voltage level of the switch control signal. A small auxiliary CTS is added to provide a high voltage level to drive the output switch so that the output stage has perfect pumping performance.

The operation of the circuit is explained as follows. In Fig. 2, clk and $\overline{clk}$ are out-of-phase and have the same voltage amplitude V_{clk}. The MOS diodes (MDx) are used to establish the initial voltages. When clk is low and $\overline{clk}$ is high, the voltage V_2 and V_4 of nodes 2 and 4 are raised to higher potential levels so that the preceding switches MS1 and MS3 can be turned on and charge $C1$ and $C3$, respectively. Simultaneously, Cc is further charged through MDC. When clk is high and $\overline{clk}$ is low, the voltages V_1, V_3, and V_5 are raised to higher potential levels. The high voltage V_3 leads the preceding switch MS2 to be turned on to charge $C2$. Simultaneously, MSO and MSA are turned on, since V_4 is low and V_5 is high. Thus, Ca and Co are charged through MDA&MSA and MDO&MSO, respectively. If the control voltage level of MSO is high enough to overcome the augmented $V_{tn(\mathrm{MSO})}$, MSO can be turned on and the pump efficiency of the output stage can be kept as high as that of the forestages.

The choice between an NMOS diode and a PMOS diode for MDC is an important design issue of PGI-1. Although PGI-1 can eliminate the V_{ds} drop in the output stage, the V_{tn} increase still exists and affects the internal charge transfer devices, especially when MDC is an NMOS diode. For the case of an NMOS diode based MDC, the pumping voltage in the circuit can be expressed as follows.

1) When clk is high and $\overline{clk}$ is low

$$V_{Ca} \simeq V_{C3} + V_{clk} \qquad \text{where} \quad \mathrm{C3} \gg \mathrm{Ca}. \tag{1}$$

2) When clk is low and $\overline{clk}$ is high

$$V_{Cc} \simeq (V_{Ca} + V_{clk}) - V_{ds(\mathrm{MDC})} \text{ where } Ca > Cc. \tag{2}$$

From (1), a complete conduction of MSA is needed to obtain higher V_{Ca} which is established by $(V_{C3}+V_{clk})$. From (2), the corresponding gate control voltage of MS3 and MSA is provided by $(V_{Ca}+V_{clk})$ and $(V_{Cc}+V_{clk})$, respectively, where V_{Cc} is established by $(V_{Ca}+V_{clk})-V_{ds(\mathrm{MDC})}$. To turn on MSO and MSA and give perfect pumping efficiency to the output stage, $V_{gs(\mathrm{MSO})}$ and $V_{gs(\mathrm{MSA})}$ must be high enough to conquer their threshold voltages. Thus, the lower-bound condition for turning on MSO and MSA must be satisfied

$$V_{gs(\mathrm{MSO})} \simeq (V_{Cc} + V_{clk}) - V_{Ca} > V_{tn(\mathrm{MSO})} \tag{3a}$$
$$V_{gs(\mathrm{MSA})} \simeq (V_{Cc} + V_{clk}) - V_{Ca} > V_{tn(\mathrm{MSA})}. \tag{3b}$$

If no load is applied to the output, V_{Ca} will be the same as V_{out} and the lower bounds of MSO and MSA will have the same value. Substituting (2) into (3), the lower-bound condition for turning on MSO can be obtained as

$$V_{gs(\mathrm{MSO})} \simeq 2V_{clk} - V_{ds(MDC)} > V_{tn(\mathrm{MSO})}. \tag{4}$$

In (4), the threshold voltage depends on the body effect and can be obtained by

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|2\phi_f + V_{sb}|} - \sqrt{2\phi_f}\right) \tag{5}$$

where V_{th0} is the threshold voltage with $V_{sb} = 0$. The Fermi level ϕ_f and the parameter γ are constant values if the process characteristic is fixed. From (5), it can be seen that increasing $V_{sb(\mathrm{MSO})}$ results in increasing the value of $V_{tn(\mathrm{MSO})}$. Similarly, if MDC is an NMOS diode, a large $V_{ds(\mathrm{MDC})}$ will occur due to a large $V_{sb(\mathrm{MDC})}$. From (4), when the sum of augmented $V_{tn(\mathrm{MSO})}$ and $V_{ds(\mathrm{MDC})}$ is larger than $2V_{clk}$, MSO and MSA will not turn on and V_{out} will start to saturate.

With the aid of (4) and (5), the approximate value of the output saturation voltage can be graphically determined from Fig. 3. Line-1 is the threshold voltage of MSO with respect to various V_{out}. In the proposed circuits, all the bodies of the NMOS transistors are connected to ground. Since the source of

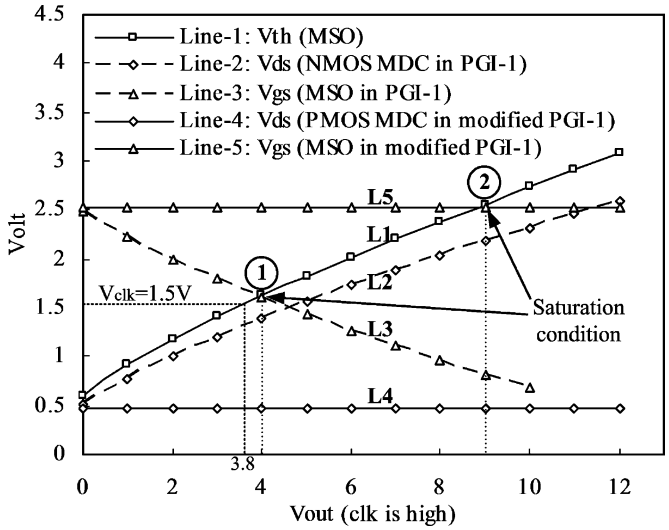

Fig. 3. Graphical solution for obtaining the output saturation voltage in PGI-1 and modified PGI-1 where V_d and V_{clk} are 1.5 V and all the voltages are taken when clk is high.

MSO is connected to the output terminal in PGI-1, $V_{\rm out}$ is equivalent to $V_{sb(\rm MSO)}$. Thus, V_{th} can be obtained by substituting $V_{\rm out}$ to (5) and that produces Line-1. When MDC is an NMOS diode, $V_{gs(\rm MSO)}$ can be calculated from (4) once $V_{ds(\rm MDC)}$ is known. However, $V_{ds(\rm MDC)}$ should be determined by its subthreshold voltage, which is smaller than $V_{tn(\rm MDC)}$. To obtain $V_{ds(\rm MDC)}$, SPICE simulation results were used to sketch Line-2. Line-3, which indicates $V_{gs(\rm MSO)}$, was obtained by calculating (4). The intersection of Line-1 and Line-3 gives the critical value of $V_{gs(\rm MSO)} = V_{tn(\rm MSO)}$. The intersection at point 1 shows that the saturation point of $V_{\rm out}$ is about 4 V. Thus, if more than two pump stages are used, $V_{\rm out}$ will start to saturate around 4 V.

An alternative design employed to solve the saturation problem uses a P-MOSFET, based on an N-well/P-substrate, for the MDC in the modified PGI-1. The body of the PMOS is connected to its output side so that the MDC operates as a forward-biased PN junction diode in the charging periods of Cc. This PMOS diode can be easily implemented with a standard process. The simulation result shows that the $V_{ds(\rm MDC)}$ voltage drop is fixed to a small value and the MDC PMOS diode no longer has a saturation problem. Thus, the saturation voltage of $V_{\rm out}$ can be increased further according to (4), which denotes that $V_{ds(\rm MDC)}$ is about 0.5 V. However, the MSO switch still affects the saturation effect. From the intersection at point 2 in Fig. 3, the saturated output voltage has been increased to about 9 V where both V_d and V_{clk} are 1.5 V.

B. PGI-2

In the second type of PGI circuit, PGI-2, the charging switch of the output stage is replaced by a single PMOS switch. Fig. 4 shows a one-stage charge pump circuit using PGI-2. MSO is a PMOS output switch and MD1 is a MOS diode used to establish the initial voltages. The control circuit of the MSO switch is omitted by connecting the gate of MSO to the CTS of the forestage. When clk is high, V_1 is raised to the higher potential $(V_{C1} + V_{clk})$. This high voltage leads MN1 to be turned on and MP1 to be turned off. Thus, V_2 is equal to the lower voltage, V_d, and forces MS1 to turn off and MSO to turn on. Since MSO is

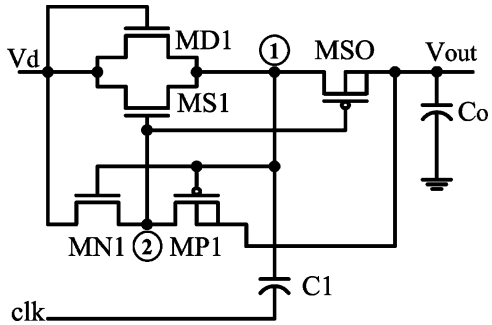

Fig. 4. One-stage charge pump circuit using PGI-2.

turned on, no voltage gain is lost in the output stage. Conversely, when clk is low, MP1 is turned on and MN1 is turned off. This forces MS1 to turn on and MSO to turn off and keeps Co isolated from its forestage.

PGI-2 solves the output voltage gain loss problem, but output saturation still exists due to the fact that MS1 is affected by the augmented threshold voltage problem. The saturation condition in PGI-2 can be derived as follows.

1) When clk is high, MSO will be turned on by $V_2 = V_d$ and $V_{\rm out}$ is established as

$$V_{\rm out} \simeq (V_{C1} + V_{clk}) - V_{ds(\rm MSO)}. \tag{6}$$

2) When clk is low, MS1 will be turned on by $V_2 = V_{\rm out}$ and $V_{gs(\rm MS1)}$ is given by

$$V_{gs(\rm MS1)} \simeq V_{\rm out} - V_{C1} > V_{tn(\rm MS1)}. \tag{7}$$

Substituting (6) in (7) and rewriting $V_{gs(\rm MS1)}$ gives the saturation condition

$$V_{gs(\rm MS1)} \simeq V_{clk} - V_{ds(\rm MSO)} > V_{tn(\rm MS1)}. \tag{8}$$

In the above equation, $V_{ds(\rm MSO)}$ across the output stage is very small since MSO is turned on during the duration of high clk. Even though $V_{ds(\rm MSO)}$ is approximately zero, (8) shows that the output saturation will start when the augmented $V_{tn(\rm MS1)}$ becomes greater than V_{clk}. This scenario happens in the PGI-2 circuit using multiple stages. Comparing (8) with (4), the output saturation level yielded by PGI-2 is smaller than that yielded by PGI-1 due to a $2V_{clk}$ term in (4). Similar to the graphic analysis in PGI-1, Line-1 of Fig. 3 also can be used to find the output saturation level of PGI-2. When clk is high, the source of MS1 is connected to $V_{\rm out}$ through MSO, so that $V_{sb(\rm MS1)}$ is equivalent to $V_{\rm out}$. Thus, Line-1 also expresses $V_{tn(\rm MS1)}$ in PGI-2 with respect to various $V_{\rm out}$. Using the graphic solution previously discussed, the approximate value of the output saturation voltage is 3.8 V in PGI-2, since the augmented $V_{tn(\rm MS1)}$ becomes greater than V_{clk}. Although the saturation condition of PGI-2 is not as good as that of the modified PGI-1, PGI-2 is simpler and the circuit for producing the additional control voltage higher than $V_{\rm out}$ is no longer necessary. While a 1.5-V supply is applied, a two-stage PGI-2 for 3× pumping gain (1.5 V-to-4.5 V) can be fabricated using normal standard CMOS technology.

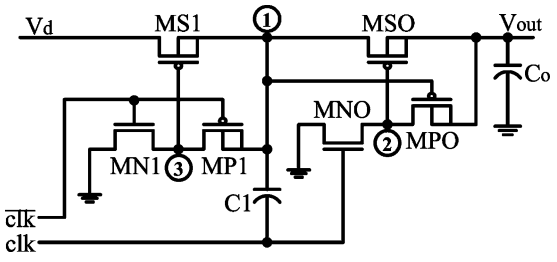

Fig. 5. One-stage charge pump circuit using PGI-3.

C. PGI-3

In PGI-2, only the output stage is replaced by a single PMOS. In the third type of PGI circuit, PGI-3, all the NMOS CTSs have been replaced by PMOS CTSs. It is found that the PMOS switch can operate equivalently to a body diode in parallel with a PMOS transistor in saturation mode. PGI-3 has a high saturation level and a high pumping gain. Fig. 5 shows a one-stage charge pump circuit of the PGI-3. When clk is low and $\overline{clk}$ is high, MS1 will be turned. This will result in V_{C1} being charged to V_d. During this time, the gate terminal of the output stage MSO (node 2) is connected to $V_{\rm out}$ through MPO. Thus, MSO is cut off for this duration. When clk is high and $\overline{clk}$ is low, MP1 and MNO will turn on and MN1 and MPO will be off. Consequently, MS1 is turned off and MSO is turned on.

It is important to mention that the connection of the body of PMOS CTS provides a body diode connecting in parallel to a PMOS transistor. There are two attractive benefits of this design: the use of body diodes reduces the charging time of $C1$ and Co, and the V_{ds} steady-state values of both MS1 and MSO are approximately zero, due to the conduction of the PMOS transistors. Since all of $|V_{gd}|$, $|V_{gs}|$, and $|V_{gb}|$ are greater than $|V_{tp}|$, there is no V_t augmentation problem in PGI-3.

D. Simulation and Measurement Results

Fig. 6 shows the simulation results for the output voltages of various charge pump designs. In order to obtain reasonable comparisons from all the circuits under test, the charging switches have been designed to have the same channel width and length. From Fig. 6, the order from high to low of output saturation voltages is PGI-3, PGI-1, PGI-2, NCP2, and Dickson. The pumping gain of PGI-3 is very close to the ideal value without a saturation problem, and $V_{\rm out}$ can easily exceed 10 V with a 1.5-V supply when six pumping stages are used. Although all four CPCs, except PGI-3, have obvious output saturation, the output saturation voltage of PGI-1 is about 7.8 V, which is much higher than the other three CPCs.

The load current also has influence on the output voltage. As shown in the simulation result presented in Fig. 7, output voltage always decreases as load current increases. Furthermore, since PGI-2 and PGI-3 use PMOS CTSs, the corresponding output voltage losses are greater than that in the PGI-1 circuit, which uses NMOS CTSs.

A three-stage PGI-1 and PGI-3 have been fabricated using a TSMC 0.35-μm mixed mode process. Fig. 8 shows the measurement results. Although the rated operating voltage of this process is 5 V, it is found from the measured data that no breakdown happens to the devices when the output is below 8 V. The measured output voltages are less than the simulation results

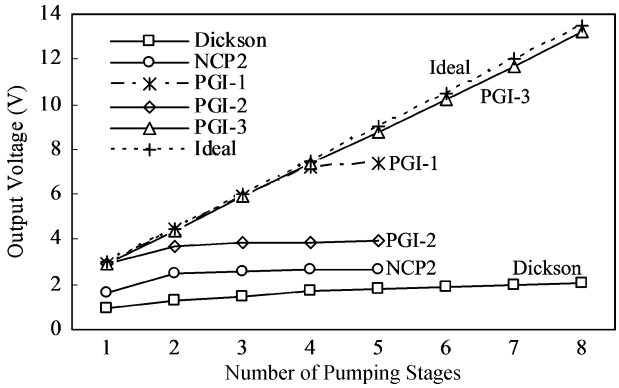

Fig. 6. Simulated output voltage versus pumping stage number of various CPCs with $V_{\rm in} = V_{clk} = 1.5$ V, $f_{clk} = 2$ MHz, and $I_o = 10\ \mu$A.

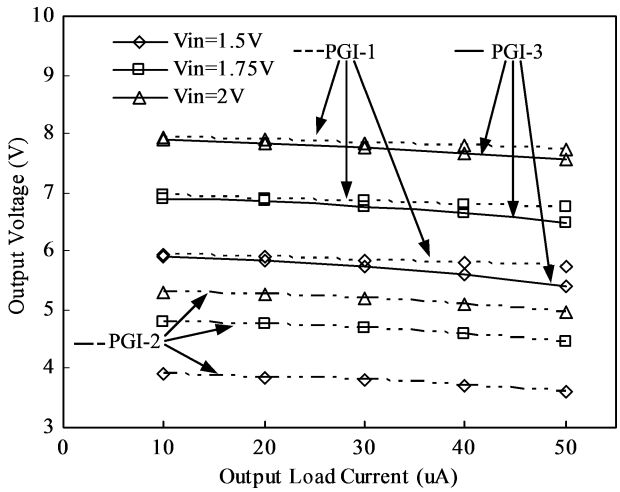

Fig. 7. Simulated output voltage versus output load current of various three-stage PGI circuits under different $V_{\rm in}$.

shown in Fig. 7, due to additional parasitic capacitors, parasitic resistors, and extra switching losses in the clock generation circuit. For the case of low-output current loading, the output voltage of PGI-3 is slightly better than that of PGI-1, as the W/L ratios of the PMOS CTSs in PGI-3 are greater than that of the NMOS CTSs in PGI-1 in the practical layout. In PGI-3, the output can climb above 7.5 V with a load current of 10 μA and a 2-V supply. This result is close to a 2 V-to-8 V ideal case with a 4$\times$ pumping gain. The measurement results for 1.5-V and 1.75-V supply voltages are also close to the ideal value.

III. Exponential-Gain Pump Structure

Since most CPCs have a linear growing structure and voltage gain loss, many stages will be needed to obtain high output voltages. Moreover, due to V_t augmentation, they will not achieve higher output voltages. Thus, an exponential-gain pump structure is proposed to solve the voltage saturation by making the clock voltage grows exponentially along with the number of stages cascaded. An n-times voltage multiplier is the fundamental cell of this structure. The output of this fundamental cell is connected as the power supply to the next one. With i cascaded cells, an exponential-gain pump structure will be formed to provide the total voltage gain of n^i. It should be noted that with this structure the output voltage will be confined by the

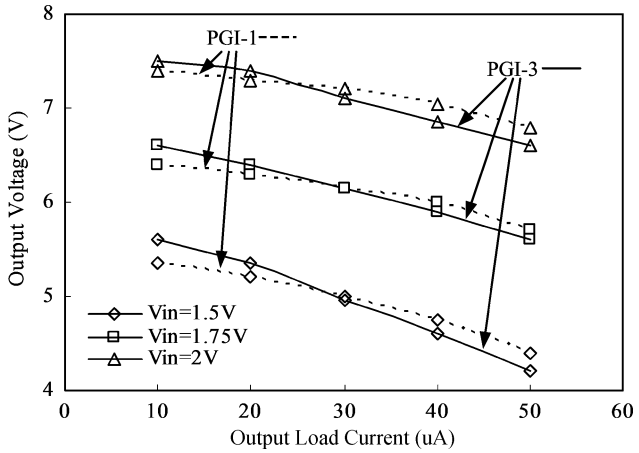

Fig. 8. Measured output voltage versus output load current of three-stage PGI-1 and PGI-3 under different $V_{\rm in}$.

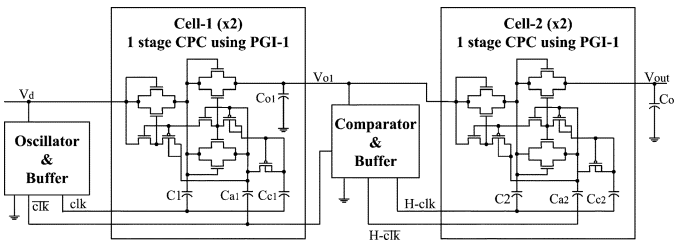

Fig. 9. Block diagram of a 2 × 2 exponential-gain pump structure.

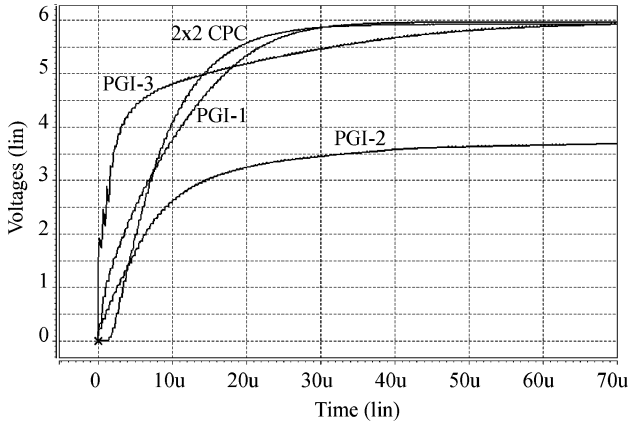

Fig. 10. Simulated transient output waveforms of 2 × 2 CPC and various three-stage PGI circuits with $V_{\rm in} = V_{clk} = 1.5$ V and $I_o = 10\ \mu$A.

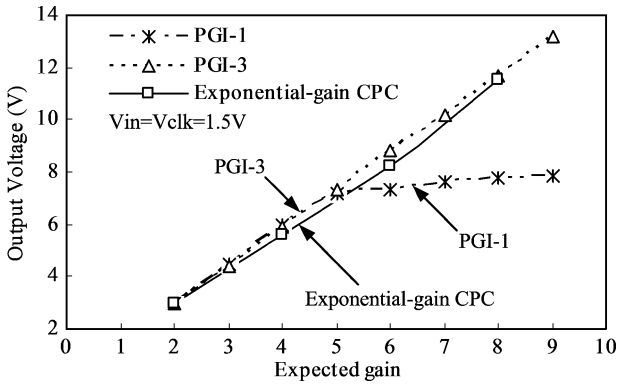

Fig. 11. Simulated output voltage versus expected gain of exponential-gain structure, PGI-1, and PGI-3 with $V_{\rm in} = V_{clk} = 1.5$ V and $I_o = 10\ \mu$A.

fabrication process. To obtain a high output voltage which exceeds the breakdown voltage of the low voltage chip, the cascaded cells need to be placed in a chip or in discrete chips fabricated by the processes which can provide a breakdown voltage higher than the operating voltages.

In Fig. 9, an exponential-gain example of a 2 × 2 charge pump circuit denoted by 2 × 2 CPC is proposed. The first stage of a 2× PGI-1 circuit, named Cell-1, is used to provide the supply voltage (V_{o1}) of the next 2× PGI-1 circuit. If more cells are cascaded, then the voltage of whole charge pump circuit will grow exponentially. From (4), since the growth of clock voltage is always greater than the growth of V_t in the structure, the V_t problem can be suppressed very well.

Other 2× cells based on PGI-2 and PGI-3, as shown in Figs. 4 and 5, respectively, have also been used to realize a 2 × 2 CPC. The advantage of the new structure can be viewed in several ways: fewer stages, lower power dissipation from switching, and high flexibility. Since the complexity of the circuit and the pumping stage number in each cell has been reduced, the parasitic effect has also been reduced and the output saturation problem will not occur, even though PGI-2 or NCP2 are used as the fundamental cells. The number of switches is decreased substantially and the power loss from switching is also reduced. In addition, a higher pumping gain can be obtained more flexibly by appropriately adjusting the number of CPC stages in each cell or the number of cascaded cells. Thus, this structure is not only suited for high pumping gain, especially in high-output voltage and low-supply voltage applications, but also simplifies the whole circuit configuration.

Fig. 10 shows the transient simulation results of the three-stage PGI-1, PGI-2, PGI-3, and the proposed exponential-gain 2 × 2 CPC based on the PGI-1 as the fundamental cell. All of these circuits are designed for a 4× ideal pumping gain and simulated with the same technology. The geometric size of each design is almost identical in all devices without optimal sizing. The simulation results show that the output voltage of the 2 × 2 CPC is equivalent to those of the PGI-1 and PGI-3.

The simulated output voltages versus expected gain of PGI-1, PGI-3, and exponential-gain CPC are shown in Fig. 11 and Table I. In the case of the exponential-gain structure, $V_{\rm out}$ is very close to the ideal value without any saturation problem in the present testing range and easily exceeds 10 V when using a 3 × 3 CPC with a 1.5-V supply. Table I also shows that the exponential-gain structure has high flexibility to generate a desired output voltage.

A 2 × 2 CPC using PGI-1, PGI-2, and PGI-3 for the fundamental cell has been fabricated with standard 0.35-μm CMOS technology. Fig. 12 shows the measured output voltage versus various supply voltages and a 10-μA output load current. The measured data show that the output voltages of 2 × 2 CPCs formed by PGI-2 or PGI-3 are lower than those formed by PGI-1. The main reason for this effect is that PGI-2 and PGI-3 use PMOSFET switches. The measured results also show that the output voltage of the exponential-gain CPC using PGI-1 has a tendency to saturate when the supply voltage exceeds 2 V.

TABLE I
COMPARISON OF OUTPUT VOLTAGES GENERATED BY PGI-1 AND EXPONENTIAL-GAIN STRUCTURE OVER SEVERAL GAIN CONFIGURATIONS

Gain V_{in} = 1.5 V (Ideal output)	**Stage number of PGI-1** (output voltage)	**Exponential-gain structure** (output voltage)
4× (V_{out} = 6V)	3-stage (V_{out} = 5.93V)	2×2 structure (V_{out} = 5.9V)
6× (V_{out} = 9V)	5-stage (V_{out} = 7.8V)	2×3 structure (V_{out} = 8.56V)
		3×2 structure (V_{out} = 8.67V)
9× (V_{out} = 13.5V)	8-stage (V_{out} = 8.2V)	3×3 structure (V_{out} = 12.3V)

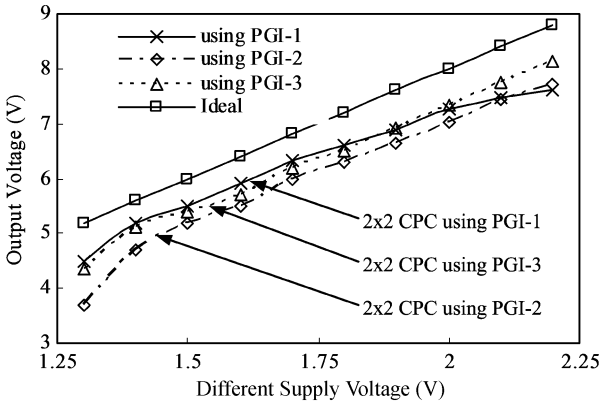

Fig. 12. Measured output voltages of 2 × 2 CPC using PGI-1, PGI-2, and PGI-3 under different supply voltages.

This is due to the breakdown voltage limitation of the process having been reached in the PGI-1 circuit of Cell-2.

IV. CONCLUSION

Two types of new designs have been proposed to overcome key problems in CPC designs. First, three different PGI circuits are proposed to reduce the voltage drop across the output stage and inner charge transfer MOS switches. The PGI circuits allow the output voltage to increase linearly as the number of pumping stages increases. However, in PGI-1 and PGI-2, the V_t increase problem still exists and limits the output voltage, as the number of stages get too large. In PGI-3, there is no saturation limit, since $|V_{gs}|$ of each CTS can always be larger than $|V_{tp}|$. Therefore, the output voltage is closer to the ideal levels.

The second design is an exponential-gain pump structure that can pump output voltage exponentially from a low power supply without an output saturation effect. This structure can be applied to produce any pumping gain with its n^i architecture. For example, a 3 × 3 CPC can be used to generate a boosted output of 12 V with a 1.5-V supply. As shown in the simulations and measurements, the proposed designs are able to generate high voltages efficiently from a power supply below 2 V. A three-stage PGI-3 circuit or a 2 × 2 CPC can generate a boosted output close to the ideal value of 6 V from a 1.5-V supply.

REFERENCES

[1] T. Kawahara, T. Kobayashi, Y. Jyouno, S. Saeki, N. Miyamoto, T. Adachi, M. Kato, A. Sato, J. Yugami, H. Kume, and K. Kimura, "Bit-line clamped sensing multiplex and accurate high voltage generator for quarter-micron flash memories," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1590–1600, Nov. 1996.

[2] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 6, pp. 374–378, Jun. 1976.

[3] T. Tanzawa and T. Tanaka, "A dynamic analysis of the Dickson charge pump circuit," *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1231–1240, Aug. 1997.

[4] K. H. Choi, J. M. Park, J. K. Kim, T. S. Jung, and K. D. Suh, "Floating-well charge pump circuits for sub-2.0 V single power supply Flash memories," in *VLSI Circuits Tech. Dig.*, Jun. 1997, pp. 61–62.

[5] J. S. Shin, I. Y. Chung, Y. J. Park, and H. S. Min, "A new charge pump without degradation in threshold voltage due to body effect," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1227–1230, Aug. 2000.

[6] J. T. Wu and K. L. Chang, "MOS charge pumps for low-voltage operation," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 592–597, Apr. 1998.

[7] A. Umezawa, S. Atsumi, M. Kuriyama, H. Banba, K. Ichi Imamiya, K. Naruke, S. Tamada, E. Obi, M. Oshikiri, T. Suzuki, and S. Tanaka, "A 5-v-only operation 0.6 um flash EEPROM with row decoder scheme in triple-well structure," *IEEE J. Solid-State Circuits*, vol. 27, no. 11, pp. 1540–1545, Nov. 1992.

[8] H. C. Lin, K. H. Chang, and S. C. Wong, "Novel high positive and negative pumping circuits for low supply voltage," in *Proc. IEEE ISCAS'99*, 1999, vol. 1, pp. 238–241.

[9] S. Y. Lai and J. S. Wang, "A high-efficiency CMOS charge pump circuit," in *Proc. Symp. IEEE ISCAS'01*, May 2001, vol. 4, pp. 406–409.

[10] L. K. Chang and C. H. Hu, "An exponential-folds design of a charge pump styled DC/DC converter," in *Proc. IEEE PESC'04*, Jun. 2004, vol. 1, pp. 516–520.