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Control of metamorphic buffer structure and device performance of $In_xGa_{1-x}As$ epitaxial layers fabricated by metal organic chemical vapor deposition

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Abstract

Using a step-graded (SG) buffer structure via metal-organic chemical vapor deposition, we demonstrate a high suitability of $In_{0.5}Ga_{0.5}As$ epitaxial layers on a GaAs substrate for electronic device application. Taking advantage of the technique's precise control, we were able to increase the number of SG layers to achieve a fairly low dislocation density ($\sim 10^6\ cm^{-2}$), while keeping each individual SG layer slightly exceeding the critical thickness (~80 nm) for strain relaxation. This met the demanded but contradictory requirements, and even offered excellent scalability by lowering the whole buffer structure down to 2.3 μm. This scalability overwhelmingly excels the forefront studies. The effects of the SG misfit strain on the crystal quality and surface morphology of $In_{0.5}Ga_{0.5}As$ epitaxial layers were carefully investigated, and were correlated to threading dislocation (TD) blocking mechanisms. From microstructural analyses, TDs can be blocked effectively through self-annihilation reactions, or hindered randomly by misfit dislocation mechanisms. Growth conditions for avoiding phase separation were also explored and identified. The buffer-improved, high-quality $In_{0.5}Ga_{0.5}As$ epitaxial layers enabled a high-performance, metal-oxide-semiconductor capacitor on a GaAs substrate. The devices displayed remarkable capacitance–voltage responses with small frequency dispersion. A promising interface trap density of $3 \times 10^{12}\ eV^{-1}\ cm^{-2}$ in a conductance test was also obtained. These electrical performances are competitive to those using lattice-coherent but pricey InGaAs/InP systems.

S Online supplementary data available from stacks.iop.org/NANO/25/485205/mmedia

Keywords: InGaAs, strain relaxation, step-graded buffer, MOSCAP, interface trap

(Some figures may appear in colour only in the online journal)

1. Introduction

Future metal-oxide-semiconductor capacitor (MOSCAP) technologies will require the integration of higher carrier mobility materials to increase drive-current capability [1, 2]. $In_xGa_{1-x}As$-based MOS devices are potentially suitable for application at low supply voltages due to high electron mobility and a bandgap lying in the range of 0.36–1.42 eV [3]. Outstanding performance of an $In_{0.5}Ga_{0.5}As$-based MOSCAP device on an InP substrate grown by molecular

beam epitaxy (MBE) has been achieved [4–6]. A major advantage of using InP as a substrate is that it is ideal for growing lattice-coherent $In_{0.5}Ga_{0.5}As$/InP. However, InP substrates are pricey and fragile and are only available in miniature size, and their manufacturing technology is less mature compared to GaAs and Si substrates [6], as the latters are now being successfully used for large-scale mass production. Hence, exploring the growth and fabrication techniques for $In_xGa_{1-x}As$ ($x \approx 0.5$)-based MOSCAP devices on GaAs or Si substrate is urgent, especially the development of the metal-organic chemical vapor deposition (MOCVD) method, which has a better scalability, a relatively faster growth rate, a shorter system downtime, and a wider temperature control range compared to MBE This makes MOCVD more suitable for the mass production of complex structures. Nevertheless, regardless of the growth technique, the major challenge in growing epitaxial $In_{0.5}Ga_{0.5}As$on GaAs/Si substrates is the considerable lattice-mismatch, which is frequently accompanied by a rough surface and a high defect density that severely deteriorates device performance. The types of defects mainly include misfit dislocations (MD) at the layer/substrate interface, and threading dislocations (TD) propagating to the outer surface of the layers. The lattice-mismatch problem has been effectively solved by using buffer layers such as Si_xGe_{1-x} [7], GaP [8], or a wafer bonding technique [9], the so-called artificial or alternative wafer platforms. By this way, defects such as TDs may be controlled by optimizing the growth parameters, as well as the use of various buffer layers. This is because a buffer layer functions as a lattice transition from the substrate to the top device layers. It also provides a smooth and a lower defect density grown front, and thus leaves strain-related defects behind.

To date, there has been a great deal of research discussing the theories of the formation, gliding, and blocking of TDs in metamorphic structures [10–12]. It is believed that TD density can be reduced through the reaction by TDs themselves [13]. Romanov theoretically suggested that the use of multiple discrete strained layers can provide a marked reduction in TD density through self-annihilation reactions [14]. According to his report, once the discrete strained layers were grown exceeding the critical thickness, TDs generated by MDs may fall within the annihilation radius at which TDs annihilate. In particular, InGaAs/GaAs heterostructure has been investigated for many years for the reduction of TDs in graded composition $In_xGa_{1-x}As$/GaAs by both molecular beam epitaxial (MBE) and MOCVD growth methods [15, 16]. It has been shown that the most effective way to reduce TDs in epitaxial layers is to optimize the Indium composition in nonlinearly continuous and step-graded buffer layers [17]. The use of a graded buffer in a lattice-mismatched system has two primary purposes: (i) to maintain a small but constant stress to prevent rampant dislocation nucleation; (ii) to keep existing dislocations moving in order to relax the lattice mismatch. Theoretically, the lattice mismatch could be slowly accommodated by a similar crystal structure in the presence of graded buffers. Yet contradictorily, a thick buffer layer is needed to achieve high crystal quality, namely, the low TD density, (thinner films have been observed to have a higher TD density [18]). This turns out to be a drawback in terms of production cost. Moreover, compositional variation induced by phase separation, which causes poor crystal quality, has been observed in ternary $In_xGa_{1-x}As$ compound at high growth temperatures [19]. Therefore, how to reconcile these demanded but contradictory requirements, and meanwhile to reach the benchmarks of device performance/scalability compared to lattice-coherent competitors, is essential to the further advance of III–V technology.

In this study, we demonstrate a successful fabrication of a MOSCAP device that meets these requirements. The MOSCAP device consisting of a high quality Al_2O_3/$In_{0.5}Ga_{0.5}As$/$In_xGa_{1-x}As$(x = 0.3–0.5)/$In_{0.3}Ga_{0.7}A$/$In_xGa_{1-x}As$(x = 0–0.3)/GaAs stacking structure was fabricated by MOCVD with a metamorphic growth. We investigate the effects of buffer ($In_xGa_{1-x}As$(x = 0.3–0.5)/$In_{0.3}Ga_{0.7}A$/$In_xGa_{1-x}As$(x = 0–0.3)) structure and growth conditions on the crystal quality and surface morphology of epitaxial $In_{0.5}Ga_{0.5}As$. It is noteworthy that from bottom to top, the device was stacked first with a buffer structure of $In_xGa_{1-x}As$(x = 0–0.3), and followed by a composition-fixed layer of $In_{0.3}Ga_{0.7}As$ (called platform layer), and continued by a second buffer structure of $In_xGa_{1-x}As$(x = 0.3–0.5), before the functional layer of $In_{0.5}Ga_{0.5}As$ was finally laid. This is because research reports had shown that the use of a platform ($In_{0.3}Ga_{0.7}As$) inserted between two buffer layers plays as a 'virtual substrate' that improves the crystal quality of the top $In_{0.5}Ga_{0.5}As$ [20, 21]. Thus, the paper is organized in a fashion of investigating the effects of the first $In_xGa_{1-x}As$ (x = 0–0.3) buffer design upon the $In_{0.3}Ga_{0.7}As$ platform layer (section 3.1), and followed by the investigations on the top $In_{0.5}Ga_{0.5}As$ influenced by the whole underneath $In_xGa_{1-x}As$(x = 0.3–0.5)/$In_{0.3}Ga_{0.7}A$/$In_xGa_{1-x}As$ (x = 0–0.3) structure (sections 3.2 and 3.3), and finally comes to the electrical performance tests (section 3.4). We demonstrate optimizations in the designed $In_xGa_{1-x}As$ buffer structure, by slightly exceeding the critical thickness (~80 nm) without sacrificing the microstructural properties (TDs density ~10^6 cm^{-2}). This enabled a high-crystal quality $In_{0.5}Ga_{0.5}As$ on a GaAs substrate. Consequently, the whole buffer thickness ($In_xGa_{1-x}As$/$In_{0.3}Ga_{0.7}A$/$In_xGa_{1-x}As$) was reduced to 2.3 μm, which offered a scalability greatly superior to the forefront studies where 5 ~ 10 μm were mostly seen in MOCVD [22–24]. Finally, the performances of the MOSCAP with designed buffer structure were tested, and its electrical versatilities were clearly revealed.

2. Experiment methods

InGaAs samples were grown on GaAs (001) substrates, which were epiready in a 6° off-cut toward [110] direction. Metal-organic chemical vapor deposition (MOCVD-EMCORE D180) was used to grow the epitaxial layers. Group-III precursors of trimethylindium (TMIn) and trimethylgallium (TMGa), and group-V precursors of pure arsine (AsH3) and phosphine (PH_3), were used. Monosilane (SiH_4) was used as an n-type doping source. The total pressure in the reactor was

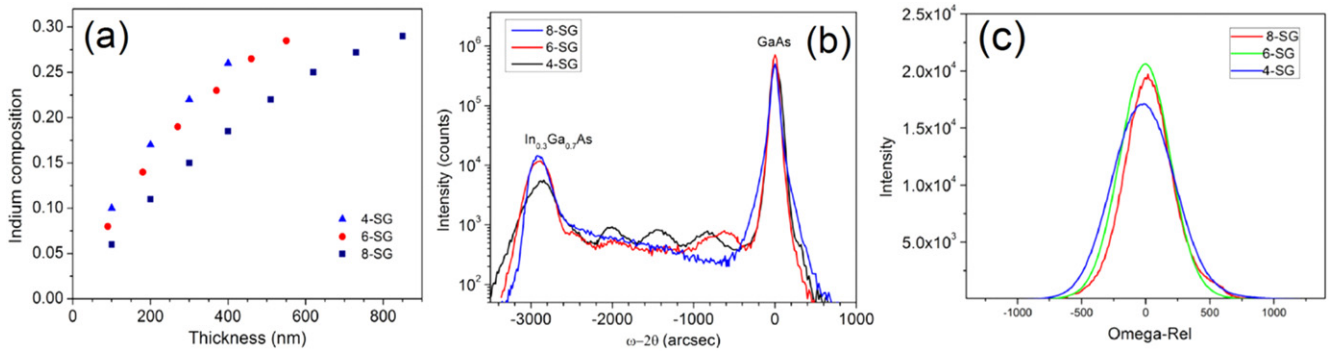

Figure 1. (a) compositional and thickness profiles for the designed 4-, 6-, and 8-SG $In_xGa_{1-x}As$ buffer structures; (b) (004) ω-2θ scan XRDs, and (c) (004) rocking curves, of $In_{0.3}Ga_{0.7}As$ epifilms grown on the 4-, 6-, and 8-SG $In_xGa_{1-x}As$ buffer layers.

kept at 70 torr. The indium composition and degree of relaxation were determined by a high-resolution x-ray diffractometer (HR-XRD). The surface texture and roughness were examined by atomic force microscopy (AFM). The dislocation density of the epitaxial layer and the phase separation phenomena were characterized by transmission electron microscopy (TEM) and energy-dispersive x-ray analysis (EDX). For MOSCAP device fabrication, an initial InGaAs/GaAs wafer was degreased in acetone and isopropanol for 2 min each. The sample was then dipped into HCL 4% solution for 2 min followed by rinsing in deionized (DI) water and N_2 blowing. It was then immediately loaded into an atomic layer deposition (ALD) chamber (Cambridge NanoTech Fiji 202 DSC). In the ALD chamber, 10-trimethyl aluminum (TMA)/Ar pulses were used for pre-cleaning, followed by the deposition of 9 nm Al_2O_3 at 250 °C using TMA and water vapor as precursors. After that, the sample was treated by a post-deposition annealing (PDA) at 500 °C in N_2 for 5 min. Ni/Au gate metal was formed by lithography/e-beam evaporation/lift-off processes. Finally, an Au/Ge/Ni/Au ohmic contact was deposited on backside using an e-beam evaporation, followed by a post-metal annealing (PMA) at 300 °C in N_2 for 1 min. Capacitance–voltage (C–V) measurements were carried out using an HP4284A LCR meter, and quasi-static C–V characterizations were performed on an Agilent B1500A analyzer.

3. Results and discussion

3.1. Effect of buffer structure on crystal quality of $In_{0.3}Ga_{0.7}As$ epilayer

We first studied the dislocation gliding and blocking process in an $In_xGa_{1-x}As$ step-graded (SG) buffer layer during the growth of $In_{0.3}Ga_{0.7}As$ on a GaAs substrate. For the purpose of this study, three different buffer structures of 4-, 6-, and 8-SG $In_xGa_{1-x}As$ layers were fabricated before the deposition of a uniform $In_{0.3}Ga_{0.7}As$ epifilm on top. Each individual SG layer was grown to ~100 nm that slightly exceeded the critical thickness (~80 nm), for the three investigated samples in order to relax the strain. It is believed that while exceeding the critical thickness, the TDs density can be reduced by self-annihilations or by being blocked by MDs during the strain relaxation in a metamorphic structure [12–14]. The critical thicknesses (h_c) can be estimated by the Matthews–Blakeslee (MB) model [25] [see a detailed equation (equation (1) in the supplementary materials]. The structural parameters and relaxation information of the epifilms were analyzed using both symmetric and asymmetric rocking curve scans on (004) and (115) ω-2θ reflections of the substrate, respectively. The In concentration (x) in the $In_xGa_{1-x}As$ epifilm is then obtained using Vegard's law [26] using the bulk equivalent or an unstrained lattice constant [27] [see detailed equations (equations (2)–(5)] in supplementary materials). Figure 1(a) shows a precise control of composition (In) with thickness profiles for the 4-, 6-, and 8-SG buffer structures. The increase of In concentration became more gradual as the number of SG layers increased, indicating an operative strain-relaxation via the SG-layer adoption. The (004) ω-2θ and ω-rocking curve XRD scans of the 4-, 6-, and 8-SG $In_{0.3}Ga_{0.7}As/In_xGa_{1-x}As$ samples are shown in figures 1(b) and (c), respectively. From the x-ray analyses described above, the In concentration of the top $In_{0.3}Ga_{0.7}As$ matched its formula for the three investigated samples. The full width at half-maximum (FWHM) of the 6- and 4-SG $In_{0.3}Ga_{0.7}As/In_xGa_{1-x}As$ samples were estimated to be 490 and 580 arcsec, respectively. A smaller FWHM of 450 arcsec was obtained in the 8-SG $In_{0.3}Ga_{0.7}As/In_xGa_{1-x}As$ sample, which suggests better crystal quality compared to the other two buffer designs.

Figures 2(a), (b) and (c) show the two-dimensional (2D) AFM images (scanning size of $5\times5\,\mu m^2$) of the top $In_{0.3}Ga_{0.7}As$ epifilms with 4-, 6-, and 8-SG layers, respectively. The root mean square (rms) roughness of the $In_{0.3}Ga_{0.7}As$ decreased from 4.8 nm to 1.8 nm upon the increase of the number of SG layers, which is indicative of an improved surface morphology. When a fewer number of SG layers were used, the lattice mismatch between layers became larger, resulting in a higher misfit dislocation density. As shown in figure 2(a) (4-SG sample), an obvious cross-hatch pattern, which is associated with a high misfit dislocation density along [110] and [1–10] directions, worsened the surface morphology. Increasing the number of the SG layer reduced misfit dislocation density substantially and led to a smoother morphology.

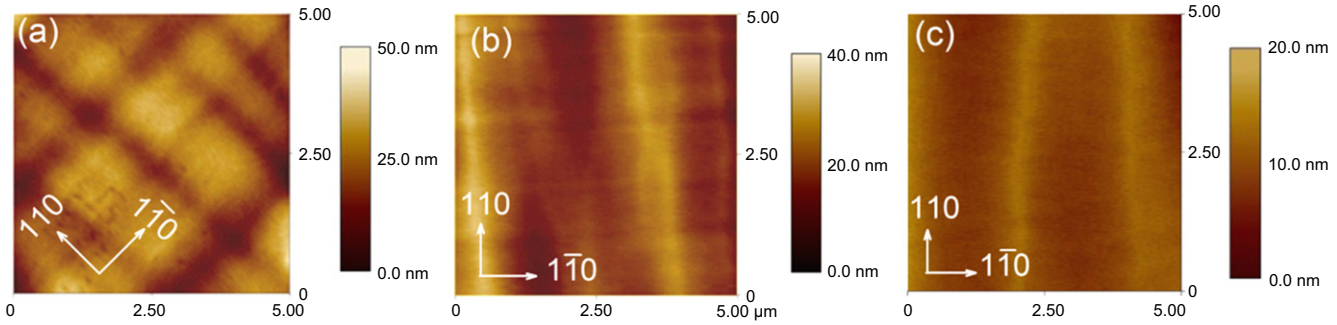

Figure 2. AFM images of $In_{0.3}Ga_{0.7}As$ epifilms grown on the (a) 4-SG, (b) 6-SG, and (c) 8-SG $In_xGa_{1-x}As$ buffer layers.

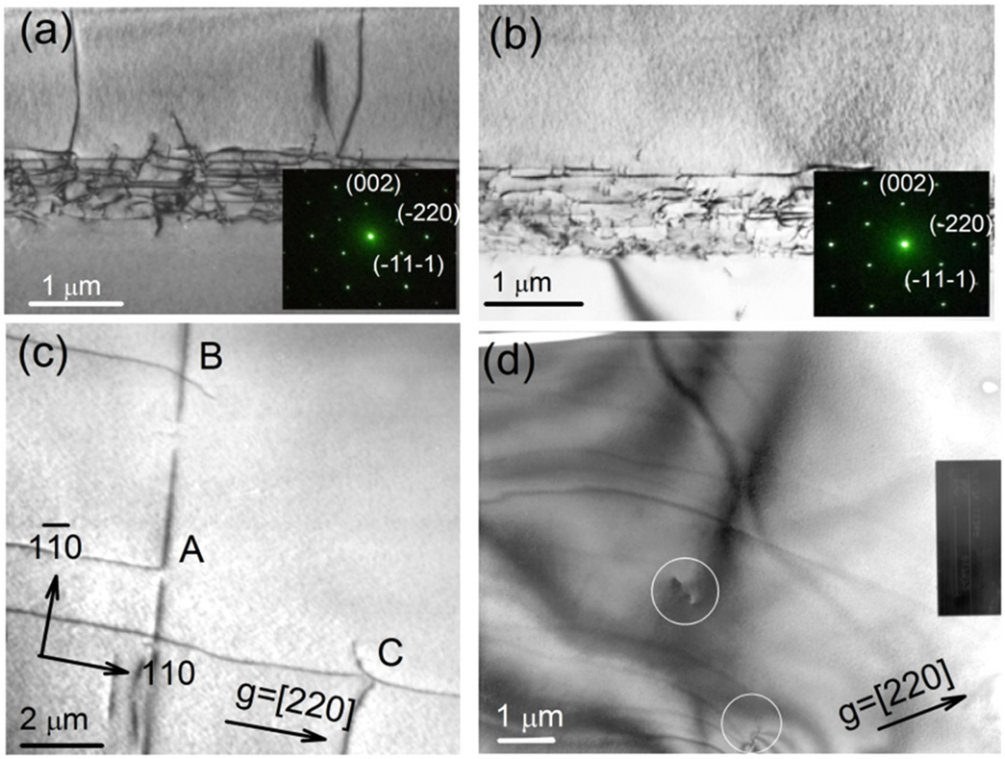

Figure 3. Cross-sectional bright field TEM images of $In_{0.3}Ga_{0.7}As$ film grown on the (a) 6-SG, (b) 8-SG $In_xGa_{1-x}As$ buffer layers, with inset figures showing corresponding SAED patterns of the top $In_{0.3}Ga_{0.7}As$. Plan-view TEM image observed at the *interface* between $In_{0.3}Ga_{0.7}As$ and 8-SG $In_xGa_{1-x}As$ buffer layers; (c) plan-view TEM image observed *within* $In_{0.3}Ga_{0.7}As$, with 8-SG buffer layers underneath (d), where the two TDs are marked.

To investigate more details about how TDs were blocked in the designed buffer, cross-sectional TEM images were collected on $In_{0.3}Ga_{0.7}As$ with 6- and 8-SG layers, as shown in figures 3(a) and (b), respectively. It appears that TDs were not blocked well in the $In_{0.3}Ga_{0.7}As$ with 6-SG layers, as they almost reached the free surface by propagating outside the buffer structure. In contrast, the 8-SG structure locked TDs more efficiently. In addition, we found that the selected area electron diffraction (SAED) pattern of the $In_{0.3}Ga_{0.7}As$ became brighter and more symmetric during the transition from 6-SG [inset of figure 3(a)] to 8-SG layers [inset of figure 3(b)]. This can be understood because by adding two more SG layers, the structural relaxation threshold was met for TDs to fall into annihilation reactions [13, 14], leading to better film quality of the $In_{0.3}Ga_{0.7}As$. As previously known, in a lattice-mismatched zinc blend crystal with a low misfit train, strain relaxation occurs primarily by the formation of 60° a/2 ⟨110⟩ {111} misfit dislocations [16]. At the end of every MD, TD segments are generated and often find their way by penetrating into active layers [16]. If TDs are glissile, then for a [001] growth (the orientation of the used GaAs substrate here) they will glide over one of four {111} slip planes. Thus, there are four unique {111} planes and six unique ⟨110⟩ directions. Considering that the dislocation Burgers vector can be either positive or negative, there will be 12 possible Burgers vectors. Finally, a glissile dislocation with an a/2 ⟨110⟩ Burgers vector can have its line in one of two possible {111} planes, and thus there are a total of 24 specific dislocation Burgers vector/slip plane combinations [13]. In all possible combinations, only certain TDs that have

anti-parallel Burger vectors can fall into annihilation reactions, while the remaining ones may result in new TDs segments through fusion reactions, and these new TDs segments tend to move up into active layers. Therefore, the purpose of multiple discrete layers in metamorphic growth is to increase the probability of annihilation reactions among TDs. As can be seen in figures 3(a) and (b), both annihilation and fusion reactions between TDs within the SG structure were observed. Meanwhile, mobile TDs blocked by MDs process [28] were also observed. Figure 3(c) presents a plane-view TEM image taken at the interface between $In_{0.3}Ga_{0.7}As$ and the 8-SG $In_xGa_{1-x}As$ buffer, with a two-beam condition taken near a [001] zone axis with g (diffraction vector) = [220]. The image features a number of dislocation intersecting events. It is observed that a variety of interactions can take place upon dislocation intersecting. Two MDs (marked as A and B) with Burgers vectors of a/2⟨101⟩(111) and a/2 ⟨0–11⟩(1–11), fell into interaction along a MD gliding on ⟨1–10⟩ direction. No blocking interaction happened, and their TDs arms still glided up over the {111} glide planes. However, an interesting event near A, where the motion of the threading arm of an a/2⟨10-1⟩ (1-1-1) MD has been arrested, was observed. Figure 3(d) shows another plan-view TEM of the $In_{0.3}Ga_{0.7}As$/8-SG $In_xGa_{1-x}As$, where the image was particularly taken *within* the top $In_{0.3}Ga_{0.7}As$. Only two TDs were observed, which derived a TDs density to be as low as $3 \times 10^6\ cm^{-2}$ (This order of magnitude is slightly higher than that observed by an etch pit density (EPD) approach ($\sim 7 \times 10^5\ cm^{-2}$) with optical microscopy over a much larger area, as presented in figure 1 of the supplementary materials. However, considering that the optical microscope might have missed features in a very local area, we rather believe that the TD density is on the order of $\sim 10^6\ cm^{-2}$ as estimated from TEM, for the reason of being conservative and scientifically rigorous). In fact, the TD density here is comparable with those also using metamorphic growth [19, 22, 24]. From TEM analyses, we understand that an 8-SG buffer is necessary to achieve better crystal quality of the $In_{0.3}Ga_{0.7}$, because of effective TD blocking processes

3.2. Effects of temperature on phase separation in $In_{0.5}Ga_{0.5}As$ epilayer

Using the same growth conditions, $In_{0.5}Ga_{0.5}As$ (500 nm)/$In_xGa_{1-x}As$ ($x = 0.3$–0.5) epifilms were grown continuously on $In_{0.3}Ga_{0.7}As$/$In_xGa_{1-x}As$($x = 0$–0.3)/GaAs at which $In_xGa_{1-x}As$ ($x = 0.3$–0.5) served as the second buffer structure to further release misfit strain between $In_{0.5}Ga_{0.5}As$ and $In_{0.3}Ga_{0.7}As$. However, given a growth temperature of 475 °C, the crystal quality and surface morphology of the top $In_{0.5}Ga_{0.5}As$ were poor, as confirmed by the cross-sectional TEM image of figure 4(a). The EDX patterns detected at points 1, 2, and 3 in figure 4(a) were used to estimate the local concentrations of In and Ga, and the results were summarized in table 1. Concentrations at points 1 and 2 were slightly lower than expected compared to those at point 3. It is therefore the deficient-In (excessive-Ga) at these microregions that caused phase separation responsible for the poor crystal quality and surface morphology [19].Thermodynamic and kinetic approaches have been recommended to circumvent this problem [29]; this means changing the growth temperature can possibly avoid phase separation. If there is a certain driving force that creates compositional variations on the surface, kinetic constraints may prevent this composition variation from forming. To avoid phase separation during film growth, controlling the atomic diffusion length on the surface (i.e., surface migration length) is a key parameter [30]. Alternatively, an appropriate increase in V/III precursor ratio was found to suppress the phase separation [31]. The V/III precursor ratio was kept as high as 90 here to reduce carbon contamination concentration as well as improving surface morphology [32], and the growth temperature was the adopted parameter (related to kinetic control) to investigate the phase separation in this work. As shown in figure 4(b), the phase separation still occurred in the top $In_{0.5}Ga_{0.5}As$ at a growth temperature of 485 °C, as manifested by those non-uniform microregions. However, it was suppressed profoundly by raising up the growth temperature to 505 °C, as confirmed by figure 4(c). Because the surface migration length is strongly dependent on growth temperature [33], the increased growth temperature will enhance the surface diffusivity of atoms, therefore increasing surface migration length and reaching an optimized microstructure for the film. Figure 5(a) shows (004) ω-2θ XRD scans of the top $In_{0.5}Ga_{0.5}As$ with a growth-temperature dependency (475, 485, and 505 °C). Cleary, from a different structural analysis, the crystal quality of the top $In_{0.5}Ga_{0.5}As$ was further shown to be much improved by an appropriate increase of the growth temperature. Figures 5(b)–(d) present the AFM images of the same sets of samples. The rms roughness decreased from 5.8 nm for the $In_{0.5}Ga_{0.5}As$ grown at 475 °C, down to 2.4 nm for the $In_{0.5}Ga_{0.5}As$ grown at 505 °C. However, further increase in growth temperature would deteriorate surface morphology as well as the crystal quality of the film.

3.3. Effects of platform thickness on $In_{0.5}Ga_{0.5}As$ epilayer

Previous report have shown that the use of a thick $In_{0.3}Ga_{0.7}As$ platform inserted between two $In_xGa_{1-x}As$ buffer layers resulted in a better crystal quality of the top $In_{0.5}Ga_{0.5}As$ [20]. However, a thick buffer/platform indicates a high production cost undesired for industry. Therefore, it is a great challenge to reduce the platform thickness to be as thin as possible without sacrificing its functionality. In this section, we investigated the thickness effects of an $In_{0.3}Ga_{0.7}As$ platform on the crystal quality of the top $In_{0.5}Ga_{0.5}A$. Two samples were grown at 505 °C using $In_{0.3}Ga_{0.7}As$ as the platform with the thickness of 1.2 and 0.3 μm. Figure 6(a) shows the TEM image of the $In_{0.5}Ga_{0.5}As$ using a 1.2 μm $In_{0.3}Ga_{0.7}As$ platform Compared to the sample using a 0.3 μm $In_{0.3}Ga_{0.7}As$ platform [figure 4(c)], the one containing a thicker platform exhibited better crystal quality in terms of microstructure. This can be further validated by the XRD rocking curve (004) scans [figure 6(b)], where the FWHM was reduced from 700 arcsec to 560 arcsec along with increasing the platform thickness. It is known that the platform is used as visual substrate for releasing misfit strain

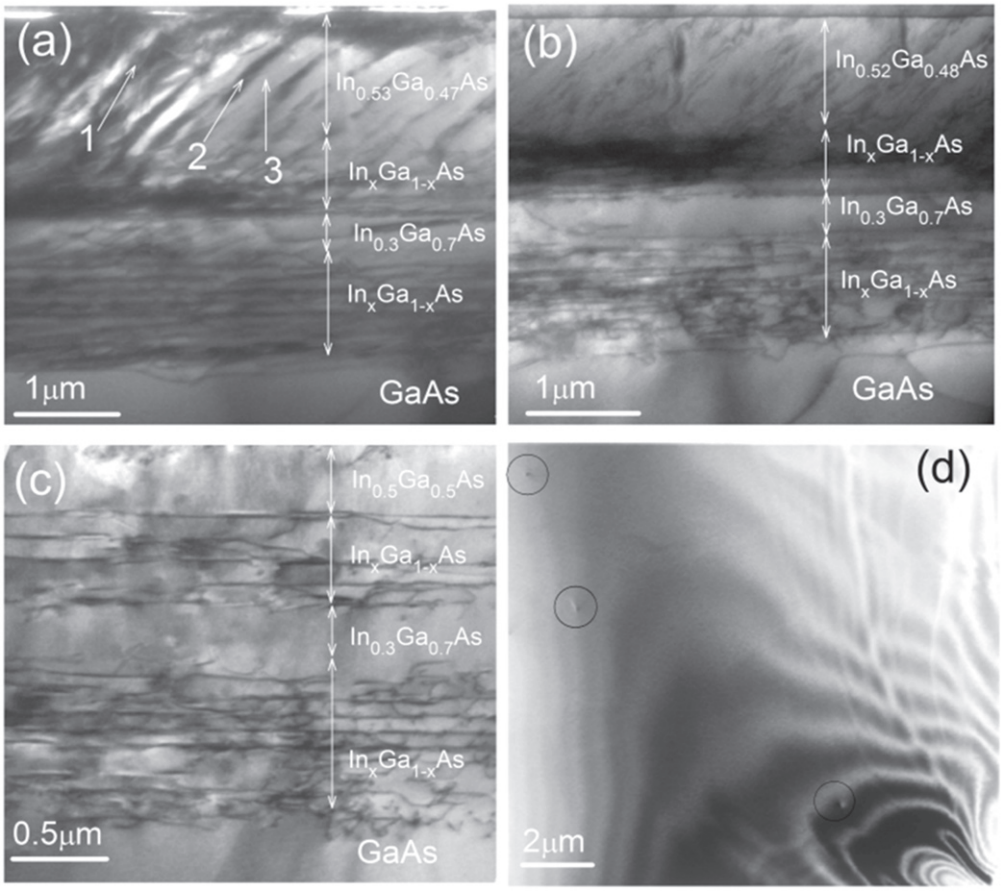

Figure 4. Cross-sectional TEM images of $In_{0.5}Ga_{0.5}As$ epifilms grown at 475 °C (a), 485 °C (b), and 505 °C (c) using optimized $In_xGa_{1-x}As$ buffer layers. (d) Plan-view TEM image of $In_{0.5}Ga_{0.5}As$ epifilm grown at 505 °C. Circles indicate the positions of the TDs.

Table 1. EDX compositional analyses at points 1, 2, and 3 in figure 4(a).

Detected point	In content (%)	Ga content (%)	As content (%)
1	20.64	28.77	50.59
2	21.33	29.31	49.36
3	26.25	24.4	49.35

in graded buffer layers. It blocked TDs from penetrating from under to above layers with high strain relaxation. To provide more insights into the relationship between crystal quality and strain relaxation, we analyzed the structural parameters and relaxation information of the $In_{0.5}Ga_{0.5}As$ from the data of reciprocal space map (RSM) scans on (115) ω-2θ reflection of substrate. The degree of strain relaxation R can be estimated using a related formula [26] (see a detailed equation [equation (6)] in the supplementary materials).

Figures 6(c) and (d) illustrate the (115) RSM of $In_{0.5}Ga_{0.5}As$ using the 1.2 and 0.3 μm platforms, respectively. The in-plane lattice constant, $a_{//}$ was 5.848 Å for the $In_{0.5}Ga_{0.5}As$ using the 1.2 μm platform, while it was 5.828 Å for the $In_{0.5}Ga_{0.5}As$ using the 0.3 μm platform. The R values of the $In_{0.5}Ga_{0.5}As$, therefore, were estimated to be 96% and 85% as using the 1.2 and 0.3 μm platforms, respectively. However, though the use of a thicker platform can improve the crystal quality and strain relaxation degree of the $In_{0.5}Ga_{0.5}As$, unfortunately the surface roughness followed an opposite trend. Figures 7(a) and (b) show the AFM images of the $In_{0.5}Ga_{0.5}As$ using the 1.2 and 0.3 μm platforms, respectively, where the RMS roughness increased from 2.4 nm to 3.1 nm with increasing the platform thickness. This is related to the strain relaxation within the $In_{0.5}Ga_{0.5}As$. It is known that the strain will be relieved by the formation of MDs [12, 15]. Therefore, the rougher surface can be attributed to a higher relaxation degree, which resulted from enormous MDs generated by a thicker platform. On the contrary, a smoother surface is a consequence of fewer MDs yielded by a thinner platform. We use figure 4(d), a plane-view TEM image of the $In_{0.5}Ga_{0.5}As$ using the 0.3 μm platform, to estimate the dislocation density. Only three TDs were observed (marked by the circles) in an area of about 200 μm^2, which derived a TD density of 2×10^6 cm^{-2} for the $In_{0.5}Ga_{0.5}As$. In terms of TD density and surface roughness, the data suggest that the good quality of the $In_{0.5}Ga_{0.5}As$ film can be substantially preserved by reducing the platform thickness to 0.3 μm. This provides an absolute advantage, similar to reducing the total buffer thickness ($In_xGa_{1-x}As/In_{0.3}Ga_{0.7}A/In_xGa_{1-x}As$) to 2.3 μm. It is noteworthy that this scalability is greatly superior to those of the forefront works using MOCVD [22, 24].

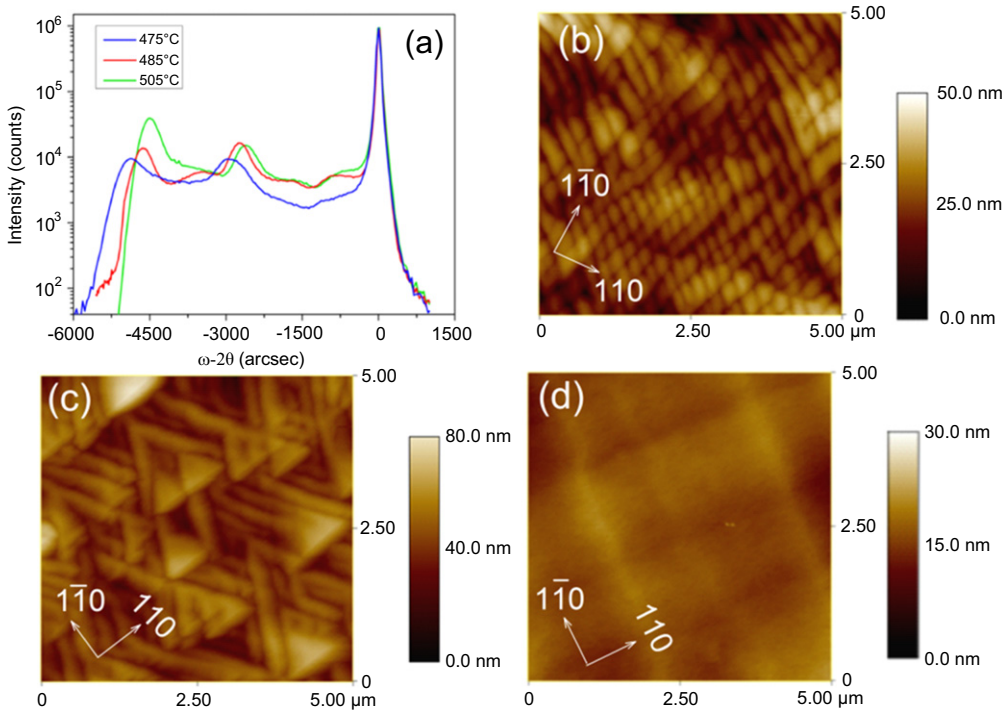

Figure 5. (a) (004) ω-2θ scan XRDs of $In_{0.5}Ga_{0.5}As$ epifilms grown at different growth temperatures. AFM images of $In_{0.5}Ga_{0.5}As$ epifilms grown at 475 °C (b), 485 °C (c), and 505 °C (d).

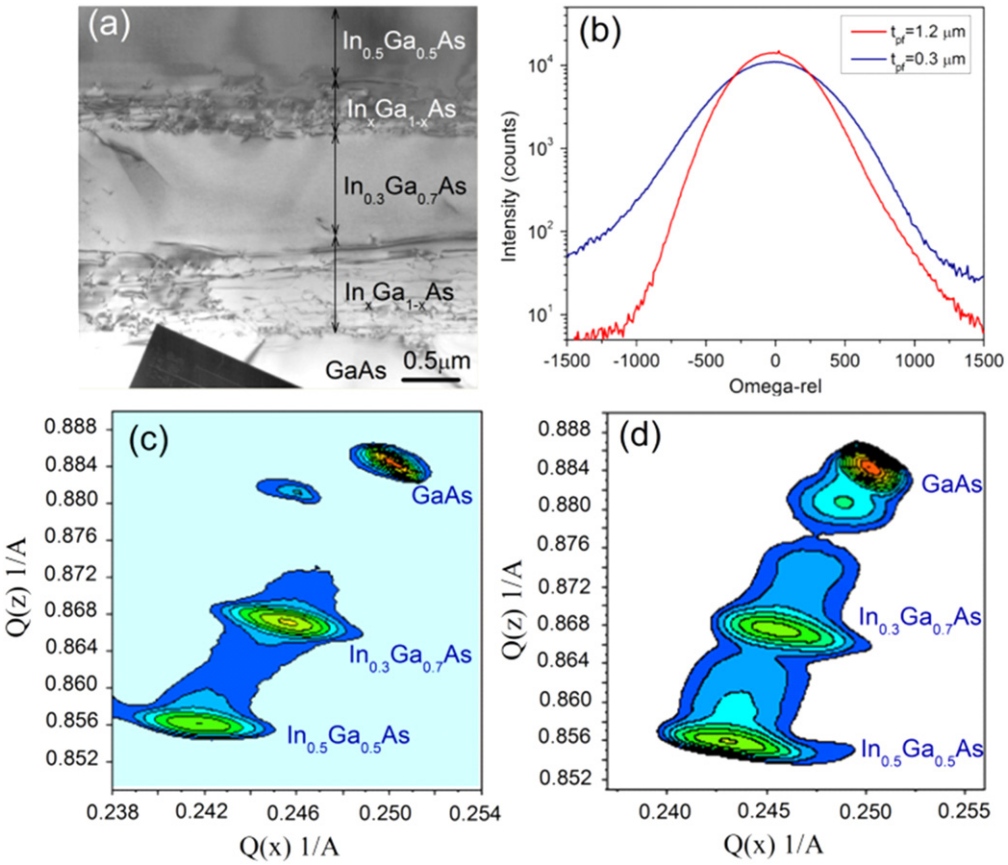

Figure 6. (a) Cross-sectional TEM image of $In_{0.5}Ga_{0.5}As$ epifilm using a 1.2 μm $In_{0.3}Ga_{0.7}As$ platform. (b) (004) XRD rocking curves of $In_{0.5}Ga_{0.5}As$ epilayers using 1.2 μm and 0.3 μm $In_{0.3}Ga_{0.7}As$ platforms. RSM images of $In_{0.5}Ga_{0.5}As$ epifilms using (c) 1.2 μm (d) and 0.3 μm $In_{0.3}Ga_{0.7}As$ platforms.

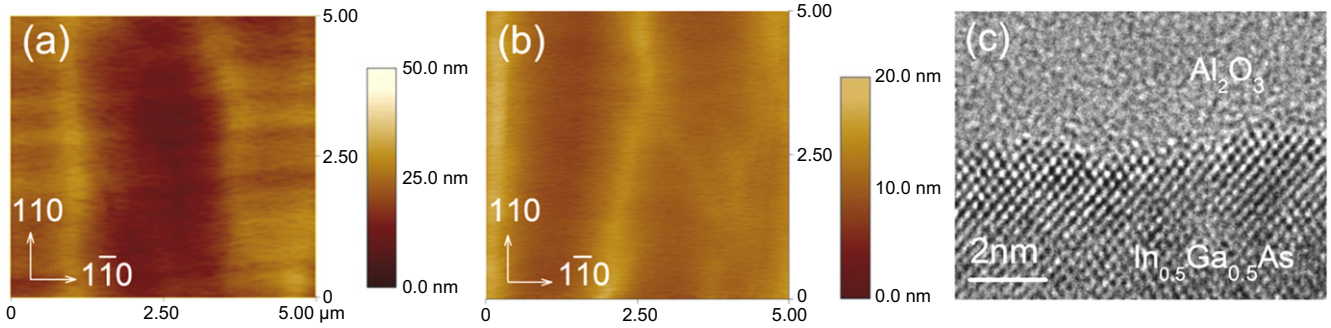

Figure 7. AFM images of $In_{0.5}Ga_{0.5}As$ epifilms using(a) 1.2 μm and (b) 0.3 μm $In_{0.3}Ga_{0.7}As$ platforms.(c) Cross-sectional HRTEM image observed at the interface of $Al_2O_3/In_{0.5}Ga_{0.5}As$ in a MOSCAP.

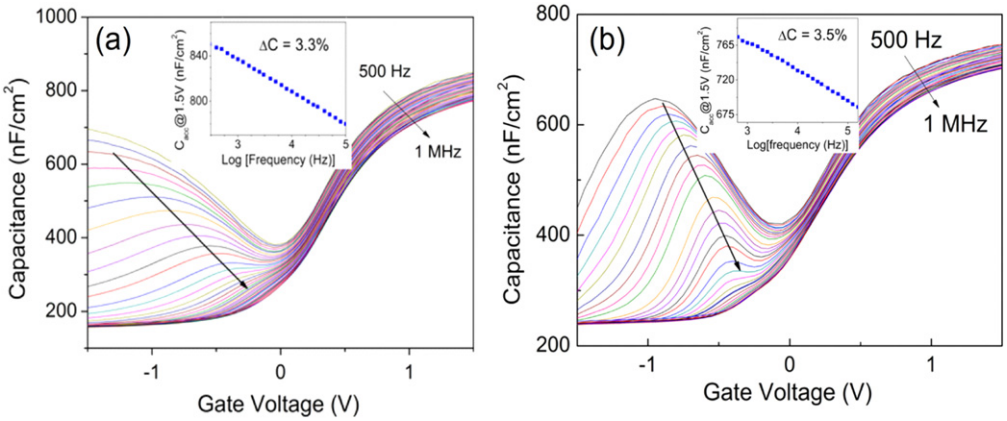

Figure 8. Multi-frequency C–V curves of MOSCAP devices using (a) 0.3 μm $In_{0.3}Ga_{0.7}As$ and (b) 1.2 μm $In_{0.3}Ga_{0.7}As$ platforms. Inset figures show the frequency dispersion at a positive bias of 1.5 V of the two devices.

3.4. $In_{0.5}Ga_{0.5}As$-based MOSCAP device

A MOSCAP based on the $In_{0.5}Ga_{0.5}As/In_xGa_{1-x}As$/0.3 μm -$In_{0.3}Ga_{0.7}As/In_xGa_{1-x}As$/GaAs structure was fabricated to test the device performance. Figure 7(c) presents a cross-sectional high-resolution TEM (HRTEM) image taken at the interface between the $In_{0.5}Ga_{0.5}As$ semiconductor and an Al_2O_3 oxide layer. We use this figure to confirm that the $In_{0.5}Ga_{0.5}As$ surface oxide layer was completely removed using HCL 4% solution for surface treatment prior to Al_2O_3 deposition. Figure 8(a) shows the multi-frequency C–V response of the $In_{0.5}Ga_{0.5}As/In_xGa_{1-x}As$/0.3 μm -$In_{0.3}Ga_{0.7}As/In_xGa_{1-x}As$/GaAs device (defined as 0.3 μm device). We also fabricated a MOSCAP with an $In_{0.5}Ga_{0.5}As/In_xGa_{1-x}As$/1.2 μm -$In_{0.3}Ga_{0.7}As/In_xGa_{1-x}As$/GaAs structure (defined as 1.2 μm device), and present its multi-frequency C–V response in figure 8(b). The frequency dispersion (3.5%) of the 1.2 μm device at a given positive bias is slightly higher than that of the 0.3 μm device. In addition, a significant reduction of the inversion hump is also observed in the 0.3 μm device compared to the 1.2 μm device. The small frequency dispersion and weak inversion hump indicate the good quality of dielectric/semiconductor interfaces, and therefore it suggests that the 0.3 μm platform is a better choice. In fact, the 0.3 μm device displays good C–V responses in distinct accumulation, depletion, and inversion regions, which are actually comparable to high k/MBE-$In_{0.53}Ga_{0.47}As$/InP MOSCAPs reported by other groups [34, 35]. The frequency dispersion in the accumulation regime [as shown in the inserted figure in figure 8(a)] of 3.3% per decade of the 0.3 μm device is comparable to that of lattice-matched $In_{0.5}Ga_{0.5}As$/InP MOSCAPs [36, 37]. Figure 9(a) illustrates bidirectional C–V responses of the 0.3 μm device at a frequency of 1 kHz. The hysteresis of 125 mV at flatband voltage was relatively small compared to that of the $Al_2O_3/In_{0.5}Ga_{0.5}As$/InP MOSCAP device [38], owing to the reduction in oxide-related traps on the surface of $In_{0.5}Ga_{0.5}As$ [39]. Conductance performance was tested over the 0.3 μm device, as well. The normalized parallel conductance ($G_p/\omega qA$) was determined from the measured impedance [40] (see a detailed equation [equation (7)] in the supplementary materials). The 2D contour plot of parallel conductance as a function of bias voltage and measurement frequency [41] of the 0.3 μm device is shown in figure 9(b). From the figure, the conductance peak maximum (the white dash line) shifted to afrequency regime lower than 1 kHz, indicating that the movement of Fermi level into a lower part of InGaAs bandgap is possible [42]. The interface trap density (D_{it}) can be analyzed using the equivalent circuit of a MOS capacitor for interface traps with a single energy level in the band gap [39] [see detailed equations (equations (8)–(10)] in the supplementary materials). The D_{it} profile of the 0.3 μm device extracted by the conductance method is shown in figure 9(c). From the figure, D_{it} values of

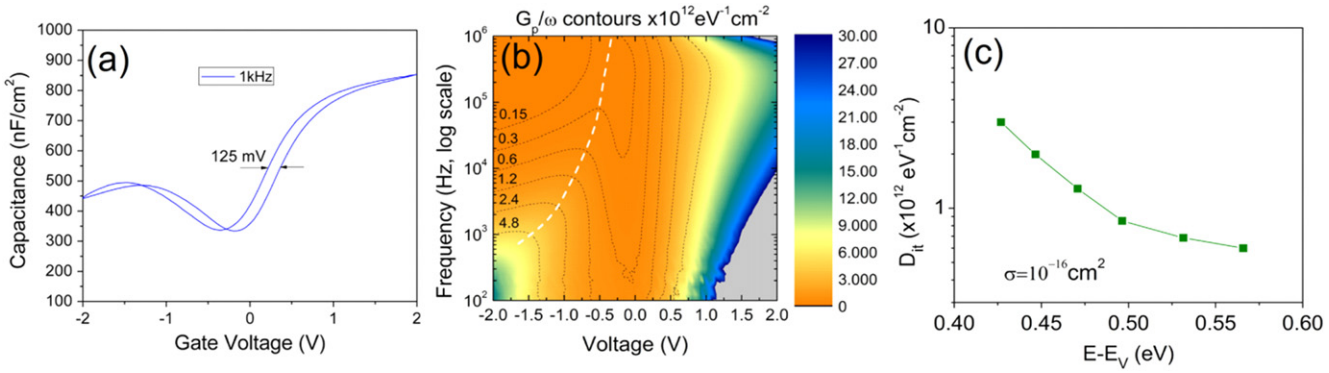

Figure 9. (a) Bidirectional C–V responses, (b) normalized parallel conductance contour map G-V, and (d) distributions of interface trap density versus energy of $Al_2O_3/In_{0.5}Ga_{0.5}As/In_xGa_{1-x}As(x = 0.3–0.5)/0.3\ \mu m\ In_{0.3}Ga_{0.7}As/In_xGa_{1-x}As(x = 0–0.3)$/GaAs-based MOSCAP.

$7 \times 10^{11} - 3 \times 10^{12}\ eV^{-1}\ cm^{-2}$ in the energy range of 0.57–0.42 eV above the $In_{0.5}Ga_{0.5}As$ valence band maximum were obtained. These D_{it} values are also comparable to those of lattice-matched $Al_2O_3/In_{0.5}Ga_{0.5}As$/InP grown by MBE method [34, 43]. The promising performances demonstrated here suggest a successful adoption of the metamorphic structure grown by MOCVD over such a scalability, which is the central value of this study.

4. Conclusion

In summary, we have successfully fabricated a high-quality $In_{0.5}Ga_{0.5}As$-based MOSCAP using the MOCVD metamorphic growth technique. The use of multiple discrete layers in metamorphic growth reduced the TD density to an acceptable level, and therefore improved the top $In_{0.5}Ga_{0.5}As$ film quality as a consequence. TD blocking mechanisms were thoroughly studied and discussed from TEM analyses to provide a full understanding of the microstructural world in such a unique structure. Kinetic constraints that can avoid compositional variation were achieved using an optimized growth temperature of 505 °C, because of a good control of atomic diffusion on the surface. Under this growth condition, the microstructural properties of a minimum number (8) of the SG layer were further optimized through a precise control of the metamorphic growth, therefore achieving a high-quality $In_{0.5}Ga_{0.5}As$ epifilm on a GaAs substrate. As an important consequence, the whole buffer structure can be largely scaled down to a competitive level that reduced the production cost and achieved device miniaturization. The practicability of the designed structure was evaluated by testing several electrical performances of the formed MOSCAP, such as C–V responses, conductance and D_{it} values. These performances were comparable to those of $Al_2O_3/In_{0.5}Ga_{0.5}As$/InP with lattice coherency in nature.

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