Evaluation of Sub-0.2 V High-Speed Low-Power Circuits Using Hetero-Channel MOSFET and Tunneling FET Devices

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***Abstract*—This paper investigates the feasibility of sub-0.2 V high-speed low-power circuits with hetero-channel MOSFET and emerging Tunneling FET (TFET) devices. First, the device designs and characteristics of hetero-channel MOSFET and TFET devices are discussed and compared. Due to the significant leakage current of ultra-low V_T hetero-channel MOSFET devices, assist-circuits are required for hetero-channel MOSFET-based circuits to operate at 0.2 V. Second, the delay, dynamic energy and the Standby power of hetero-channel TFET-based and MOSFET-based logic circuits including Inverter, NAND, BUS Driver, and Latch are analyzed and evaluated. The results indicate that hetero-channel TFET-based circuits with Dual Oxide (DOX) device design to reduce the Miller capacitance provide the potential to achieve high-speed low-power operation at $V_{DD} = 0.2$ V, while the use of assist-circuits in MOSFET-based design improves the delay and dynamic energy at the expense of increased device count, circuit area, and large Standby and sleep-mode leakage power. Finally, the impacts of temperature and process variations on TFET-based and MOSFET-based logic circuits are discussed.**

***Index Terms*—Hetero-channel MOSFET, high-speed, low-power, tunnel FET.**

I. Introduction

REDUCING the power consumption in processors, mobile devices and bio-medical electronics is one of the most challenging tasks. Voltage scaling is an efficient way to achieve low power consumption. However, due to the physical limit of the subthreshold swing of MOSFET device and the increased variation as scaling, continual reduction of supply voltage causes dramatic increase in leakage current [1], [2]. Thus the need of novel devices and circuits are indispensable for sub-0.2 V high-speed low-power circuits. Recently, an advanced assist-circuit using the dual-supply dual-V_T technique is proposed by A. Kotabe *et al.* [3] to enable high-speed low-power operation for MOSFET devices in subthreshold region. The concept is to use lower supply and lower (near zero) V_T MOSFET in the core circuits to enable high-speed and low dynamic energy consumption during the operation, while utilizing the higher supply and higher V_T MOSFET to reduce the leakage current in Standby. In this circuit topology, the assist-circuit inevitably increases the device count and chip area, and on-chip supply generation circuit (Level Shifter) is needed.

On the other hand, TFET device which utilizes the band-to-band tunneling (BTBT) as the major conduction mechanism is considered to be one of the most promising devices to replace MOSFET device for ultra-low voltage operation due to its steep (<60 mV/dec at room temperature) subthreshold slope [4]–[6]. The device structures and band diagrams of N-type TFET and P-type TFET describing the conduction mechanism are shown in Fig. 1(a) and Fig. 1(b), respectively. The superior subthreshold slope and better $I_{on} - I_{off}$ characteristics of TFET device provides substantial advantages in designing high-speed low-power circuits for $V_{DD} = 0.2$ V operation. However, due to the source-channel barrier in TFET device, the TFET device capacitance is dominated by C_{gd} (Miller capacitance) in the weak and strong inversion region, which is substantially larger than that in the MOSFET device [7]. In MOSFET device, once the inversion channel is formed, the source and drain are "connected" by the conducting inversion channel, and the gate-to-channel capacitance is divided/partitioned into C_{gs} and C_{gd}. For TFET device, due to the source-channel barrier, the gate-to-channel capacitance manifests itself almost entirely as C_{gd}. The large Miller capacitance C_{gd} in TFET device causes significant overshoot and undershoot during circuit switching to degrade the switching delays and dynamic energy consumption, thus undermining the advantage of steep subthreshold slope of TFET devices. From circuit point of view, the Miller capacitance of TFET device is of particular importance and should be reduced. In our previous study [8], the device design techniques for improving the device characteristic and reducing C_{gd} of TFET device are investigated. Among the techniques, the Dual Oxide (DOX) approach, where low-κ gate dielectric is used near the drain side to reduce the Miller capacitance, provides better improvements in both the delay and dynamic energy. In this work, we use DOX TFET devices for 0.2 V circuit designs.

The rest of the paper is organized as follows. Section II describes the device designs and TCAD simulation methodology of hetero-channel TFET and MOSFET devices. Section III evaluates the feasibility of sub-0.2 V high-speed low-power circuits using hetero-channel MOSFET and TFET devices. Four cases are considered: (1) the nominal hetero-channel MOSFET-based circuits, (2) hetero-channel MOSFET-based circuit with dual supply, dual V_T assisted circuits [3], (3) nominal hetero-channel TFET-based circuits and (4) hetero-channel TFET-based circuits using DOX TFET devices. Logic circuits

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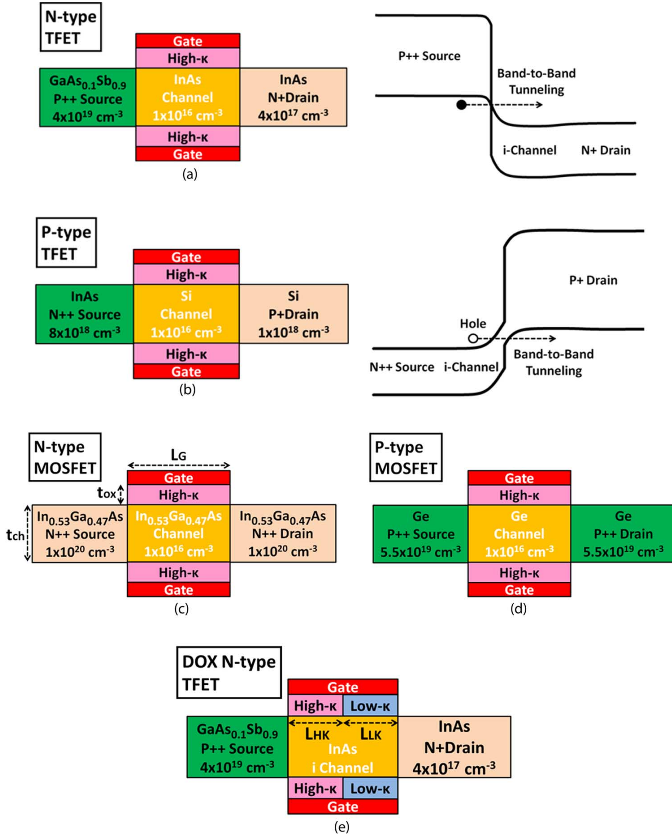


Fig. 1. Device structure of tied-gate (double-gate) FinFET: (a) N-type TFET and the corresponding ON-state band structure, (b) P-type TFET and the corresponding ON-state band structure, (c) N-type MOSFET, (d) P-type MOSFET, and (e) N-type TFET using Dual Oxide (DOX) technique.

including Inverter, NAND, BUS Driver, and Latch are analyzed and evaluated. Section IV discusses the impacts of temperature and process variations on the hetero-channel TFET-based and MOSFET-based logic circuits. Section V concludes the paper.

II. Device Designs and TCAD Simulation Methodology

Hetero-channel MOSFETs with III-V and Ge semiconductors as channel materials are promising candidates for future CMOS technology to replace conventional Si MOSFETs due to their high mobility, and recent studies have demonstrated the successful fabrication of InGaAs channel (N-type) and Ge channel (P-type) MOSFET devices on the Si substrate [9], [10]. The terminology "hetero-channel MOSFET" refers to MOSFET devices with non-Si channel (such as III-V or group IV materials) grown on the Si-platform. In this work, we consider the n-InGaAs MOSFET and p-Ge MOSFET devices. On the other hand, smaller bandgap and direct bandgap materials such as III-V compounds are possible choices for boosting TFET performance [11], [12]. In this work, we consider the GaAsSb/InAs NTFET and InAs/Si PTFET devices. The device designs and structures of the N-/P-type MOSFET device, N-/P-type TFET device, and TFET device using Dual Oxide (DOX) technique are shown in Fig. 1. FinFET tied-gate (double-gate) structures are used for all five devices in Fig. 1. The device parameters are listed below: channel length $(L_G) = 22\ \mathrm{nm}$, channel thickness $(t_{ch}) = 5\ \mathrm{nm}$, high-$\kappa$ gate oxide $(t_{ox}) = 2.5\ \mathrm{nm}$ with HfO_2 as the gate dielectric $(\mathrm{permittivity} = 22)$ and SiO_2 as the low-κ gate dielectric $(\mathrm{permittivity} = 3.9)$, the length of the high-κ gate oxide (L_{HK}) and of the low-κ gate oxide (L_{LK}) are 5 nm and 17 nm, respectively for DOX TFET. To

TABLE I
Material Parameters in This Work

Parameters	$GaAs_{0.1}Sb_{0.9}$	InAs	$In_{0.53}Ga_{0.47}As$	Ge
E_G [eV]	0.84	0.53	1.08	0.79
Electron affinity [eV]	4.10	4.92	4.52	3.96
A_{path} [$cm^{-3}s^{-1}$]	$1.58x10^{20}$	$1.48x10^{20}$	--	--
B_{path} [$cm^{-3}s^{-1}$]	$6.45x10^{6}$	$2.4x10^{6}$	--	--
eDOS [cm^{-3}]	$1.95x10^{17}$	$8.72x10^{16}$	$2.54x10^{17}$	$1.02x10^{19}$
hDOS [cm^{-3}]	$6.84x10^{18}$	$6.66x10^{18}$	$7.51x10^{18}$	$5.92x10^{18}$

accurately assess the device characteristics and circuit behaviors of high mobility channel n-InGaAs and p-Ge MOSFET devices, the mobility model and Schenk band-to-band tunneling (BTBT) model capturing the leakage current are calibrated with the experimental data in [13]–[15] for mixed-mode TCAD simulations [17]. For heterojunction TFET devices, the nonlocal BTBT model which is applicable for arbitrary tunneling barrier with non-uniform electric field is used. The tunneling paths are dynamically determined according to the gradient of the band energy. The band-gap widening due to quantum confinement is considered in this work and the BTBT model parameters, A_{path} and B_{path}, which are important material-related factors determining the band-to-band generation rates are referenced from [16] in which these parameters are calibrated with the NEGF (Non-Equilibrium Green's Functions)-based approach for heterojunction Tunneling FET devices. The detailed material parameters used in this work are listed in Table I.

For TFET device, the DOX technique (Fig. 1(e)) uses different gate dielectric material at the drain and source side. By placing the high-κ gate oxide at the source side and low-κ gate oxide at the drain side, the C_{gd} and C_{inv} can be reduced while retaining the ON-OFF characteristics of the TFET device as shown in Fig. 2(a) and Fig. 2(b). Simulated I_{on} and I_{off} with different lengths of high-κ gate oxide (L_{HK}) are shown in Fig. 2(a). The I_{on} degrades about 7% when L_{HK} shrinks to 5 nm, while I_{off} shows an inflection point at about half of the channel length. This is because in the ON state, the BTBT occurs near the source-channel junction, the shrinkage of L_{HK} in which the energy band of the channel region controlled by the high-κ gate oxide does not significantly affect the band-to-band tunneling junction. However, as the L_{HK} becomes smaller to 5 nm, the energy band near the source-channel tunnel junction becomes retarded (Fig. 2(d)), resulting in larger tunneling length (L_{tunnel}) and thus degrading I_{on}. The detailed band diagrams showing the increased tunneling length as the L_{HK} decreases and the corresponding Hole-Band-to-Band Tunneling Rate are shown in Fig. 2(c) and Fig. 2(d), respectively. For I_{off}, as L_{HK} reduces to about half of the channel length, the channel region controlled by the high-κ gate oxide near the drain side becomes smaller, thus the energy band at the drain side gets retarded, leading to I_{off} increase as indicated by the gray dashed circle shown in Fig. 2(e). As L_{HK} continues to shrink, the influence of the high-κ gate oxide on the energy band of the source-channel junction becomes smaller, and I_{off} starts to decrease due to less BTBT leakage as indicated by

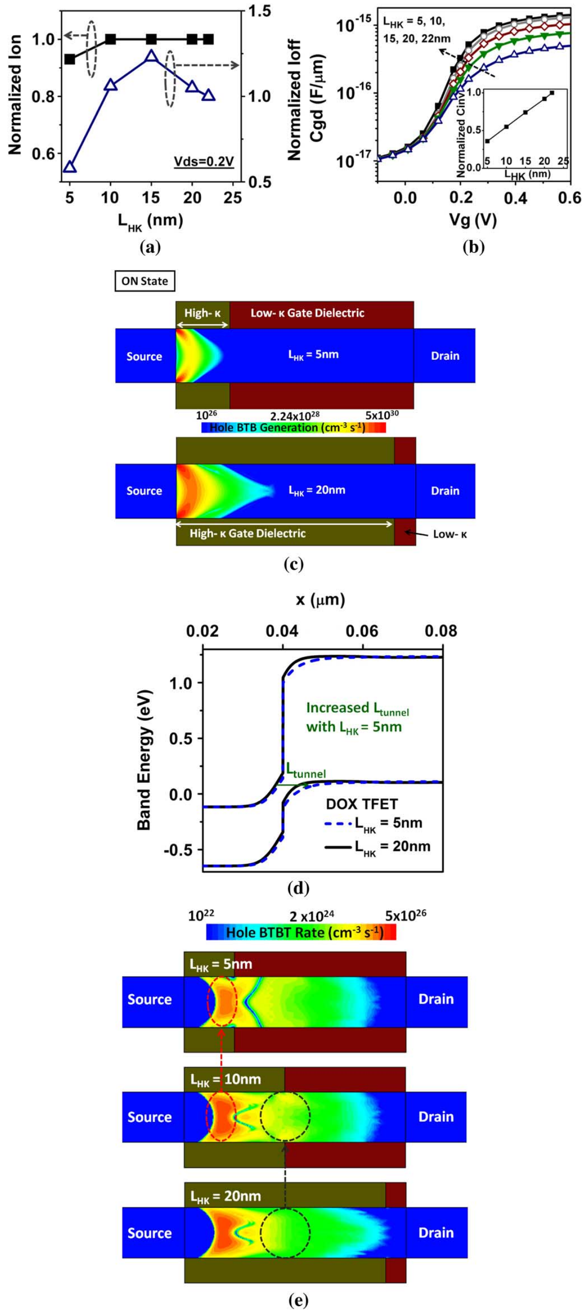


Fig. 2. (a) Normalized Ion-Ioff characteristic with different lengths of high-κ gate dielectric and (b) Cgd-Vg characteristic of TFET device using dual gate oxide (DOX) technique. The inset of (b) shows the C_{inv} improvement with L_{HK} when using the DOX technique. (c) Hole-Band-to-Band Tunneling (BTBT) Rate in the ON state for DOX TFET devices with $L_{HK} = 5$ nm and 20 nm, respectively. (d) Band diagrams of DOX TFET devices in the ON state with $L_{HK} = 5$ nm and 20 nm, respectively. (e) Hole-Band-to-Band Tunneling Rate in the OFF state for DOX TFET devices with $L_{HK} = 5$ nm, 10 nm and 20 nm. The gray dashed circles indicate the increased I_{off} with $L_{HK} = 20$ nm decrease to 10 nm, while the red dashed circles indicate the decreased I_{off} with $L_{HK} = 10$ nm decrease to 5 nm.

the red dashed circle shown in Fig. 2(e), thus resulting in the inflection in Fig. 2(a). In Fig. 2(b), we can clearly see that the use of low-κ gate oxide at the drain side can effectively reduce C_{gd} and C_{inv}, and the reduction of capacitances becomes more pronounced as L_{HK} becomes smaller. As shown in the inset of Fig. 2(b), for $L_{HK} = 5$ nm, C_{inv} can be reduced to 30% of the nominal C_{inv} of TFET without the DOX technique. From CV/I point of view, the DOX TFET provides substantial advantages for improving the circuit performance and energy, in additional to the significant benefit of reducing the overshoot/undershoot during switching. In this work, we choose $L_{HK} = 5$ nm for of the DOX TFET. Simulated Id-Vg characteristics of the hetero-channel MOSFET and TFET device are shown in Fig. 3. The hetero-channel MOSFET with lower threshold voltage V_{TL} is designed to have the same threshold voltage as that of the N-type TFET device ($V_{TL} = 50$ mV). The higher threshold voltage of the hetero-channel MOSFET ($V_{TH} \sim 150$ mV) is designed for a target leakage current I_{off} near $1 nA/\mu m$. The Id-Vg of the DOX TFET is quite close to the nominal TFET with slight degradation in I_{on}. Note that here we use constant-current defined threshold voltage, and we adjust the work functions for TFET and MOSFET devices to attain similar threshold voltages.

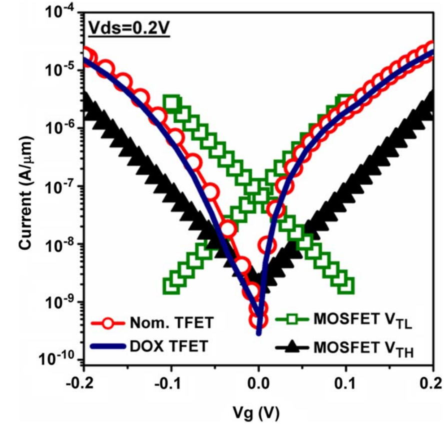


Fig. 3. Id-Vg characteristics of hetero-channel MOSFET and TFET devices.

III. Sub-0.2 V High-Speed Low-Power Circuits

In this section, high-speed low-power circuits consisting of nominal hetero-channel MOSFET device, hetero-channel MOSFET device with dual supply, dual V_T assisted circuits, nominal hetero-channel TFET device and hetero-channel DOX TFET device are comprehensively analyzed and compared using mixed-mode TCAD simulations for sub-0.2 V operation. In the following sections, the word "hetero-channel" will be omitted for simplicity of description, while it is to be understood that "hetero-channel" devices as shown in Fig. 1 are used.

A. NAND

Fig. 4(a) shows the schematics of the conventional two-way NAND structure for the nominal MOSFET, nominal TFET, and DOX TFET, while Fig. 4(b) is the schematics of two-way NAND structure using assist-circuits with dual supply, dual V_T MOSFET devices. In Fig. 4(b), V_{TL} MOSFET devices (indicated by blue colors) are used in the core circuit with lower supply voltage, whereas V_{TH} MOSFET devices are used for the power-gating devices in the assist-circuits with larger input swing to reduce Standby leakage and power. It should be noted that the use of V_{TL} P-type MOSFET power-gating devices [1] is to provide higher driving current. With its large input swing (V_{DD}), the Standby leakage current of the internal logic core can be reduced. Without a negative bias VNN, the V_{TH} N-type MOSFET power-gating device should be used to reduce the Standby leakage and power. Fig. 5 shows the transient waveforms of the two-way NAND during switching. The worst-case, bottom-switching pattern is considered. For the NAND structure with power-gating assist-circuit, a core supply $V_{DL} = 0.2$ V/0.1 V and a higher supply $V_{DD} = 0.3$ V/0.2 V

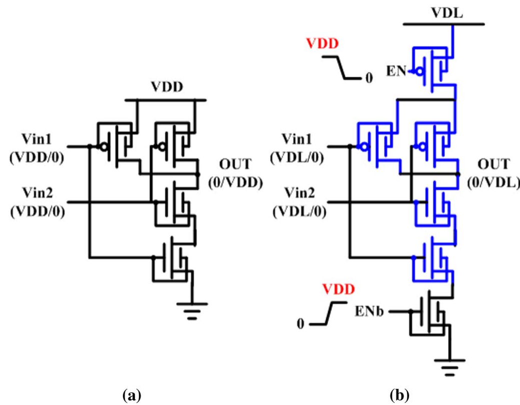


Fig. 4. Schematics of two-way NAND structures of (a) nominal MOSFET device, nominal TFET device, DOX TFET device, and (b) MOSFET device with assist circuits using V_{TH} powering-gating devices (indicated by black color).

are both considered. Fig. 6(a) and 6(b) show the dynamic energy versus delay and energy-delay product (EDP) versus Standby leakage power of TFET-based and MOSFET-based NAND circuits with two, three and four inputs, respectively. As shown, the utilization of dual supply $(V_{DD}/V_{DL} = 0.2\ V/0.1\ V)$, dual V_T technique improves both the delay and dynamic energy compared with the case using nominal MOSFET devices. While $V_{DD}/V_{DL} = 0.3\ V/0.2\ V$ provides the best delay, it consumes larger dynamic energy. The nominal TFET devices outperform the nominal MOSFET devices in operational speed due to steeper subthreshold swing and higher drive current at low supply voltage, but suffer from larger dynamic energy due to deteriorated overshoot/undershoot characteristic from Miller capacitance. With the reduced Miller capacitance of DOX TFET, the overshoot is significantly reduced (Fig. 5), resulting in further improvement in delay and dynamic energy compared with the nominal TFET devices. The energy-delay product and Standby leakage power are important metrics for high-speed low-power operation. As shown in Fig. 6(b), the DOX TFET device provides substantial advantages in both the energy-delay product and Standby leakage power. Although MOSFET device with assist-circuit using dual supply $(V_{DD}/V_{DL} = 0.2\ V/0.1\ V$ and $V_{DD}/V_{DL} = 0.3\ V/0.2\ V)$, dual V_T technique improves the energy-delay product, the corresponding Standby leakage is one to two orders of magnitude larger compared with the DOX TFET device. Furthermore, the power-gating devices increase the device count and area, and on-chip supply generation circuit (Level Shifter) is needed. For NAND circuits with more number of inputs, the results indicate that the degradation of delay becomes more pronounced for both MOSFET and TFET-based NAND circuits. For the cases with four inputs, MOSFET device with assist-circuit using dual supply $(V_{DD}/V_{DL} = 0.3\ V/0.2\ V)$, dual V_T technique provides best delay performance, and DOX TFET shows better delay performance among the others. Regarding the EDP versus leakage power, MOSFET with dual supply $(V_{DD}/V_{DL} = 0.3\ V/0.2\ V)$, dual V_T assist-circuit with higher number of inputs exhibits best EDP performance but suffer from about two orders larger leakage power compared with the nominal MOSFET and TFET-based NAND circuits. Both the nominal MOSFET-based and DOX TFET-based NAND demonstrates sufficient EDP performance and lower leakage power when considering increased complexity in number of inputs.

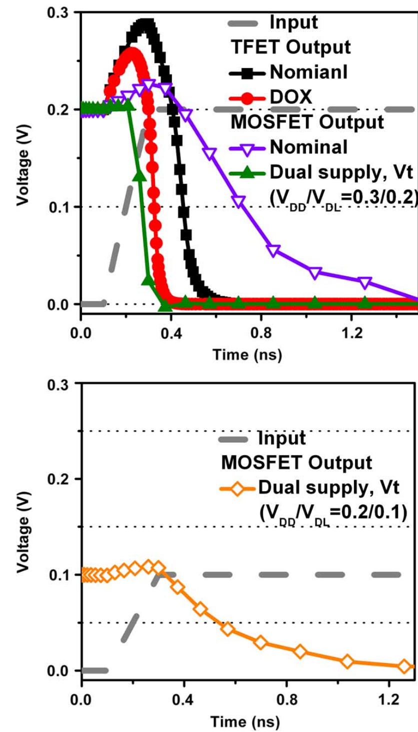


Fig. 5. Waveforms of TFET-based and MOSFET-based two-way NAND circuit.

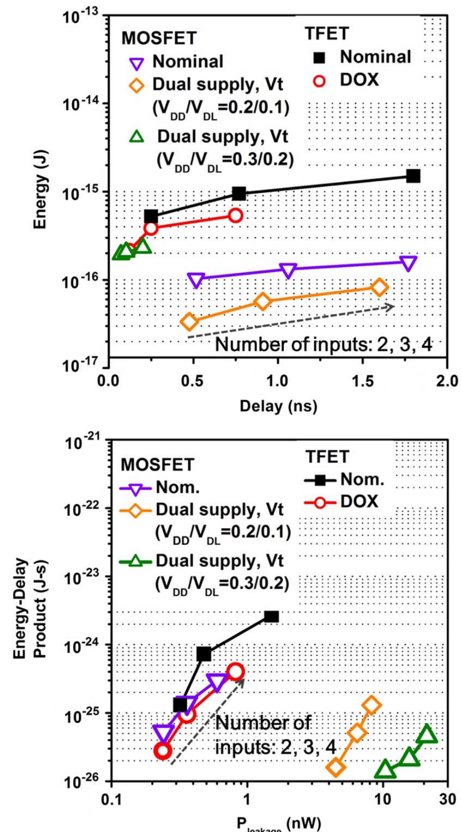


Fig. 6. (a) Dynamic energy versus delay, and (b) Energy-delay product versus Standby leakage power of MOSFET and TFET based NAND circuits with two, three and four inputs.

B. Inverter Chain

Fig. 7(a) shows the schematics of the conventional unloaded three stages inverter chain for nominal MOSFET device,

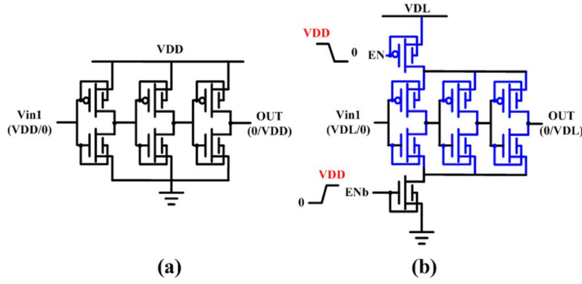


Fig. 7. Schematics of unloaded three stages inverter chain of (a) nominal MOSFET device, nominal TFET device, DOX TFET device, and (b) MOSFET device with assist circuits using V_{TH} power-gating devices.

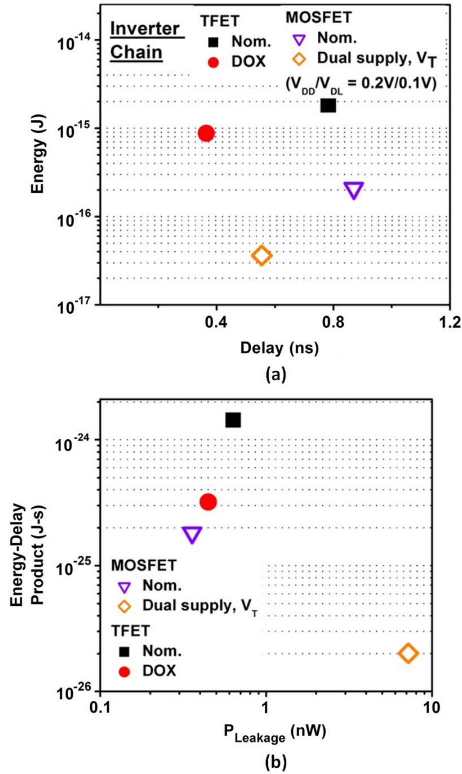


Fig. 8. (a) Dynamic energy versus delay, and (b) energy-delay product versus Standby leakage power of MOSFET and TFET based unloaded three stages inverter chain.

nominal TFET device and DOX TFET device. Fig. 7(b) shows the corresponding schematics for MOSFET devices with dual supply, dual V_T assist-circuit.

Fig. 8(a) and 8(b) show the dynamic energy versus delay and the energy-delay product versus Standby leakage power of TFET-based and MOSFET-based unloaded three stages inverter chain, respectively. Similar to the case for the NAND structure, compared with the nominal MOSFET case, the results indicate that the use of dual supply, dual V_T technique effectively reduces the dynamic energy by approximately 6x, and improves the delay by 36%. The DOX TFET offers the best delay (58% improvement compared with MOSFET with dual supply, dual V_T technique), but suffers from larger dynamic energy due to larger overshoot. MOSFET devices with dual supply, dual V_T assist-circuit exhibit substantial energy-delay product improvement, yet suffer significantly larger Standby leakage power (more than one order of magnitude compared with the nominal MOSFET case).

On the other hand, DOX TFET provides comparable (only slightly larger) energy-delay product and Standby leakage power compared with the nominal MOSFET, while achieving significant (>2x) delay improvement.

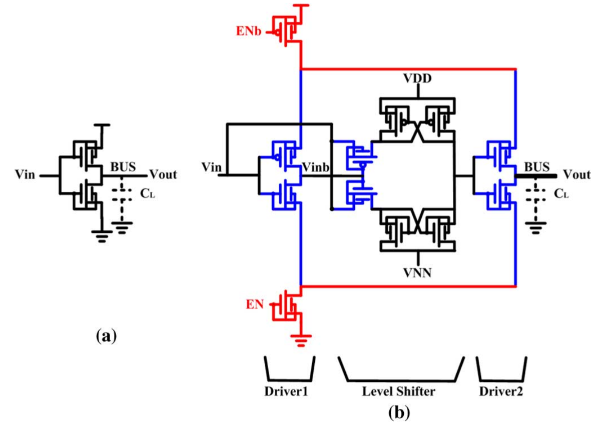


Fig. 9. Schematics of Bus Driver structures of (a) nominal MOSFET device, nominal TFET device, DOX TFET device, and (b) MOSFET device with assist-circuit using dual supply dual V_T technique.

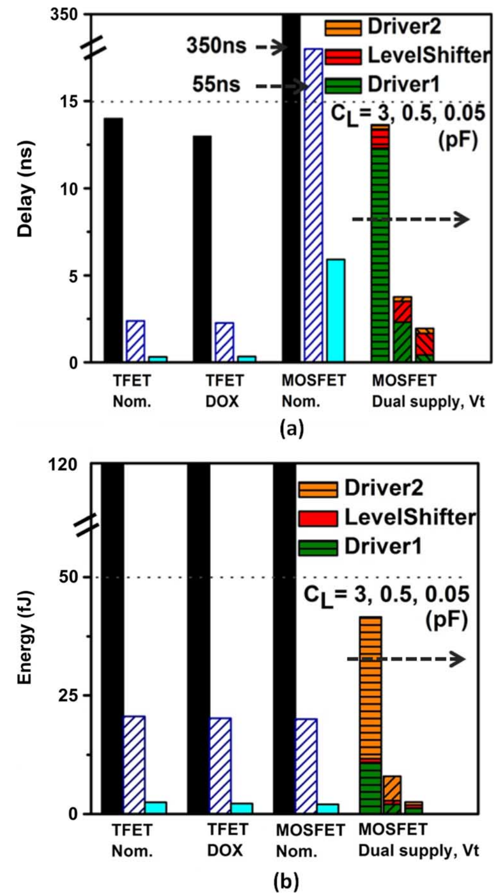


Fig. 10. (a) Delay and (b) dynamic energy of the TFET-based and MOSFET-based bus driver with different bus line loading.

C. Bus Driver

Fig. 9(a) show the schematics of the conventional bus driver for nominal MOSFET device, nominal TFET device, and DOX TFET device, while Fig. 9(b) is the schematics of bus driver using assist-circuit with dual supply, dual V_T MOSFET devices. For MOSFET-based bus driver, in order to drive the heavy load (bus line with capacitance C_L) quickly, the level shifter to generate large swing from V_{NN} to V_{DD} is needed. The relative strength of pass transistors, pull-up transistors, and

pull-down transistors of the level shifter should be carefully designed between the contention devices. Also, Driver1 should be sized up to fast pass the data into the level shifter at the expense of increasing area of assist-circuit and Standby power.

Fig. 10(a) and (b) show the delay and dynamic energy of TFET-based and MOSFET-based bus driver with differnet bus line loading (C_L), respectively. As shown in Fig. 10(a), with $C_L = 3$ pF, compared with the nominal MOSFET-based bus driver, all other three cases can provide near 95% reduction in delay.

However, as C_L becomes smaller, the delay of the MOSFET-based bus driver with dual supply, dual V_T assist-circuit is hindered by the delay of the Level Shifter and the delay is worse than the TFET-based case. Both the nominal TFET-based bus driver and the DOX TFET-based bus driver provide significant delay improvement without the overhead of assist-circuit. For the dynamic energy, the MOSFET-based bus driver with dual supply, dual V_T assist-circuit is superior than the other three cases. As discussed earlier in this section, the MOSFET-based bus driver with dual supply, dual V_T assist-circuit should be carefully designed to ensure that the energy consumption of the high-V_{DD} circuit is negligibly small compared with the driver and the load. Also, the sized-up Driver1 may contribute a significant portion of the total dynamic energy and the dynamic energy becomes comparable with the other three cases when C_L becomes lighter.

Fig. 11 shows the energy-delay product versus delay of the TFET-based and MOSFET-based bus driver with different bus line loading (C_L), respectively. As shown, when the bus line loading is heavy $(C_L = 3$ pF$)$, the MOSFET-based bus driver with dual supply, dual V_T assist-circuit can improve the delay by one order of magnitude and improve the energy-delay product by two orders of magnitude compared with the nominal MOSFET bus driver. As the bus line loading becomes lighter $(C_L = 0.05$ pF$)$, the improvement provided by the dual supply, dual V_T technique decreases, and the delay becomes comparable to the nominal MOSFET bus driver. This is because with light load, the delay is mostly from the level shifter which constrains the improvement of overall bus driver delay as indicated in Fig. 10(a).

On the other hand, as shown in Fig. 11(a), both the nominal TFET-based bus driver and DOX TFET-based bus driver can provide comparable delay and energy-delay product to the MOSFET-based bus driver with dual supply, dual V_T assist-circuit, and even outperform under light bus line loading condition. Fig. 11(b) shows the Standby power and Sleep-mode power of the TFET-based and MOSFET-based bus driver. Here, the Standby power is defined as the power that the bus driver consumes when the dynamic operation is OFF and the power-gating devices are ON. The Sleep-mode power is defined as the power that the bus driver consumes when the dynamic operation and the power-gating devices are both OFF. As shown, the nominal MOSFET-based, nominal TFET-based, and DOX TFET-based bus driver have comparable Standby power and Sleep-mode power, while the MOSFET-based bus driver with dual supply, dual V_T assist-circuit exhibits Standby power three orders of magnitude larger and Sleep-mode power near two orders of magnitude larger. The large Standby power consumption comes mainly from the assist-circuit, namely the level shifter and Driver1. For the Sleep-mode, although the power-gating devices in the OFF-state can reduce the power by 23x compared with the Standby-mode, Driver1 and Driver2 still have larger leakage compared with the other three cases.

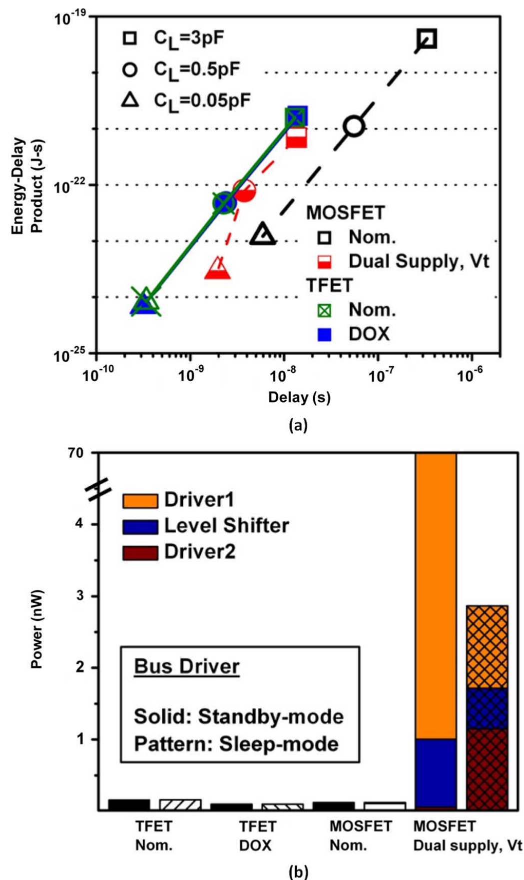


Fig. 11. (a) Energy-delay product versus delay with square symbol indicates $C_L = 3$ pF, circle symbol indicates $C_L = 0.5$ pF, and triangle indicates $C_L = 0.05$ pF. (b) Standby power (indicated by solid bars) and Sleep-mode power (indicated by pattern bars) of the TFET-based and MOSFET-based bus driver with different bus line loading.

D. Latch

Here we consider the Clocked-CMOS Latch instead of the Transmission Gate Latch due to its better stability in low voltage operation [18]. Fig. 12(a) shows the schematics of the Clocked-CMOS Latch circuit for nominal MOSFET, nominal TFET, and DOX TFET, while Fig. 12(b) is the schematics of Latch for MOSFET with dual supply, dual V_T assist-circuit technique. The dynamic energy versus clock-to-Q delay for each case are shown in Fig. 13(a). The energy-delay product versus the power in retention mode are shown in Fig. 13(b). As shown, the DOX TFET-based latch has energy-delay produtct and retention-mode power comparable to the nominal MOSFET-based latch. The MOSFET-based latch with dual supply, dual V_T technique shows better energy-delay product, but suffers from one order of magnitude larger retention-mode power compared with the nominal MOSFET-based latch. Also, the power-gating devices in MOSFET-based latch with dual supply, dual V_T technique should be carefully designed to ensure the data integrity in the retention mode. Table II shows the total fin number used in MOSFET-based and TFET-based Bus Driver and CMOS-Clocked Latch. The large fin number required for the MOSFET-based design with dual-supply dual-V_T assist-circuit can be clearly seen.

IV. Impacts of Temperature and Process Variations

In this section, the impacts of temperature and process variations on TFET-based and MOSFET-based NAND circuits are discussed.

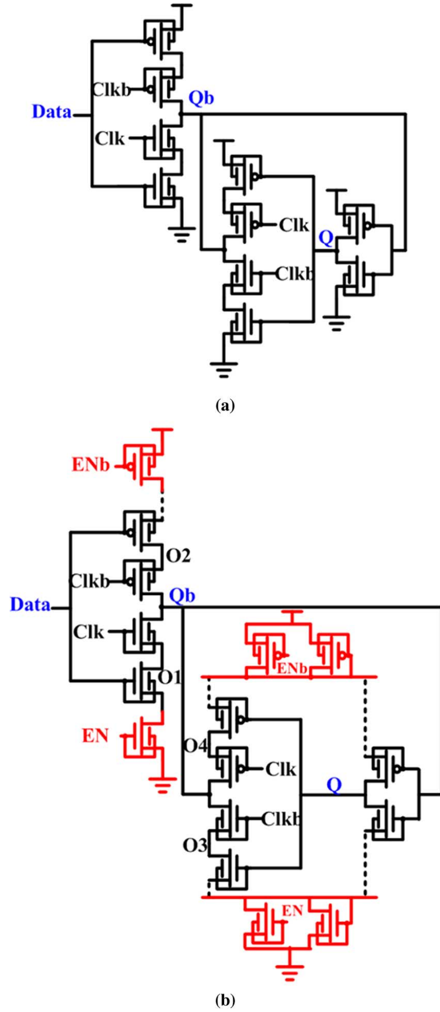
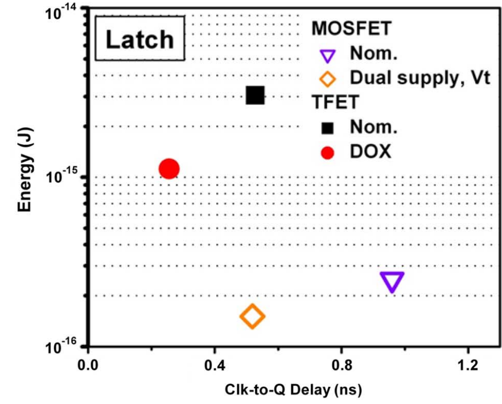


Fig. 12. Schematics of Clocked CMOS Latch of (a) nominal MOSFET device, nominal TFET device, DOX TFET device, and (b) MOSFET device with assist-circuit using dual supply dual V_T technique.



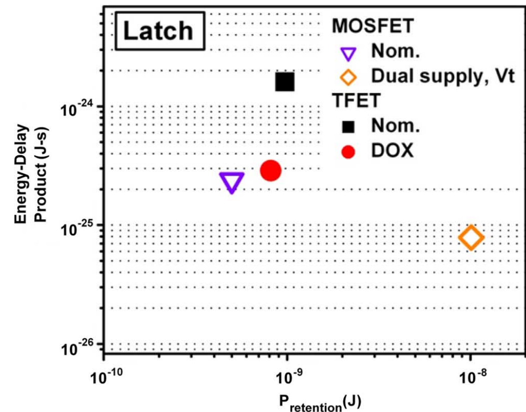


Fig. 13. (a) Dynamic energy versus clock-to-Q delay, and (b) energy-delay product versus the power in retention mode for TFET-based and MOSFET-based Clocked CMOS Latch.

TABLE II
TOTAL FIN NUMBER OF THE TFET-BASED AND MOSFET-BASED BUS DRIVER AND CLOCKED-CMOS LATCH

	Total Fin Number			
	TFET		MOSFET	
Circuit Type	Nominal	DOX	Nominal	Dual Vt, Supply
Bus Driver	6	6	2	190
Latch	30	30	10	220

Several simulation-based and experimental studies have investigated the impact of temperature variations on the Tunneling FET devices and MOSFET devices [19], [20]. These studies indicate that TFET device shows distinct behavior and weak temperature variability compared with MOSFET devices. It is believed that the current of TFET would increase slightly due to the weak temperature dependence of band-gap narrowing as temperature increases. For MOSFET devices, on the other hand, the temperature dependence of the current results from two sources: mobility, and threshold voltage. The ON state current would decrease and shows larger variability with increasing temperature owing to the phonon scattering in the channel. While the threshold voltage would decrease hence the current would increase with increasing temperature. Hence, the TFET-based logic circuits are expected to exhibit less temperature variability compared with the MOSFET-based logic circuits.

For process variations, deviations in device parameters such as L_{eff}, t_{ox} and W_{eff} are considered to assess process-induced variability in TFET-based and MOSFET-based circuits. For each process parameters, devices with $\pm 10\%$ variations from its nominal value are considered at high drain bias condition ($V_{DS} = V_{DD}$; while for dual supply dual V_T MOSFET, $V_{DS} = V_{DL}$), and the parameters whose variation cause the largest deviation of the drain current at device level are chosen and used for the circuit simulations. In our analysis, t_{ox} variation causes the most pronounced variability in drive current for TFET devices while for MOSFET devices, W_{eff} results in the largest current variability.

The simulated energy versus delay of TFET-based and MOSFET-based two-way NAND and three-way NAND circuits considering the process variations are shown in Fig. 14(a) and Fig. 15(a) where the error bar indicates circuit variability caused by the dominant process variation source. The simulated energy-delay product (EDP) versus power of TFET-based and MOSFET-based two-way NAND and three-way NAND circuits considering the process variations are shown in Fig. 14(b) and Fig. 15(b) where the nominal case is indicated by solid

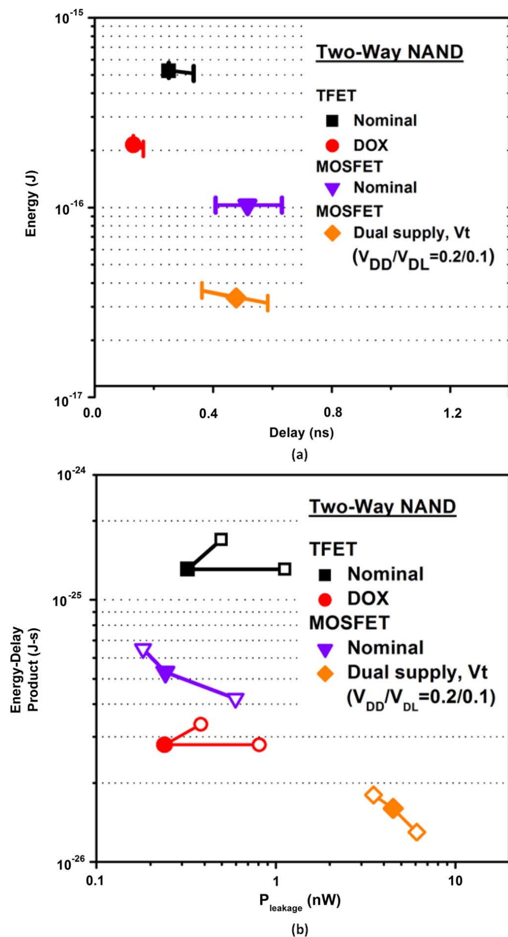


Fig. 14. (a) Dynamic energy versus delay and (b) energy-delay product versus the power of MOSFET and TFET based two-way NAND circuits considering the process variations. The variability caused by the process variations are indicated with error bar in (a) and by hollow symbols in (b).

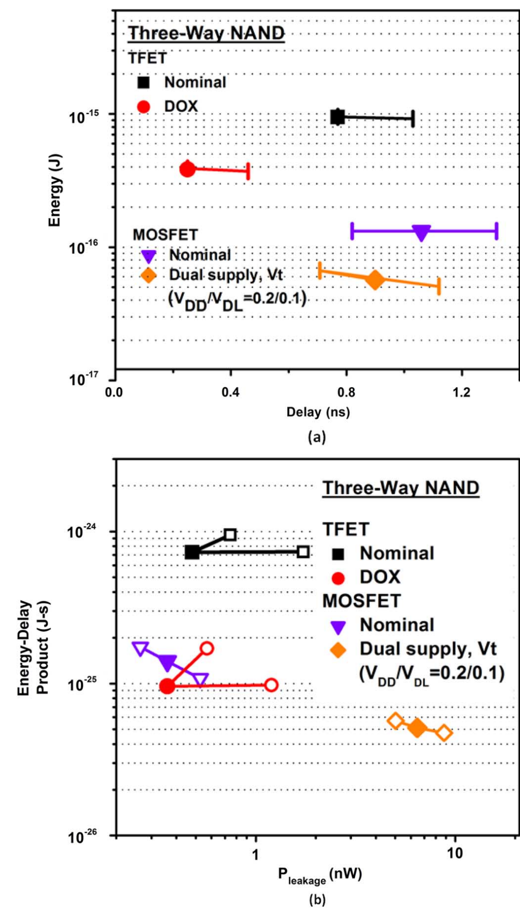


Fig. 15. (a) Dynamic energy versus delay and (b) energy-delay product versus the power of MOSFET and TFET based three-way NAND circuits considering the process variations. The variability caused by the process variations are indicated with error bar in (a) and by hollow symbols in (b).

symbols and the process variation caused variability is indicated by hollow symbols.

In Fig. 14(a), TFET-based two-way NAND circuits show smaller variation in delay compared with the MOSFET-based two-way NAND circuits. Also, the MOSFET circuit with dual supply dual V_T assist-circuit shows the largest variation in dynamic energy. TFET-based two-way NAND circuits show smaller variation in EDP but slightly larger variation in leakage power consumption. For three-way NAND circuits, the four topologies all exhibit larger variability due to larger device counts compared with the two-way NAND circuits. The result shows similar trends as the two-way NAND circuits but with larger variability.

V. Conclusion

We present a comprehensive evaluation of the feasibility of sub-0.2 V high-speed low-power circuits with hetero-channel MOSFET and TFET devices using TCAD mixed-mode simulations. The delay, dynamic energy, and Standby power of the TFET-based and MOSFET-based logic circuits including NAND, Inverter, BUS Driver, and Latch are analyzed and compared. The results indicate that for the logic circuits including the NAND, Inverter chain, and Latch circuits, nominal TFET-based circuits provide significant improvement in delay compared with the nominal MOSFET-based circuits. However, due to the large Miller capacitance in Tunnel FET devices, the dynamic power is larger than the nominal MOSFET-based circuits, hence would have larger EDP (energy-delay product). With the DOX device design, the dynamic energy is greatly improved with the nominal TFET-based circuits. The DOX TFET-based circuits have comparable EDP and Standby power in NAND, inverter chains and Clocked-CMOS Latch compared with the nominal MOSFET-based circuits. While the MOSFET-based circuits using assist-circuits with dual supply, dual V_T technique improve the delay and dynamic energy at the expense of the device count, circuit area, and large leakage power in Standby and Sleep-mode. For the Bus Driver circuits, both the nominal and DOX TFET-based circuits outperform the nominal MOSFET-based circuits in EDP by about two orders of magnitude and consume comparable Standby power. On the other hand, the MOSFET-based circuits using assist-circuits with dual supply, dual V_T technique have comparable EDP at the expense of the complicated sizing in contention devices, device count, circuit area, and large leakage power in Standby mode. The TFET-based circuits with DOX device design provides the potential to achieve high-speed low-power circuit operation at $V_{DD} = 0.2$ V.

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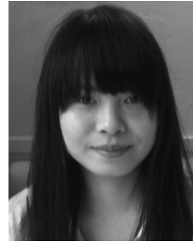

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