A Fully Integrated BIST $\Delta\Sigma$ ADC Using the In-Phase and Quadrature Waves Fitting Procedure

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***Abstract*— This paper demonstrates a fully integrated built-in self-test (BIST) $\Delta\Sigma$ analog-to-digital converter (ADC) based on the proposed in-phase and quadrature waves fitting (IQWF) procedure. The IQWF procedure enables accurately measuring the phases and amplitudes of test responses so as to enhance the test accuracy of the BIST circuitry. The all-digital BIST circuitry, with on-chip stimulus generator and response analyzer, conducts single-tone functional tests to test for the ADCs characterization results such as signal-to-noise-and-distortion ratio (SNDR), dynamic range (DR), frequency response, input-referred offset, and gain error. Since the IQWF procedure is performed successively in real time, the BIST circuitry does not need huge memory to store all the output samples like conventional fast Fourier transform (FFT) analysis does. The overall hardware overhead only consists of 16.6 k digital gates. The fully integrated BIST $\Delta\Sigma$ ADC has been fabricated in 0.18-μm CMOS. Measurement results show that the BIST circuitry reports a peak SNDR of 88.0 dB and a DR of 92.6 dB while the corresponding FFT-based analog tests result in 88.8 and 94.1 dB, respectively. Particularly, the BIST circuitry achieves a test bandwidth as wide as the ADCs 20-kHz rated bandwidth, which is the widest to the best of our knowledge. The proposed BIST ADC can be tested without costly external test resources and is thus well suited for the applications in which conventional test resources are not available such as 3-D ICs.**

***Index Terms*— $\Delta\Sigma$ modulation, ADC test, analog and mixed-signal (AMS) test, analog-to-digital converter (ADC), built-in self-test (BIST), design-for-testability (DfT).**

I. Introduction

$\Delta\Sigma$ MODULATION is a very popular technique for implementing high-resolution analog-to-digital converters (ADCs). With its oversampling and noise-shaping capability, the $\Delta\Sigma$ ADC provides a high signal-to-noise-and-distortion ratio (SNDR) with the robustness against process, voltage, and temperature variations. Conventionally, testing such a high-resolution ADC is very costly and troublesome because it requires high-end analog and mixed-signal (AMS) automatic test equipment (ATE) and a low-noise test environment [1], [2]. However, the required external test resources are not available in various applications. 3-D ICs are examples.

3-D ICs are considered one of the emerging techniques for implementing the next-generation ICs [3] because of increased functional density, decreased power, more compact volume, reduced signal latency, and so on. [4]. However, the 3-D structure also leads to new test challenges [5], [6]. The main issues of testing 3-D ICs are the reduced controllability and observability due to the lack of accessible I/O pads. From this testing point of view, the circuits under test incorporated with some on-chip design-for-testability (DfT) or built-in self-test (BIST) functions are highly demanded.

Many BIST techniques for memory and digital circuits have been proposed and adopted in industry [7]–[9], yet those for ADCs are fewer. Among various BIST designs for ADCs [10]–[14], the functional-test-based BIST approaches are very appealing because they are promising to provide standard ADC characteristics as conventional test methods do. The functional-test-based BIST scheme generally consists of two substantial blocks: an analog stimulus generator (ASG) and an output response analyzer (ORA). The success of a BIST design heavily relies on high test accuracy and a low hardware cost.

Converting a pulse-density-modulated (PDM) bit-stream to an analog stimulus is a cost-effective approach for implementing the highly accurate ASG [15]–[21]. Reference [15] proposed such an ASG that provides high-quality and well-controlled analog stimuli with a small hardware. The ASG is composed of a digital oscillator, a one-bit DAC, and a passive anti-aliasing filter (AAF). The digital oscillator embedded with a digital $\Delta\Sigma$ modulator generates a PDM bit-stream output, which is converted to a continuous-time analog stimulus by the one-bit DAC and the AAF. However, the discrete-time to continuous-time conversion asks for a bulky AAF to provide steep and high stopband attenuation. Implementation with passive components also limits its driving capability. References [18]–[21] used an alternative way to implement the ASG. Although their inputs are also PDM bit-streams, these designs adopted the one-bit digital-to-charge converters (DCCs) to convert the PDM bit-streams into discrete-time analog stimuli instead of continuous-time ones to eliminate the bulky AAF. For example, the experimental results of a second-order $\Delta\Sigma$ modulator in [18] depicted the design-for-digital-testability (DfDT) scheme was able to test for a 84.4-dB dynamic range (DR) at an oversampling ratio (OSR) of 128 while the hardware overhead is negligible.

On the other hand, conventional ORA designs are fast Fourier transform (FFT) or histogram analysis-based [22]–[26]. However, the hardware requirements of both

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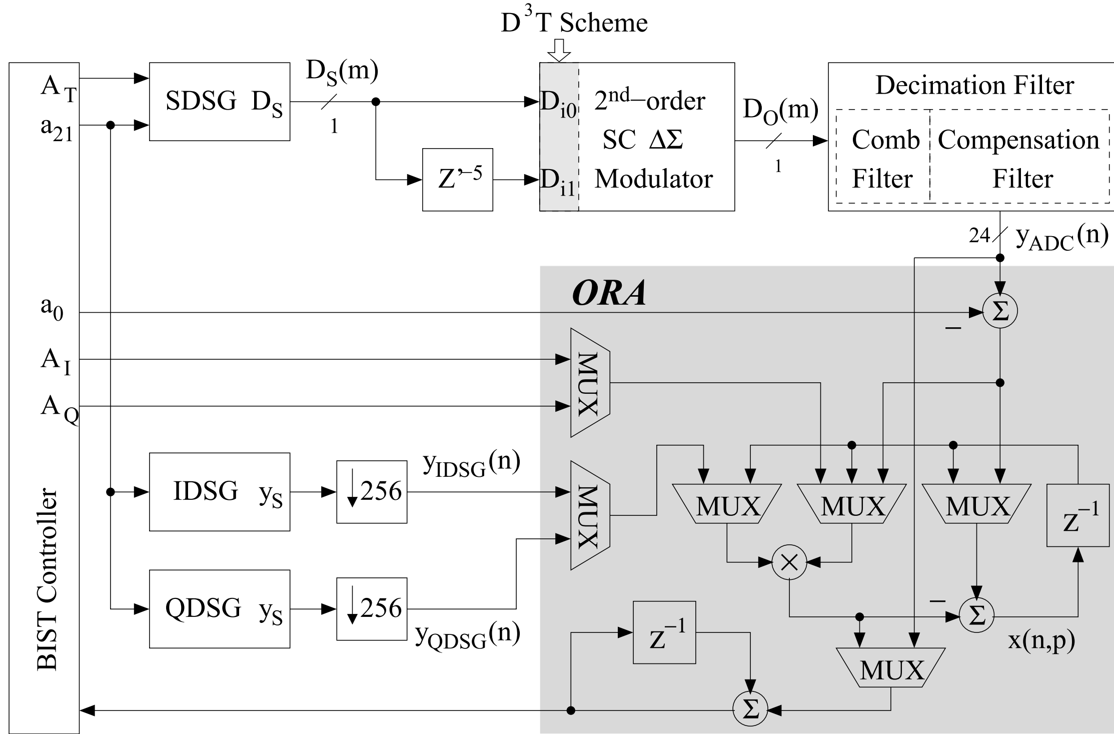

Fig. 1. Block diagram of the proposed BIST ADC.

analysis methods are too high to integrate the whole BIST system on the same chip. It is because the FFT algorithm needs a lot of memory to store all the samples and the histogram analysis method needs a large counter array for analysis. To the best of our knowledge, reference [21] presented the first fully integrated BIST $\Delta\Sigma$ ADC, which is based on the modified controlled sine wave fitting (CSWF) procedure. The DfDT scheme combined with the digital oscillator in [15] implemented the ASG. The modified CSWF procedure processes the ADCs output samples in real time without storing all of them. Therefore, the ORA consists of just 13.3 k gates. Experimental results demonstrated that the BIST design achieved a good test accuracy for low stimulus frequencies, but had larger SNDR errors at higher stimulus frequencies. The reason is that the design assumed the $\Delta\Sigma$ modulator under test (MUT) has a fixed phase shift regardless of the stimulus frequency to simplify the BIST hardware. In practice, the phase shift of $\Delta\Sigma$ modulators varies with the stimulus frequency. The inaccurate phase information at high stimulus frequencies leads to significant SNDR errors and thus limits the BIST bandwidth. For the case in [21], the test bandwidth was 17 kHz out of a 20-kHz rated bandwidth.

This paper proposes a novel in-phase and quadrature waves fitting (IQWF) BIST procedure to address the limited test bandwidth issue in [21]. The IQWF procedure enables accurately measuring the phases and amplitudes of the test responses so as to enhance the test accuracy of the BIST circuitry. Like the conventional FFT-based test method, the IQWF procedure aims at testing for the SNDR, which is the major parameter revealing the performance of an oversampling ADC. The other parameters that can be tested by the IQWF procedure include the DR, frequency response, input-referred offset, and gain error. The main achievement of this paper is achieving a BIST bandwidth as wide as the ADCs rated bandwidth with high test accuracy by the proposed IQWF procedure. Compared with the conventional FFT-based test method requiring lots of memory to store N output samples and a CPU/DSP to conduct the N-point FFT, the IQWF procedure benefits from its real-time low-complexity computation to save the hardware overhead and thus the test cost. The total gate count of the all-digital BIST implementation is only 16.6 k. In addition, a highly accurate ASG is cost-effectively implemented by making the low-cost digital signal generator (DSG) in [17] cooperating with the D^3T input stage in [20]. A test chip containing the fully integrated BIST $\Delta\Sigma$ ADC has been fabricated in 0.18-μm CMOS. Experimental results show that the proposed BIST circuitry successfully achieves a test bandwidth as wide as the ADCs rated bandwidth. In addition, the BIST circuitry reports a peak SNDR of 88.0 dB and a DR of 92.6 dB while the corresponding results of the conventional FFT-based analog tests are 88.8 and 94.1 dB, respectively.

This paper is organized as follows. Section II depicts the circuit design of the $\Delta\Sigma$ ADC under test (AUT). The proposed IQWF procedure and the circuit implementation are illustrated in Section III. Section IV demonstrates the experimental results. Finally, Section V draws our conclusion.

II. Design of the $\Delta\Sigma$ AUT

Fig. 1 shows the block diagram of the $\Delta\Sigma$ AUT. It consists of an analog second-order switched-capacitor (SC) $\Delta\Sigma$ modulator equipped with a decorrelating design-for-digital-testability (D^3T) input stage [20] and a digital decimation filter. The AUT operates at an oversampling frequency f_{OS}

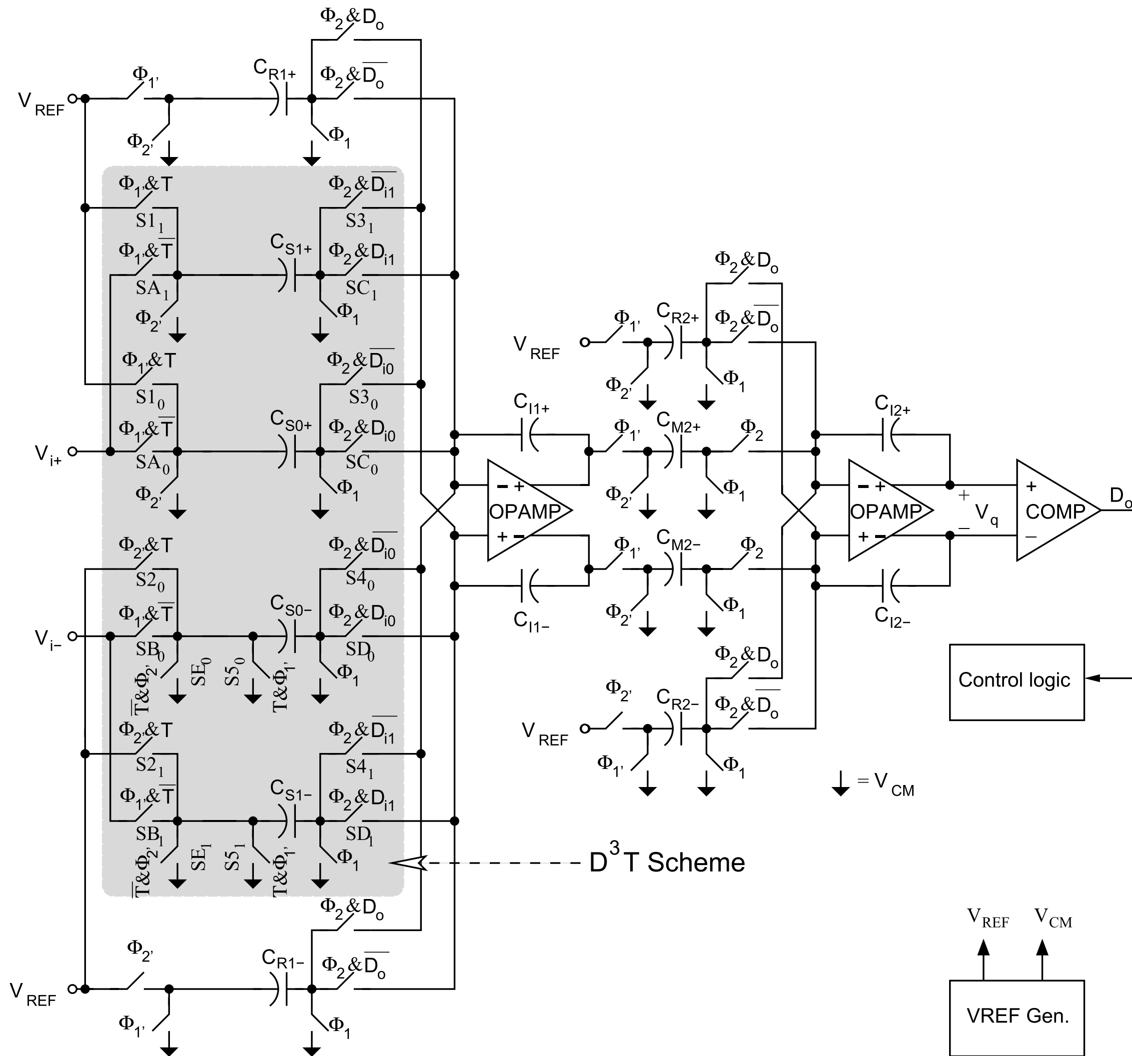

Fig. 2. Schematic of the D[3]T second-order $\Delta\Sigma$ MUT [20].

of 12.288 MHz and an OSR of 256, providing a rated 20-kHz bandwidth for audio applications.

A. D^3T $\Delta\Sigma$ Modulator

To conduct functional tests, an ASG is essential for generating flexible and high-quality stimuli. For the built-in consideration, the area overhead of the ASG must be small enough to be embedded on chip. As has been discussed in Section I, using the PDM bit-streams as the stimuli is an appealing approach to testing $\Delta\Sigma$ ADCs. Therefore, we adopted the D^{3}T scheme in [20], which can precisely convert the PDM bit-streams into the required analog stimuli, to implement the input stage of the $\Delta\Sigma$ MUT. In addition, the D^{3}T scheme is very cost-effective since it only adds a few switches to the original $\Delta\Sigma$ MUT design and reuses most of the original circuits.

Fig. 2 shows the schematic of the D^{3}T $\Delta\Sigma$ MUT. It consists of two cascaded integrators and a comparator as a single-bit quantizer in addition to a built-in reference voltage generator. Φ_1 and Φ_2 are two nonoverlapped clock phases derived from the oversampling clock f_{OS}. The D^{3}T structure, indicated by the shaded area in Fig. 2, provides the $\Delta\Sigma$ MUT with two operation modes including the normal operation mode and the digital test mode. The test-mode control pin T switches the operation mode of the D^{3}T $\Delta\Sigma$ MUT. Setting T to 0 and fixing the stimulus inputs D_{ij}, $j \in \{0, 1\}$, at 1 turn off the switches $S1_j$ to $S5_j$ and make the MUT operate in the normal operation mode. In this mode, the D^{3}T $\Delta\Sigma$ MUT samples the primary analog input V_i and converts it into a PDM output D_O as a conventional second-order $\Delta\Sigma$ modulator does.

The D^{3}T $\Delta\Sigma$ MUT operates in the digital test mode if we set T to 1. The switches SA_j, SB_j, and SE_j are turned off due to the setup. The sampling capacitors C_{S0+}, C_{S0-}, C_{S1+}, and C_{S1-} now sample the dc reference voltage V_{REF} instead of the primary analog input in Φ_1. During the successive Φ_2, the two digital stimuli D_{ij} control the switches $S3_j$, $S4_j$, SC_j, and SD_j, and decide which integration capacitor (either C_{I1+} or C_{I1-}) the sampled charges are transferred to. In other words, the D^{3}T SC input stage behaves as two differential single-bit DCCs to provide the $\Delta\Sigma$ MUT with two inherently linear discrete-time analog stimuli. Hence, the D^{3}T $\Delta\Sigma$ MUT achieves high test accuracy in the digital test mode as well as in the normal mode.

Let $C_{S0} = C_{S1}$ and the two digital stimuli D_{ij} be the same PDM bit-stream D_i but with a relative delay of K oversampling cycles. The I/O relationship of the D^{3}T $\Delta\Sigma$ MUT was shown to be

$$D_O(z) = STF_{\text{MUT}}(z)\left(\frac{1+z^{-K}}{2}\right)D_i(z) + NTF_{\text{MUT}}(z)E_{\text{MUT}}(z) \quad (1)$$

where $D_O(z)$, $STF_{\text{MUT}}(z)$, $NTF_{\text{MUT}}(z)$, and $E_{\text{MUT}}(z)$ are the PDM output, the signal transfer function (STF), the noise transfer function (NTF), and the quantization noise of the $\Delta\Sigma$ MUT, respectively [20]. Equation (1) shows a unique feature of the D^{3}T scheme: it has an additional low-pass filtering (LPF) term $(1 + z^{-K})/2$ associated with $D_i(z)$, which can attenuate the undesired shaped noise of the digital stimulus $D_i(z)$. This LPF capability makes the stimuli generated by the DCCs more similar to their purely analog counterparts used in conventional analog tests. Thus, the D^{3}T scheme effectively improves the test accuracy and alleviates the premature overloading issue when using the PDM bit-streams to test $\Delta\Sigma$ modulators [20].

The operational amplifiers (OPAMPs) used in the MUT are realized with the conventional folded-cascode structure. Simulation results show the OPAMPs nominally have an open-loop gain of 80 dB, a unit-gain bandwidth of 300 MHz, and a phase margin of 63°.

B. Decimation Filter

The $\Delta\Sigma$ AUT also contains a digital decimation filter to remove the out-of-band shaped noise from the MUTs output and to decimate the output to a conversion rate of 48 kHz. Fig. 1 shows the block diagram of the decimation filter. The MUTs output is first filtered by a third-order comb filter and then decimated by a factor of 128. A following finite-impulse-response compensation filter is used to compensate for the amplitude distortion introduced by the comb filter so that the passband ripple of the decimation filter is within ±0.05 dB. Finally, the output of the compensation filter is decimated by a factor of 2 to provide a 48-kHz conversion rate.

III. BIST Design Based on the Proposed IQWF Procedure

The all-digital BIST circuitry conducts single-tone functional tests based on the IQWF procedure and can test for SNDR, DR, frequency response, input-referred offset, and gain error of the AUT. Contrary to the conventional FFT-based analog test methods, the IQWF procedure benefits form its real-time computation and therefore does not need huge memory to save all the analyzed output samples. Hence, the required hardware is small enough to be integrated on chip.

Recall that a single-tone functional test applies a pure sine wave with a stimulus amplitude of A_T and a stimulus frequency of f_T to the AUT. Note that the stimulus frequency f_T must be carefully chosen to fulfill the coherent sampling criterion [27]. The resulted output of the AUT can be expressed as

$$y_{\text{ADC}}(n) = a_0 + \underbrace{a_1 \sin\left(2\pi\frac{f_T}{f_S}n + \phi_1\right)}_{y_{\text{tone}}(n)} + \underbrace{\sum_{k=2}^{\infty} a_k \sin\left(2\pi\frac{kf_T}{f_S}n + \phi_k\right) + e(n)}_{\text{thdn}(n)} \quad (2)$$

where a_0, $y_{\text{tone}}(n)$, and $\text{thdn}(n)$ are the offset, the stimulus-tone response, and the total-harmonic-distortion-plus-noise (THD + N) signal of the AUTs output $y_{\text{ADC}}(n)$, respectively. The term $\text{thdn}(n)$ includes the harmonic distortion induced by the nonlinearity of the AUT and an additive noise $e(n)$. $e(n)$ represents the total noise at the AUTs output, which comprises the quantization noise of the AUT, the jitter noise introduced by the sampling clock source, the thermal and flicker noise of the circuits, and so on. f_S is the conversion rate of the AUTs decimated output, i.e., $f_S = f_{\text{OS}}/\text{OSR}$.

If we can generate a digital fitted sine wave, $y_{\text{fit}}(n)$ that best fits the stimulus-tone response, i.e., $y_{\text{tone}}(n) \cong y_{\text{fit}}(n)$ for all n, and also test for the constant offset a_0, the digital THD + N signal can be derived according to

$$\text{thdn}(n) \cong y_{\text{ADC}}(n) - a_0 - y_{\text{fit}}(n) \quad (3)$$

which is then used to compute the THD + N power of the test. Meanwhile, the estimated amplitude a_1 of the stimulus-tone response can be used to compute the signal power and the gain error of the test. The ratio of the signal power and the THD + N power reveals the SNDR value of the test.

To generate the digital fitted sine wave that best fits the stimulus-tone response, it is necessary to accurately acquire the amplitude, frequency, and phase shift of the stimulus-tone response. Since the stimulus frequency f_T is a controlled factor, the amplitude a_1 and the phase shift ϕ_1 are what we need to test for. Reference [21] already showed how to accurately test for the amplitude a_1 on chip, yet conventional methods of testing for and generating the phase shift ϕ_1 are too complicated for BIST implementation.

The IQWF procedure simplifies the estimation and compensation of the AUTs phase response as follows. Let us first decompose the fitted sine wave into two orthogonal parts

$$y_{\text{fit}}(n) = A_I \sin\left(2\pi\frac{f_T}{f_S}n\right) + A_Q \cos\left(2\pi\frac{f_T}{f_S}n\right) \quad (4)$$

where

$$A_I \equiv a_1 \cos\phi_1 \quad (5)$$

$$A_Q \equiv a_1 \sin\phi_1. \quad (6)$$

The former term $A_I \sin(2\pi f_T/f_S n)$ is referred to the in-phase component, which has the same phase as that of the stimulus, and the latter term $A_Q \cos(2\pi f_T/f_S n)$ is referred to the quadrature component, which is always $\pi/2$ out of phase of the stimulus. The amplitude of the stimulus-tone response can be calculated by

$$a_1 = \sqrt{A_I^2 + A_Q^2}. \quad (7)$$

Equation (4) indicates that we can accurately synthesize $y_{\text{fit}}(n)$ by measuring the two amplitudes A_I and A_Q instead of directly measuring the phase shift ϕ_1. The latter case is much more difficult. Once the amplitudes A_I and A_Q are tested for and the two IQ reference signals $\sin(2\pi f_T/f_S n)$ and $\cos(2\pi f_T/f_S n)$ are available, the fitted sine wave is certainly attainable.

Due to the coherent and zero-mean properties of thdn(n), the least-squares (LS) estimation described in IEEE Standard 1241 [28] well suits for deriving the coefficients a_0, A_I, and A_Q in our applications [29]–[31]. Assume N samples $y_{\text{ADC}}(1), \ldots, y_{\text{ADC}}(N)$ are taken in the estimation. The LS estimation tends to find the values of a_0, A_I, and A_Q that minimize the following sum:

$$\sum_{n=1}^{N}\left[y_{\text{ADC}}(n)-a_0-A_I\sin\left(2\pi\frac{f_T}{f_S}n\right)-A_Q\cos\left(2\pi\frac{f_T}{f_S}n\right)\right]^2.$$

The LS solution is given by [28]

$$\beta=(X^TX)^{-1}X^Ty_{\text{ADC}} \tag{8}$$

where $\beta=[a_0\ A_I\ A_Q]^T$, $y_{\text{ADC}}=[y_{\text{ADC}}(1),\ \ldots,\ y_{\text{ADC}}(N)]^T$, and

$$X=\begin{bmatrix}1 & \sin\left(2\pi\frac{f_T}{f_S}\cdot 1\right) & \cos\left(2\pi\frac{f_T}{f_S}\cdot 1\right)\\ 1 & \sin\left(2\pi\frac{f_T}{f_S}\cdot 2\right) & \cos\left(2\pi\frac{f_T}{f_S}\cdot 2\right)\\ \vdots & \vdots & \vdots\\ 1 & \sin\left(2\pi\frac{f_T}{f_S}\cdot N\right) & \cos\left(2\pi\frac{f_T}{f_S}\cdot N\right)\end{bmatrix}.$$

Again, due to the coherent property, the computation of (8) can be simplified as

$$X^TX=\text{diag}(N,\ N/2,\ N/2) \tag{9}$$

and

$$X^Ty_{\text{ADC}}=\begin{bmatrix}\sum_{n=1}^{N}y_{\text{ADC}}(n)\\ \sum_{n=1}^{N}\sin\left(2\pi\frac{f_T}{f_S}n\right)\cdot y_{\text{ADC}}(n)\\ \sum_{n=1}^{N}\cos\left(2\pi\frac{f_T}{f_S}n\right)\cdot y_{\text{ADC}}(n)\end{bmatrix}. \tag{10}$$

From (8)–(10), we have

$$\begin{bmatrix}a_0\\ A_I\\ A_Q\end{bmatrix}=\begin{bmatrix}\frac{1}{N}\sum_{n=1}^{N}y_{\text{ADC}}(n)\\ \frac{2}{N}\sum_{n=1}^{N}\sin\left(2\pi\frac{f_T}{f_S}n\right)\cdot y_{\text{ADC}}(n)\\ \frac{2}{N}\sum_{n=1}^{N}\cos\left(2\pi\frac{f_T}{f_S}n\right)\cdot y_{\text{ADC}}(n)\end{bmatrix}. \tag{11}$$

Given the test response $y_{\text{ADC}}(n)$ and the two digital IQ reference signals $\sin(2\pi f_T/f_S n)$ and $\cos(2\pi f_T/f_S n)$, the values of a_0, A_I, A_Q can be estimated according to (11). Once the amplitudes A_I and A_Q are acquired, the digital fitted sine wave $y_{\text{fit}}(n)$ is generated according to (4).

Fig. 1 shows the detailed design of the fully integrated BIST ADC. The all-digital BIST circuitry comprises three main blocks: the DSGs, the ORA, and the BIST controller. The stimulus DSG (SDSG) generates the PDM bit-stream $D_S(m)$ to stimulate the D^{3}T $\Delta\Sigma$ AUT in the digital test mode where the notation m is the index of the signals operating at the oversampling frequency f_{OS}. The in-phase DSG (IDSG) and the quadrature DSG (QDSG) provide the aforementioned IQ reference signals in (4) with a normalized amplitude of 0.5 to simplify the hardware implementation, i.e., $y_{\text{IDSG}}(n)=0.5\sin(2\pi f_T/f_S n)$ and $y_{\text{QDSG}}(n)=0.5\cos(2\pi f_T/f_S n)$.

A. Proposed IQWF Procedure

The IQWF procedure contains four steps to complete a test. Every step conducts the same coherent test and acquires N decimated output samples for analysis. In our design, N is set to be 2^{11}, a power of 2, to eliminate the need of a divider. The following detail the IQWF procedure and the BIST functions performed in the successive steps.

1) Calculating the Offset a_0: At the beginning of the BIST, the setup parameters A_T and a_{21} are loaded into the DSGs to specify the amplitude A_T and the frequency f_T of the stimulus, respectively. Then, the SDSG generates the PDM bit-stream $D_S(m)$ to stimulate the D^{3}T AUT. Then, the ORA accepts N decimated outputs from the AUT and calculates the offset a_0 in real time according to (11). The offset-free response is defined as

$$\widetilde{y}_{\text{ADC}}(n)\equiv y_{\text{ADC}}(n)-a_0. \tag{12}$$

2) Calculating the Amplitude of the In-Phase Component A_I: In the second step, the IDSG generates the in-phase reference signal $y_{\text{IDSG}}(n)=0.5\sin(2\pi f_T/f_S n)$. According to (11), the ORA performs the following equation to calculate A_I:

$$A_I=\frac{4}{N}\sum_{n=1}^{N}y_{\text{IDSG}}(n)\cdot\widetilde{y}_{\text{ADC}}(n). \tag{13}$$

Note that the offset-free response $\widetilde{y}_{\text{ADC}}(n)$ is used in (13) instead of $y_{\text{ADC}}(n)$ to increase the computational DR of the ORA design. Equations (11) and (13) have the same results because the coherent property makes $\sum_{n=1}^{N}y_{\text{IDSG}}(n)\cdot a_0=0$.

3) Calculating the Amplitude of the Quadrature Component A_Q: Similar to the previous step, the ORA now accepts the quadrature reference signal generated by the QDSG, $y_{\text{QDSG}}(n)=0.5\cos(2\pi f_T/f_S n)$, and conducts the following:

$$A_Q=\frac{4}{N}\sum_{n=1}^{N}y_{\text{QDSG}}(n)\cdot\widetilde{y}_{\text{ADC}}(n). \tag{14}$$

4) Calculating the THD + N Power: The last step aims at calculating the THD + N power. The BIST circuitry first uses the computed A_I and A_Q to derive the THD + N signal according to

$$\begin{aligned}\text{thdn}(n)=\ &\widetilde{y}_{\text{ADC}}(n)-2A_Iy_{\text{IDSG}}(n)\\ &-2A_Qy_{\text{QDSG}}(n).\end{aligned} \tag{15}$$

After that, the ORA accepts the resulted THD + N signal and calculates the THD + N power of the test by

$$P_{\text{THDN}}=\frac{1}{N}\sum_{n=1}^{N}\text{thdn}(n)^2. \tag{16}$$

Finally, the SNDR of the test can be calculated by

$$\text{SNDR}=\frac{A_I^2+A_Q^2}{2P_{\text{THDN}}}. \tag{17}$$

TABLE I
SUMMARY OF THE IQWF BIST FUNCTIONS OF THE ORA

	BIST function
Step 1	$a_0 = \frac{1}{N}\sum_{n=1}^{N} y_{ADC}(n)$
Step 2	$A_I = \frac{4}{N}\sum_{n=1}^{N} y_{IDSG}(n) \cdot \widetilde{y}_{ADC}(n)$
Step 3	$A_Q = \frac{4}{N}\sum_{n=1}^{N} y_{QDSG}(n) \cdot \widetilde{y}_{ADC}(n)$
Step 4	$P_{THDN} = \frac{1}{N}\sum_{n=1}^{N}\{\widetilde{y}_{ADC}(n) - 2A_I y_{IDSG}(n) -2A_Q y_{DBSG}(n)\}^2$
Result	$SNDR = \frac{A_I^2+A_Q^2}{2P_{THDN}}$

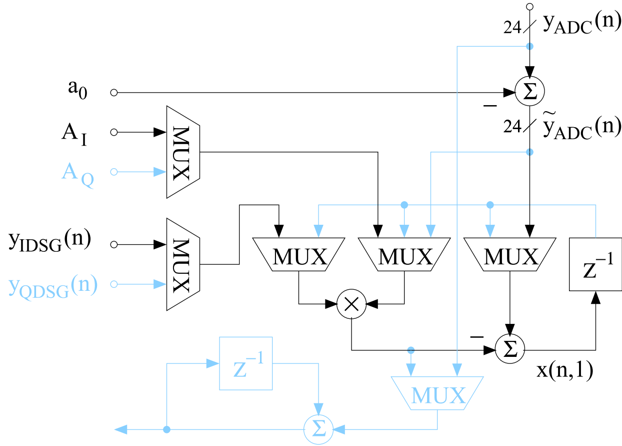

Fig. 3. Configuration of the ORA in substep 1.

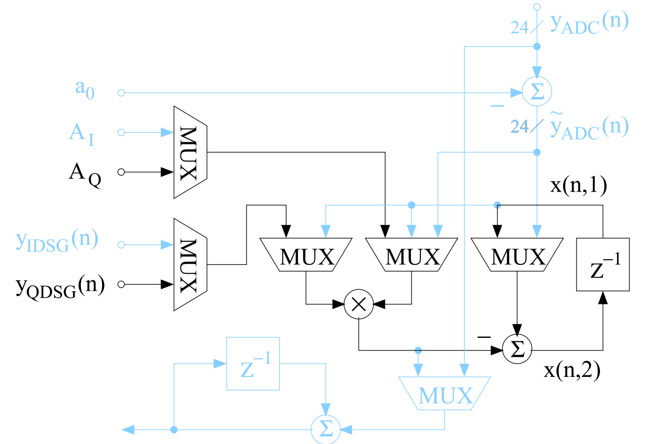

Fig. 4. Configuration of the ORA in substep 2.

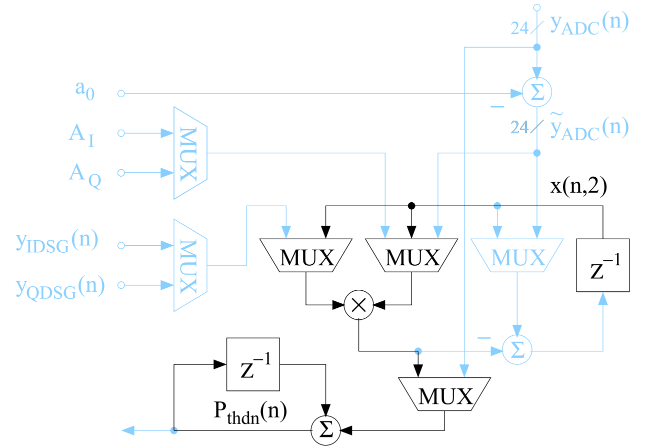

Fig. 5. Configuration of the ORA in substep 3.

B. Implementation of the BIST Circuitry

The BIST circuitry benefits from its all-digital implementation so that it is synthesizable, scalable, testable, and robust. Since the real-time IQWF procedure does not need huge memory, the BIST hardware is small enough for on-chip integration.

1) Implementation of the ORA: Table I lists the IQWF BIST functions of the ORA in every BIST step. The function in the first step performs accumulation while the other functions perform both multiplications and accumulation. Since the BIST functions are executed sequentially, the four BIST steps are designed to share the same multiplier and accumulator with the help of the multiplexers to save the hardware cost. By taking advantage of the ΔΣ ADCs oversampling feature, a radix-2 Booth multiplier instead of a parallel multiplier is used to perform the signed multiplication. In addition, the computation of every decimated output in the last BIST step is further divided into three serial substeps to avoid adopting additional multipliers. The design sets $N = 2^{11}$ to eliminate the need of a divider. With all the efforts, the ORA design consists of only 2.5 k digital gates. Figs. 3–5 show the configurations of the ORA in the corresponding substeps. The temporary results of the first two substeps are stored in the register $x(n, p)$, where $p \in \{1, 2\}$. For the nth decimated output of the AUT, $1 \leqslant n \leqslant N$, the ORA processes it as follows.

a) Substep 1 (Removing the in-phase component of the fitted sine wave): With the configuration shown in Fig. 3, the ORA first computes

$$x(n,1) = \widetilde{y}_{\text{ADC}}(n) - 2A_I y_{\text{IDSG}}(n) = \widetilde{y}_{\text{ADC}}(n) - A_I \sin\left(2\pi \frac{f_T}{f_s} n\right). \tag{18}$$

The Booth multiplier in this substep takes 24 oversampling cycles to complete the 24-bit by 24-bit multiplication.

b) Substep 2 (Removing the quadrature component of the fitted sine wave): Fig. 4 shows the configuration of the ORA in this substep. The ORA computes

$$\begin{aligned} x(n,2) &= x(n,1) - 2A_Q y_{\text{QDSG}}(n) \\ &= \widetilde{y}_{\text{ADC}}(n) - A_I \sin\left(2\pi \frac{f_T}{f_s} n\right) - A_Q \cos\left(2\pi \frac{f_T}{f_s} n\right) \\ &= \widetilde{y}_{\text{ADC}}(n) - y_{\text{fit}}(n) \\ &\cong \text{thdn}(n). \end{aligned} \tag{19}$$

So far, the offset and the fitted sine wave are both eliminated from the AUTs nth output, resulting in the nth THD + N signal sample. Similarly, this substep takes another 24 oversampling cycles to complete the Booth multiplication.

c) Substep 3 (Accumulating the square of the current THD + N signal): As the signal flow shown in Fig. 5, the ORA

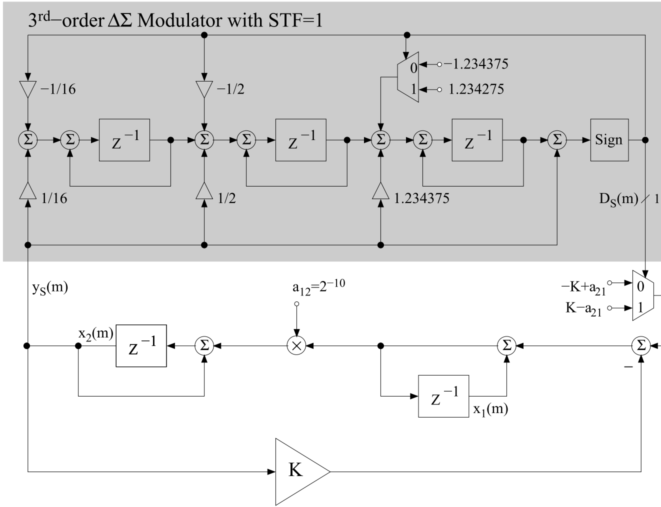

Fig. 6. Implementation of the DSG.

first calculates the square of the nth THD + N signal resulted from the prior substep. Then, the ORA accumulates the square and results in

$$P_{\text{thdn}}(n) = P_{\text{thdn}}(n-1) + x(n,2)^2 = \sum_{i=1}^{n} \text{thdn}(i)^2. \quad (20)$$

This substep also requires 24 oversampling cycles for the Booth multiplication.

The above three substeps are repeated for every decimated output until $n = N$. Finally, the output of the ORA is

$$\frac{1}{N} P_{\text{thdn}}(N) = \frac{1}{N} \sum_{i=1}^{N} \text{thdn}(i)^2 = P_{\text{THDN}} \quad (21)$$

which is the THD + N power of the test. For each decimated period of the $\Delta\Sigma$ AUT, the three substeps totally take only 72 out of 256 oversampling cycles.

2) Implementation of the DSG: As shown in Fig. 1, the IQWF procedure requires three DSGs to provide the PDM bit-stream and the digital IQ reference signals. As the stimulus, the in-band SNDR of $D_S(m)$ is suggested to be at least 12 dB higher than that of the AUTs response to ensure the test accuracy [32]. Regarding the linearity of the stimuli, the discrete-time analog stimuli converted from $D_S(m)$ are inherently linear thanks to that the D^{3}T scheme only adopts single-bit DCCs. In addition, the SNDRs of $y_{\text{IDSG}}(n)$ and $y_{\text{QDSG}}(n)$ are suggested to be at least 6 dB higher than that of the AUTs response to ensure the computational accuracy according to (15).

We modified the digital oscillator in [17] to implement the three DSGs. Fig. 6 shows the DSG design, which is a digital resonator embedded with a digital $\Delta\Sigma$ modulator with a unity-gain STF. The DSG operates at the oversampling frequency and simultaneously generates the multibit sine wave $y_s(m)$ and the PDM bit-stream $D_S(m)$. The required reference signal is obtained by directly decimating $y_s(m)$ by a factor of OSR.

To stimulate the second-order analog MUT, we embedded a third-order digital $\Delta\Sigma$ modulator in the DSG for its better noise-shaping capability. Thus, the DSG can provide the PDM bit-streams with high in-band SNDRs. However, the embedded digital $\Delta\Sigma$ modulator introduces an extra shaped quantization noise into the oscillation loop and thus may disturb the stability of the DSGs oscillation, especially when the amplitude and/or the frequency of the output signal is high.

An effective approach to keeping the oscillation stable and enhancing the quality of the stimuli is to add another feedback path with a gain K, as shown in Fig. 6 [17]. The characteristic equation of the DSG was shown to be

$$z^{-2} + (a_{12}a_{21} - 2)z^{-1} + 1 + \frac{(a_{12}a_{21} - K)z^{-1}\text{NTF}_{\text{DSG}}(z)E_{\text{DSG}}(z)}{X_2(z)} = 0 \quad (22)$$

where $\text{NTF}_{\text{DSG}}(z)$ and $E_{\text{DSG}}(z)$ are the NTF and the quantization noise of the embedded digital $\Delta\Sigma$ modulator, respectively. $X_2(z)$ is the z-transform of $x_2(m)$. The DSG stably oscillates if (22) has solutions exactly on the z-domain unit circle. Thus, the term containing the shaped noise $\text{NTF}_{\text{DSG}}(z)E_{\text{DSG}}(z)$ in (22) needs to be eliminated. Setting $K = a_{12}a_{21}$ makes this term approximate to zero as desired. Note that the gain K is realized by shifting and adding so that the DSG is multiplier-free. The implementation results show the SDSG has a gate count of 4.6 k while the IDSG and the QDSG both consist of 3.8 k gates after properly truncating the signals. The three DSGs have different sizes because they are used to generate different signals. The SDSG is demanded to supply the high-quality stimuli even with an amplitude as small as −60 dBFS for the dynamic tests. On the other hand, the amplitude of the IQ reference signals provided by the other two DSGs are fixed at 0.5. Hence, the implementation of the SDSG needs to be more precise.

Once the shaped noise related term in (22) is vanished, the oscillation frequency is solely determined by the product of a_{12} and a_{21}. We fixed a_{12} at 2^{-10} so that the stimulus frequency can be set by a_{21} alone to simplify the test setup. In addition, the amplitude and the phase of the output signal are well controlled by the initial values of the two integrators $x_1(0)$ and $x_2(0)$ [17]. To sum up, the design not only is cost-effective, but also provides the flexibility of conducting accurate tests with various amplitudes and frequencies.

With slight modifications, the proposed IQWF-based ORA can be applied to arbitrary ADCs with the same computational accuracy. However, the method of using the PDM bit-streams as stimuli is only suitable for $\Delta\Sigma$ ADCs. To make the proposed BIST design applicable to arbitrary ADCs, an on-chip ASG, instead of the cost-effective combination of the SDSG and the simple D^{3}T scheme, is necessary.

IV. Experimental Results

The fully integrated BIST $\Delta\Sigma$ ADC has been fabricated in a 0.18-μm CMOS process. Fig. 7 shows the micrograph of the test chip. The active area of the $\Delta\Sigma$ ADC including the analog D^{3}T $\Delta\Sigma$ MUT and the digital decimation filter is 0.49 mm^2. On the other hand, the all-digital BIST circuitry consists of 16.6 k gates and occupies 0.20 mm^2. The hardware overhead of the BIST circuitry is about 29.0%. When the design is

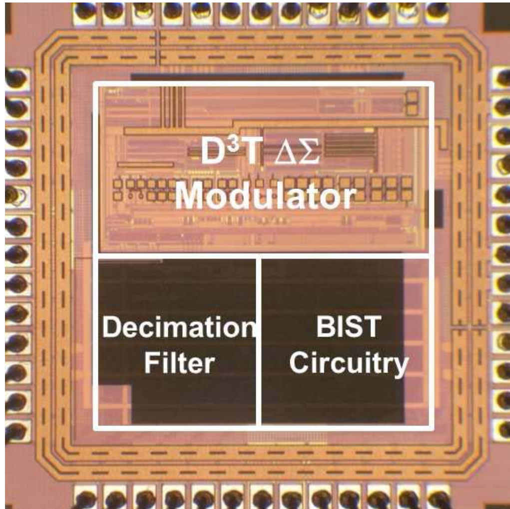

Fig. 7. Micrograph of the test chip.

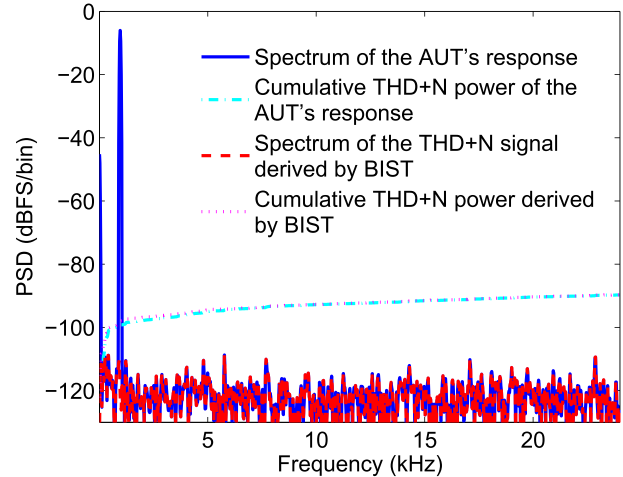

Fig. 8. Measured spectra of the AUTs output and the corresponding THD + N signal derived by the BIST circuitry in the 1 kHz, −6-dBFS test.

TABLE II
SUMMARY OF THE TEST CHIP

Process	0.18-μm CMOS	
Test chip area	1.33 by 1.33 mm^2	
Block	Gate counts	Area
D^{3}T ΔΣ MUT	N/A	0.35 mm^2
Decimation filter	11.2k gates	0.14 mm^2
Total ΔΣ ADC	N/A	0.49 mm^2
SDSG	4.6k gates	0.14 mm^2
IDSG & QDSG	3.8k ×2 gates	
ORA	2.5k gates	0.03 mm^2
BIST controller & I2S interface	2.2k gates	0.03 mm^2
Total BIST circuitry	16.6k gates	0.20 mm^2

ported to advanced technology, the area of the analog core is scaled down less while the digital core has the same gate count and its area is scaled down more significantly. Thus, the BIST area overhead becomes smaller in advanced technology. Table II summarizes the test chip design.

A. Test Setup

For each BIST, the setup parameters are loaded to specify the amplitude and frequency of the single-tone test. As soon as the BIST procedure is completed, the BIST circuitry outputs the test results. Note that the BIST design achieves an all-digital I/O interface during the BIST. If users prefer to control the BIST and observe the detailed results externally, the only test resource required is a low-cost digital tester, which can be realized by a low-end FPGA. For production tests, the BIST design outputs as simple as a go/no-go signal by storing all the BIST setup parameters including the threshold values for pass/fail decisions in on-chip memory. In both the cases, the proposed BIST ADC eliminates the need of high-end AMS ATE of conventional analog tests. Hence, the proposed design not only significantly reduces the test cost but also addresses the test issue of lacking accessible I/O pads in 3-D ICs.

In addition to the BIST, we also conducted the corresponding FFT-based analog tests in the conventional way as references. The analog stimuli are generated by the audio precision system II while the AUTs outputs are captured by a logic analyzer. The acquired output samples are then analyzed by FFT to compute the SNDR result of the test.

B. Validation of the IQWF Procedure

The similarity between the spectrum of the AUTs output and that of the derived THD + N signal in the last BIST step validates the IQWF procedure. The BIST design contains an additional I2S interface to simultaneously acquire the AUTs output and the corresponding THD + N signal. Fig. 8 plots the measured spectra of these two signals of the 1-Hz, −6-dBFS test. The offset and the stimulus-tone response are successfully eliminated to be beneath the noise floor in both spectra. Meanwhile, the THD + N floors of the two spectra are almost the same. Thus, the cumulative THD + N power plots of the two test results highly overlap with each other. The observations indicate that the amplitude, frequency, and phase shift of the fitted sine wave accurately match those of the stimulus-tone response, respectively, as our expectation. In the meantime, the BIST circuitry reports an offset of −49.5 dBFS in this test.

C. SNDR Versus Stimulus Level Test Results

Fig. 9 shows the test results of SNDR versus stimulus level. The stimulus amplitude was swept from −60 to −3 dBFS with a 2-dBFS step till −10 dBFS, and a narrower 1-dBFS step thereafter. In the meantime, the stimulus frequency was kept at 0.96 kHz. The BIST circuitry reports a peak SNDR of 88.0 dB and a DR of 92.6 dB, while the conventional FFT-based analog tests result in 88.8 and 94.1 dB, respectively. The peak SNDR of the BIST results occurs at a stimulus level of −3 dBFS, very close to the full scale of the AUT.

Fig. 10 further shows the SNDR differences between the FFT-based analog test results and their BIST counterparts. For various stimulus levels, the SNDR differences are within 1.5 dB. The SNDR results of the BIST are slightly lower than their counterparts of the FFT-based analog tests because using

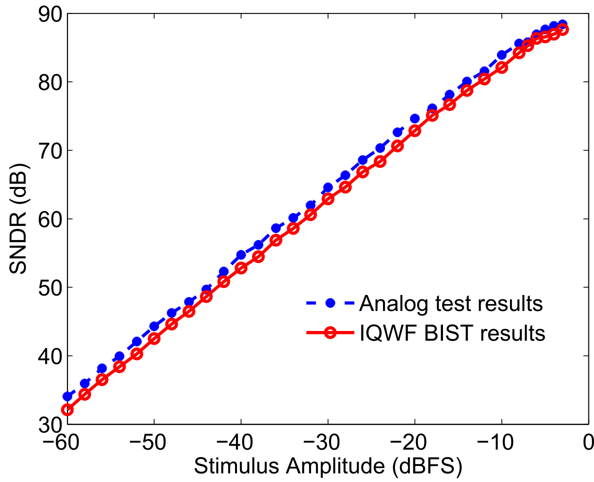

Fig. 9. Test results of SNDR versus stimulus level.

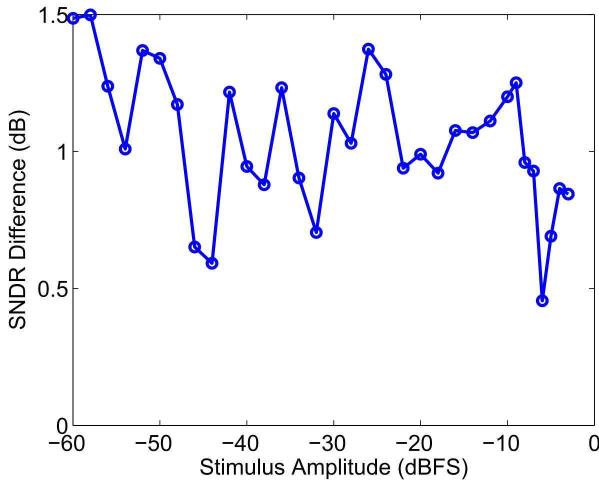

Fig. 10. SNDR differences of the SNDR versus stimulus level test.

TABLE III
SUMMARY OF THE DR TESTS

	Proposed BIST	Analog test
Stimulus type	PDM bit-stream	Analog stimulus
Analysis method	IQWF procedure	FFT analysis
DR	92.6 dB	94.1 dB
Peak SNDR	88.0 dB	88.8 dB

the PDM bit-streams as stimuli induces additional correlated shaped noise, which slightly increases the THD + N power of the test [20]. Table III summarizes the tests. Compared with the conventional FFT-based analog tests, the proposed BIST achieves a good test accuracy and a lower test cost with less setup efforts.

D. SNDR Versus Stimulus Frequency Test Results

Fig. 11 shows the SNDR test results versus stimulus frequency with the same stimulus amplitude of −6 dBFS. The BIST circuitry successfully achieves a test bandwidth as wide as the AUTs 20-kHz rated bandwidth. The SNDR differences between the FFT-based analog test results and their BIST counterparts are shown in Fig. 12 and within 0.6 dB.

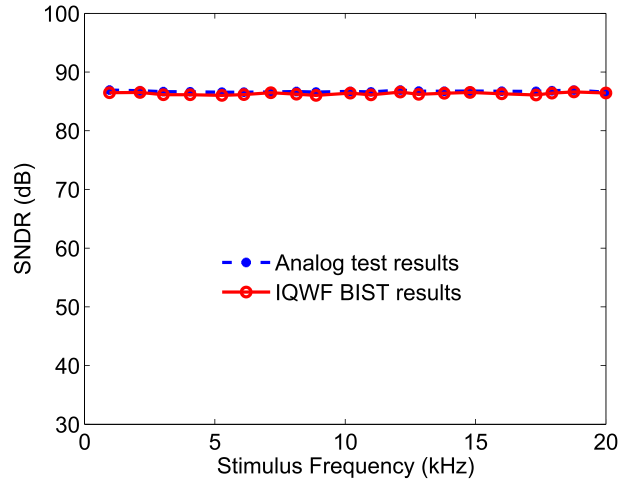

Fig. 11. Test results of SNDR versus stimulus frequency.

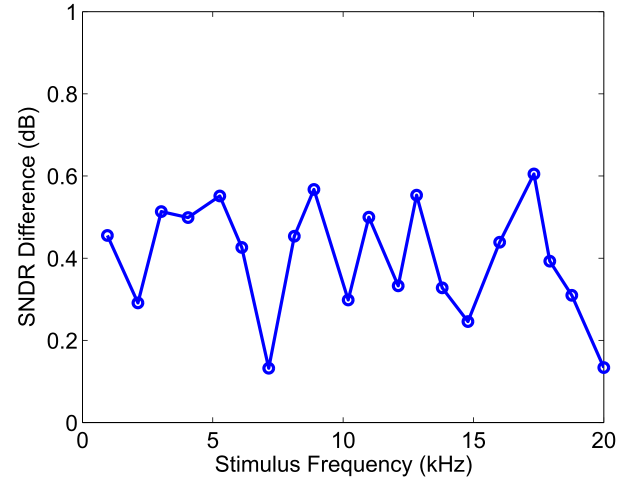

Fig. 12. SNDR differences of the SNDR versus stimulus frequency test.

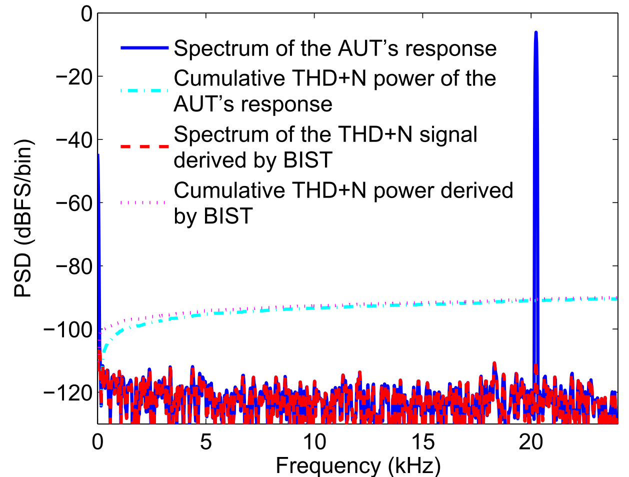

Fig. 13. Measured spectra of the AUTs output and the corresponding THD + N signal derived by the BIST circuitry in the 20 kHz, −6-dBFS test.

Fig. 13 further plots the measured spectra of the AUTs output and the corresponding THD + N signal in the 20 kHz, −6-dBFS test. As well as the 1 kHz, −6-dBFS test, the BIST circuitry successfully eliminates the offset and the stimulus-tone response from −44.6 and −6.1 dBFS to −110.7 and −109.7 dBFS, respectively. The results verify that the

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON

	[21]		This work	
Process	0.35 μm		0.18 μm	
AUT structure	2nd-order DfDT $\Delta\Sigma$ ADC		2nd-order D^{3}T $\Delta\Sigma$ ADC	
OSR	128		256	
Sampling rate	6.144 MHz		12.288 MHz	
Rated bandwidth	20 kHz		20 kHz	
DSG structure	2nd-order DSG×2		3rd-order DSG×3	
DSG hardware	6.1k gates		11.3k gates	
ORA hardware	5.6k gates		2.5k gates	
Analyzed sample no.	2048		2048	
BIST Method	Modified CSWF procedure		Proposed IQWF procedure	
BIST bandwidth	17 kHz		20 kHz	
Overall BIST hardware	13.3k gates		16.6k gates†	
Fully integrated	Yes		Yes	
	BIST	Analog test	BIST	Analog test
DR	81.6 dB	≅ 84 dB	92.6 dB	94.1 dB
Peak SNDR	75.5 dB	≅ 82 dB	88.0 dB	88.8 dB
A_T for the peak SNDR	−6 dBFS	−3 dBFS	−3 dBFS	−3 dBFS

†Including the BIST controller and the I2S interface.

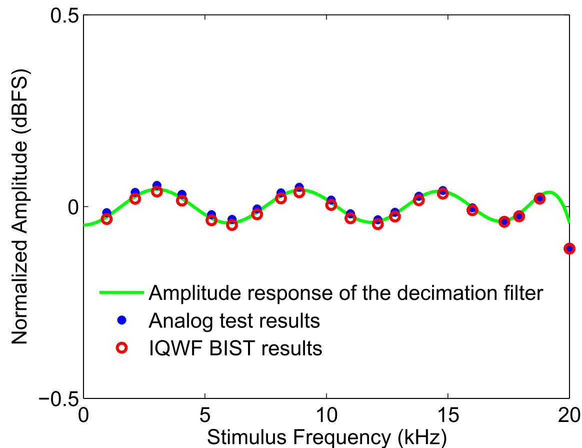

Fig. 14. Frequency response test results.

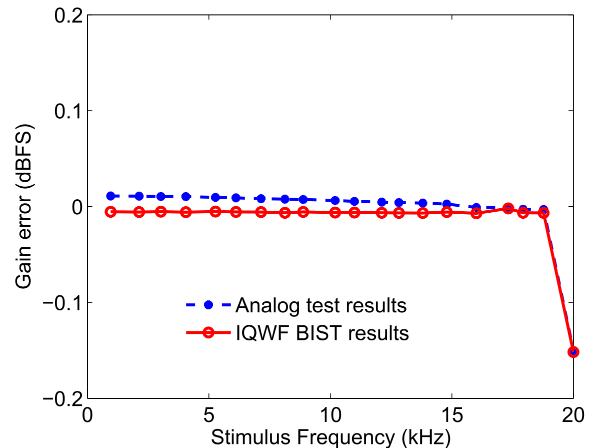

Fig. 15. Gain error test results.

fitted sine wave generated by the IQWF procedure precisely matches the stimulus-tone response, even though the MUTs phase shift varies more significantly at the higher stimulus frequencies. Hence, the proposed IQWF procedure successfully addresses the limited BIST bandwidth issue in [21].

E. Frequency Response Test Results

Fig. 14 shows the frequency-response test results in which the stimulus amplitude was kept at −6 dBFS. The passband ripples are mainly due to the intrinsic frequency response of the decimation filter design, which is also plotted on the figure. The BIST result of the 20-kHz test is less than the expected gain by 0.06 dB only. Since the corresponding FFT-based analog test also shows the same gain, the difference comes from the frequency response of the ΔΣ MUTs STF.

Fig. 15 shows the test results of the gain error of the AUT. The gain error is defined as the differences between the measured gains and the designed values including the deterministic passband ripples of the decimation filter. The test results indicate that the proposed BIST circuitry can accurately calculate the signal power.

Note that the frequency responses tested by the BIST are more reliable than those tested by the FFT-based analog tests. The reason is that the analog signal paths on the evaluation board may introduce unpredictable gain errors, which are hard to be precisely calibrated. On the other hand, all the analog signal paths of the BIST are within the AUT. Thus, all the tested frequency responses are due to the AUT itself. No calibration for the test environment is required. This is another advantage of the proposed BIST design.

Table IV summarizes the performance of the proposed BIST ADC and compares it with the previous work.

V. CONCLUSION

This paper demonstrated the fully integrated BIST ΔΣ ADC based on the proposed IQWF procedure. The all-digital BIST circuitry provided the SNDR, DR, frequency response, offset, and gain error of the AUT. Compared with the FFT-based test methods, the BIST circuitry benefited from its real-time computation so it did not need huge memory and only consisted of 16.6 k gates. Experimental results showed that the BIST circuitry reported a peak SNDR of 88.0 dB and a DR of 92.6 dB while the corresponding conventional analog tests resulted in 88.8 and 94.1 dB, respectively. Particularly, it is the first BIST ΔΣ ADC that achieves a test bandwidth as wide as the ADCs rated bandwidth thanks to the IQWF

procedure. The tested frequency responses of the BIST and those of the corresponding FFT-based analog tests were almost the same. Moreover, the BIST design can be modified to test the noise, individual harmonic distortion components, SFDR, and SNR by first testing for the coefficients a_i of the harmonic components of interest using the IQWF procedure. Once the coefficients are obtained, the aforementioned parameters can be calculated. The proposed BIST $\Delta\Sigma$ ADC eliminated the need of high-end AMS ATE without compromising test quality. It greatly reduced the test cost and provided a test solution for the applications in which conventional test resources are not available such as 3-D ICs.

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