# A Millimeter-Wave In-Phase Gate-Boosting Rectifier

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*Abstract*—This paper introduces a new class of RF-to-dc rectifiers called the in-phase gate-boosting rectifier (IGR). An IGR utilizes an in-phase passive voltage multiplier (IPVM) to boost *in-phase* $V_{\rm GS}$ swing from the driving $V_{\rm DS}$ swing. This design simultaneously reduces the effective threshold voltage, forward resistance, and the reverse leakage current of the rectifying transistor. As a consequence, the sensitivity and the efficiency of a high-frequency rectifier can be improved. Furthermore, a $C_G$-loaded IPVM presents low input conductance and is shunted with the drains/sources of the rectifying transistors. This makes the realization of the input matching network between the IGR core and the antenna easier, and achieves a higher voltage swing at the input terminals of the IGR core. The criteria, properties, and relating proofs of the IPVM are also discussed. A differential *seven*-stage millimeter-wave IGR is implemented in a 65-nm RF CMOS process. In this design, an interleaving internal threshold cancellation bias scheme is also introduced to further suppress the power consumption due to biasing circuitry without increasing the layout area. The implemented integrated circuit achieves a state-of-the-art $-7$-dBm sensitivity with 20% peak efficiency at 53 GHz and a bandwidth of 10 GHz from 46 to 56 GHz.

*Index Terms*—Energy harvesting, rectifying circuits.

## I. INTRODUCTION

HIGH-SENSITIVITY RF-to-dc rectifier is a key building block inside all passive RF identifications (RFIDs) and telemetric sensors. In these applications, dc power is directly extracted from the RF power captured in the surroundings. To embed these systems in almost every object [1], [2], the operating frequency should be increased to reduce the dimensions of the antenna. As the frequency moves higher, however, the sensitivity of the rectifiers drops quickly because the parasitic capacitance from the passive and the active devices starts to dominate.

Many authors have studied and invented creative techniques to improve the rectifiers' high-frequency performance. In both Dickson's [3] and the bridge architectures, reducing the forward voltage drop and the reverse leakage current of each diode improves sensitivity. The Schottky-junction diode has a relatively small forward voltage drop at a given bias current compared to a P/N junction diode, and has been used in [4]–[8]. The forward voltage drops can also be reduced by reducing the
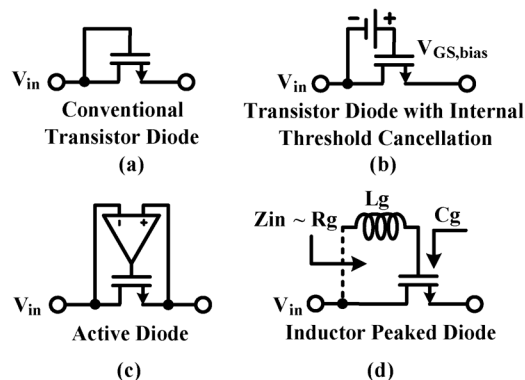
Fig. 1. Representative transistor diode designs used in a rectifier.

rectifying transistor's threshold voltage if it is made by a transistor diode. This is demonstrated in [9]–[11], which use native transistors with almost zero (40–50 mV) threshold voltage in a silicon on sapphire (SoS) process, and in [12], which programs the threshold voltage of the floating-gate transistors. Both SoS and floating-gate transistors require a special semiconductor process, which adds costs.

Efforts have been made to improve the sensitivity of rectifiers in the standard CMOS process. In a MOSFET process, the two-terminal diode can be implemented using a diode-connected MOSFET, as shown in Fig. 1(a). This diode-connected MOSFET rectifier has a threshold voltage issue, and its output current will be generated only when the instantaneous $V_{\rm in}$ is greater than the MOSFET threshold voltage $V_{\rm th}$.

In [13], a gate pre-charging technique is adopted to periodically charge the gate capacitor and to provide a gate bias voltage. In [14], the internal threshold-voltage cancellation (ITC) technique is proposed. ITC uses a diode-connected threshold voltage generator to generate a gate bias voltage from a rectifier's output dc voltage. In [15]–[18], a self-bias approach used in a single- and multiple-stage rectifier is proposed. This technique utilizes the internal dc voltages between each stage to bias the gates of the rectifying transistors in adjacent stages. These three techniques described in this paragraph all focus on providing a dc gate-to-source bias voltage $V_{\rm GS,bias}$ to the rectifying transistors, as shown in Fig. 1(b), so their effective threshold voltages can be reduced to $V_{\rm th} - V_{\rm GS,bias}$. A large $V_{\rm GS,bias}$ not only reduces effective threshold voltage, but also increases reverse leakage current. Besides, they have a startup problem because all internal voltages are initially zero. This means the input voltage swing still needs to be higher than the transistor's $V_{\rm th}$ for starting up.

Though using a comparator is infeasible in high-frequency application, it is instructive to look at the popular active-diode approach, as shown in Fig. 1(c) [19]. The active diode approach treats the rectifying transistor as a three-terminal device instead of a two-terminal diode by decoupling $V_G$ swing from $V_D$ swing. The instantaneous forward $V_{\rm GS} = V_{DD} - V_S$ is much

greater than $V_{\text{DS}}$. This dramatically improves forward conductance. In the reverse period, the rectifying transistor will be completely turned off to minimize the reverse leakage current.

The philosophy of treating the rectifying transistor as a three-terminal device is adopted in the inductor-peaking method proposed in [20] and [21]. Instead of ac-coupling drain voltage to the transistor's gate voltage, this approach utilized an inductor to generate a larger gate voltage swing, as shown in Fig. 1(d). This approach achieves good measurement results, but has two major problems. First of all, $V_{\text{GS}}$ and $V_{\text{DS}}$ are not *in-phase*. This generates excessive reverse leakage current. Secondly, the input impedance of the rectifier is low due to a series $L_G C_G$-resonant circuit. This small resonant impedance will shunt between drain to source and reduce the voltage swing of $V_{\text{DS}}$.

A better way to design a high-frequency rectifier is to generate a large *in-phase* $V_{\text{GS}}$ swing from the driving $V_{\text{DS}}$ as in the active diode in Fig. 1(c), but in a passive manner as in the inductor-peaking approach in Fig. 1(d). This sets the starting point of this work. This paper is organized as follows. Section II examines the role of a diode in a rectifier and introduces the basic concept of the in-phase gate-boosting rectifier (IGR) in a single-transistor-diode level. This diode uses an in-phase passive voltage multiplier (IPVM) to generate a large *in-phase* $V_{\text{GS}}$ swing from the input $V_{\text{DS}}$. Since the design of the IPVM is crucial for the IGR, criteria and proofs on the properties of IPVM will be discussed in Section III. The simplest design of the IGR is composed of only one transistor. In Section IV, both single-NMOSFET and single-PMOSFET IGR designs will be discussed. When a multiple-transistor IGR is built from single-transistor IGRs, the layout area can be excessive due to the large IPVM layout area used in each single-transistor IGR. An IPVM merging procedure can be carried out to reduce total layout area, as explained in Section V. To further suppress dc power consumption from the bias circuitry and to improve IGR's sensitivity, Section VI introduces interleaved internal threshold voltage (i.e., IITC) with simulation comparisons. In Section VII, the design details of a millimeter-wave IGR using TSMC 65-nm RF CMOS process will be discussed. Its experimental results are provided in Section VIII with discussions. Conclusions of this paper are drawn in Section IX.

## II. IN-PHASE GATE-BOOSTING RECTIFIER

The operating principle of an IGR can be best explained through design evolution in the single-transistor level. Starting from the ac-coupling topology with an ITC technique, as shown in Fig. 2(a), when an RF input $V_{\text{in}}$ is applied to the drain of the rectifying MOSFET, it is ac coupled to the gate through $C_C$. This creates a $V_{\text{GS}} = V_{\text{in}} + V_{\text{ITC,bias}}$, and the instantaneous overdrive voltage is now $V_{\text{in}} - (V_{\text{th}} - V_{\text{ITC,bias}})$. Instead of using a coupling capacitor $C_C$ to couple the $V_D$ to $V_G$, if we can introduce an ac voltage gain from drain voltage $V_D$ to gate voltage $V_G$ as conceptually shown in Fig. 2(b), the instantaneous gate overdrive voltage will be increased to

$$V_{\text{OV}} = A_v \cdot V_{\text{in}} - (V_{\text{th}} - V_{\text{ITC,bias}})$$
$$= A_v \cdot \left( V_{\text{in}} - \frac{V_{\text{th}} - V_{\text{ITC,bias}}}{A_v} \right). \qquad (1)$$
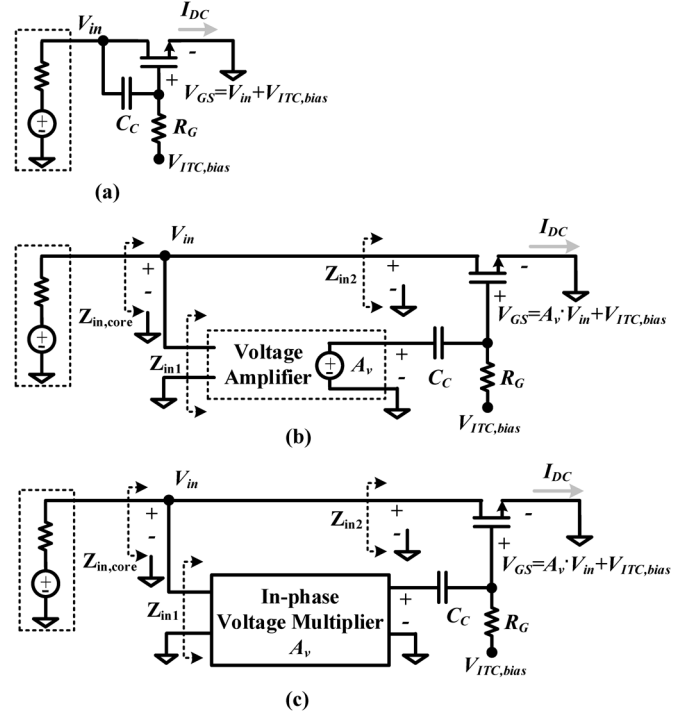


Fig. 2. Evolution of a single-transistor IGR using an IPVM. For explanation purposes, the source is connected to ground here.

From (1), the effective threshold voltage is reduced to $(V_{\text{th}} - V_{\text{ITC,bias}})/A_v$. This means even when no gate bias $V_{\text{ITC,bias}}$ is presented, the effective threshold voltage can still be reduced by a factor of $A_v$. This relieves the startup problem in all gate-biasing techniques if the voltage gain $A_v$ can be achieved in a passive manner. The peak overdrive voltage is increased by a factor of $A_v$, which reduces the forward resistance $R_{\text{on}}$ by the same factor. Similarly, during the negative $V_{\text{in}}$ period, the overdrive voltage becomes more negative. This suppresses leakage current during the negative input voltage swing. Since the effective threshold voltage, forward resistance, and reverse leakage current are all reduced, both the output power and RF-to-dc power conversion efficiency (PCE) will be increased.

In this paper, the *in-phase* voltage amplification $A_v$ is realized through the use of a passive network, as shown in Fig. 2(c). The difficult part for the passive realization of $A_v$ is that all passive networks are reciprocal, and this creates couplings between its input and output ports. This coupling problem is relieved if this passive network satisfies IPVM criterion, as will be elaborated upon in Section III. The IPVM increases the ac gate voltage swing to $A_v \times V_{\text{in}}$ while maintaining a well-controlled $C_G$-loaded impedance $Z_{\text{in1}}$ under input driving signals $V_{\text{in}}$. Under the ITC biasing, the instantaneous gate overdrive voltage is now (1). In normal usage, the output current $I_{\text{DC}}$ will drive a load resistor $R_L$ or a large charge-storage capacitor.

The $I_D V_D$-curves of a Schottky diode reported in [22] is compared with a conventional diode-connected low-$V_{\text{th}}$ nMOS transistor and various IPVM-driven low-$V_{\text{th}}$ nMOS transistors. The Schottky diode has an $I_D = 50 \cdot (e^{V_D/35\,\text{mV}} - 1)$ nA. Since this comparison focuses on the conceptual $I_D V_D$ behavior with different IPVMs, ideal voltage-controlled voltage sources (VCVSs) with $A_v$ voltage gain are used to mimic the in-band behavior of an IPVM, as shown in Fig. 3. The nMOS
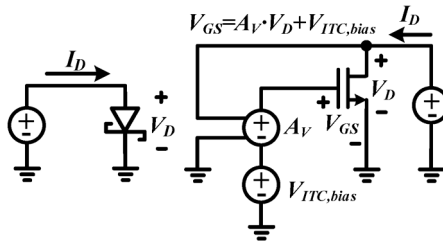
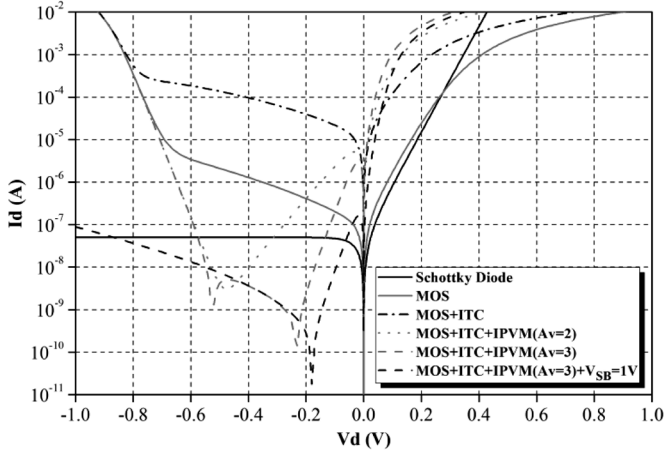Fig. 3. Simulation setup for comparison presented in Fig. 4.



Fig. 4. $I_D$ versus $V_D$ for a Schottky diode, a conventional diode-connected low-$V_{\text{th}}$ nMOS transistor, and various IPVM-driven nMOS transistor with different $A_v$ values.
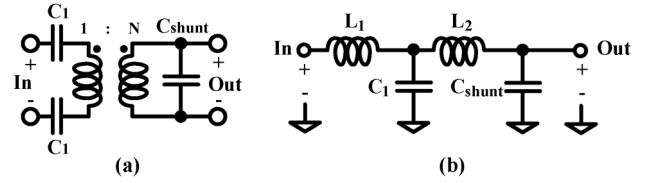


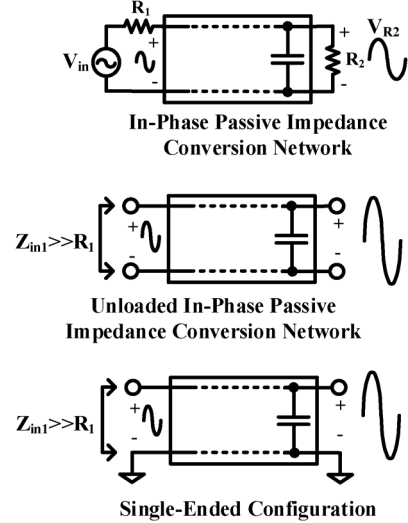Fig. 5. (a) Differential IPVM example. (b) Single-ended IPVM example.



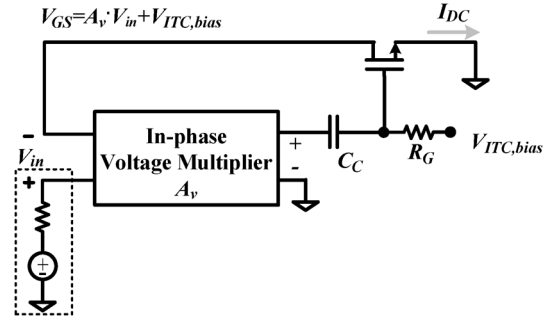Fig. 6. Passive in-phase voltage multiplier in loaded and unloaded conditions.



Fig. 7. Series input IGR based on a two-port IPVM does not exist.

transistor has a low-$V_{\text{th}}$ (300 mV) and a $W/L = 12 \ \mu\text{m}/60$ nm. The $V_{\text{ITC,bias}}$ chosen in this simulation is a typical 200 mV.

The simulated $I_D$ versus input voltage $V_D$ characteristics are plotted in Fig. 4. Though this comparison is not quantitatively meaningful between the Schottky diode and the IPVM-driven nMOS transistors due to different $I_D$ to $V_D$ behaviors, it does show that IPVM-driven nMOS transistors provide an improved forward conductance with increased $A_v$. Besides, a larger $A_v$ also provides a lower reverse leakage current. IPVM-driven nMOS transistors ($A_v > 1$) are advantageous to both the diode-connected transistor and the traditional ITC design [14].

Special attention should be paid to the large negative input swing. When $V_D$ is too negative ($V_D < -0.5$ V in our simulations), the bulk to drain P/N junction will be forward biased. This introduces a very large reverse leakage current through the drain-substrate path. A negative substrate bias voltage can reduce this substrate leakage current, also shown in Fig. 4, with $V_{\text{SB}} = 1$ V. Also note that the overall IGR input impedance, which is equal to $Z_{\text{in1}} \| Z_{\text{in2}}$. Here, $Z_{\text{in1}}$ is the input impedance looking into IPVM and $Z_{\text{in2}}$ is the total impedance looking into the drain of the rectifying transistor in Fig. 2. To achieve the largest $V_{\text{in}}$ at a specified input power, $Z_{\text{in1}}$ should be large or conjugately matched.

### III. IN-PHASE VOLTAGE MULTIPLIER

Any passive network that satisfies the following two criteria and one optional condition serves as an IPVM.

1) It is a passive impedance conversion network matching an input resistor $R_1$ to an output resistor $R_2$ at the design frequencies. No limitations on the values of $R_1$ and $R_2$ are assumed since this network will be used in an unloaded manner.

2) The phase of the loaded forward transmission coefficient is equal to 0° or 180° at the design frequencies depending on the polarity of the transistors. (*Note:* $V_{\text{GS}}$ and $V_{\text{DS}}$ of the rectifying transistors will still be *in-phase*, as will be explained in Section IV.)

3) (*Optional*) The last nominal element at the output of the IPVM design should be a shunt capacitor $C_{\text{shunt}}$.

Any impedance matching networks that satisfy the IPVM criteria can be used as an IPVM, and it can be implemented using either single-ended or differential topology, as exemplified in Fig. 5(a) and (b). For the differential IPVM, the sign of voltage gain can be swapped by exchanging the $+/-$ terminals of the output port. If the IPVM is single-ended, negative terminals of both the input and the output ports are grounded. In the IPVM of Fig. 5(b), the phase difference between the input and the output ports is 180°.
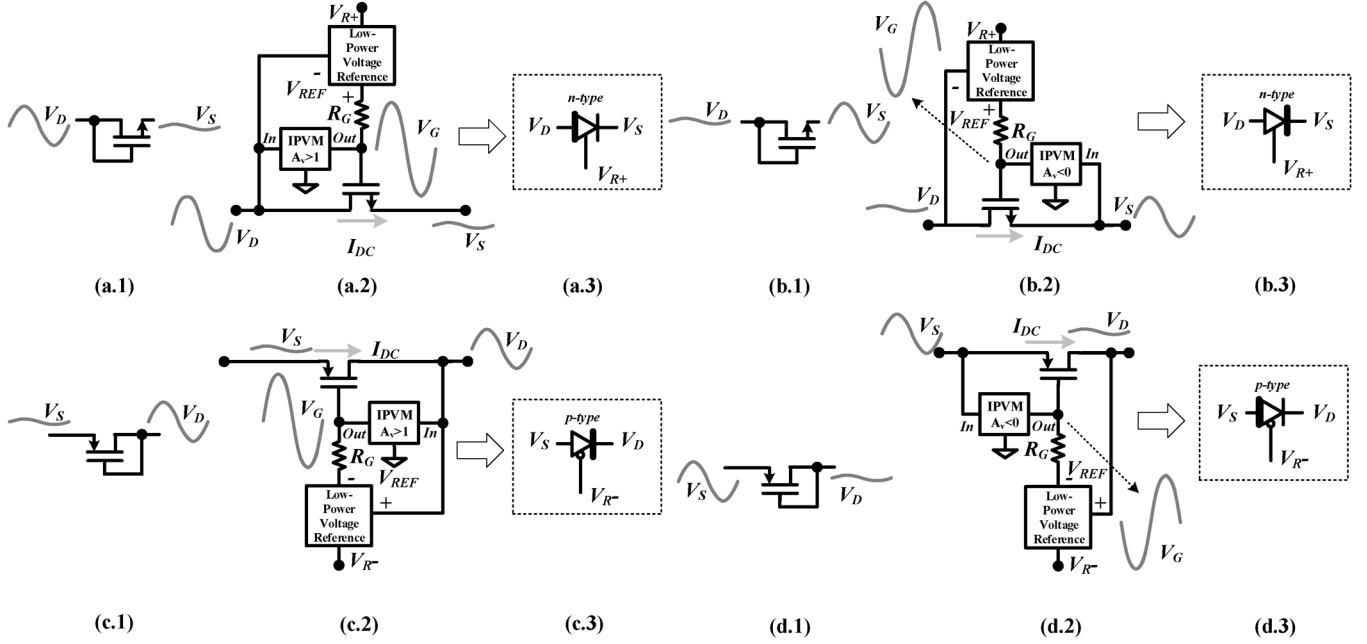
Fig. 8. Evolution of IPVM single-transistor rectifier. High-frequency voltage waveform of a signal period is illustrated for different terminals. *N-type* rectifier with higher voltage swing at: (a) drain or (b) source, and *p-type* rectifier with higher voltage swing at: (c) drain or (d) source.

From criterion 1), since the network is an impedance conversion network, the input and output voltage swing under matched condition will be

$$V_{R2} = V_{\text{in}} \cdot \sqrt{\frac{R_2}{R_1} \cdot \eta_{\text{passive}}}. \tag{2}$$

Here, $V_{\text{in}}$ is the input voltage swing, and $V_{R2}$ is the output voltage swing across load resistor $R_2$, as shown in Fig. 6. $\eta_{\text{passive}}$ is the single-trip passive efficiency of this network. If $R_2$ is connected, the input impedance will be $R_1$. Now, if we remove the load resistor $R_2$, the reflected voltage wave will not be phase shifted, and hence, a $2V_{R2}$ will appear across the open load. At the input port, the reflected voltage wave $V_{\text{in}}\eta_{\text{passive}}$ is added constructively with the input signal due to criterion 2). Due to round-trip power loss, the voltage swing of the reflected wave is smaller by a factor of $\eta_{\text{passive}}$. The unloaded voltage swing across the input port will now be increased to $V_{\text{in}}(1 + \eta_{\text{passive}})$. However, the reflected current is *out-of-phase* with the input current wave, and the unloaded current at the input node is now $V_{\text{in}}/R_1 \times (1 - \eta_{\text{passive}})$. This will make the unloaded input impedance of this IPVM equal to

$$Z_{\text{in1}} = \frac{R_1(1 + \eta_{\text{passive}})}{(1 - \eta_{\text{passive}})}. \tag{3}$$

If the loss of this IPVM is small, $Z_{\text{in1}}$ will be much larger than $R_1$, as shown in Fig. 6. This large $Z_{\text{in1}}$ is important in practical design, as it will be shunted with $Z_{\text{in2}}$, as in Fig. 2(c). This large shunt $Z_{\text{in1}}$ will load the input matching network minimally. This is opposite to the cases in [20] and [21]. In the inductor-peaking method, $Z_{\text{in}}$ from the passive network will be a small $R_g$ at the resonant frequency, as shown in Fig. 1(d). The unloaded voltage gain is now

$$A_v = \frac{2}{(1 + \eta_{\text{passive}})} \cdot \sqrt{\frac{R_2}{R_1} \cdot \eta_{\text{passive}}}. \tag{4}$$

It is slightly larger than the matched voltage gain when $\eta_{\text{passive}}$ is close to unity.

The $C_{\text{shunt}}$ in condition 3) is used to absorb the IPVM effective load capacitance from the gates of rectifying transistors, as shown in Fig. 2(c). The $C_{\text{shunt}}$ in the nominal design is realized completely by the effective load capacitance including the effect of coupling capacitors $C_C$, the effective gate capacitance $C_G$, and the IPVM's own port parasitic capacitance.

A natural extended question to the evolved IGR in Fig. 2(c) is if it is possible to sense the input current instead of the input voltage in a passive manner using a two-port IPVM, as shown in Fig. 7. The answer is *no*. A series input requires a small unloaded input impedance, which means, the reflected voltage phase should be 180°. This corresponds to a ±90° phase of loaded forward transmission coefficient, and a ±90° difference in $V_{\text{GS}}$ and $V_{\text{DS}}$. This will create excessive reverse leakage current.

## IV. SINGLE-MOSFET IGR

In a practical rectifier design, the drain of the diode-connected MOSFET may not always have a greater voltage swing than the source. In this case, connecting $V_D$ to the input of IPVM is not an effective way of using it. Since a two-terminal diode can be implemented using an nMOS transistor, as shown in Fig. 8(a.1) and (b.1) or using a pMOS transistor, as shown in Fig. 8(c.1) and (d.1), either the drain or the source of the MOSFET will have a larger ac voltage swing with reference to the RF ground.

Take the diode in Fig. 8(a.1) for example, where the amplitude of $V_D$ is greater than the amplitude of $V_S$. In this case, we would like to use $V_D$ to create a large *in-phase* voltage swing using an $A_v > 1$ IPVM and apply it to the gate of the rectifying transistor, as shown in Fig. 8(a.2). This creates an *in-phase* $V_{\text{GS}} = A_v \cdot V_{\text{DS}}$ voltage swing, and hence, an improved performance compared to a typical diode-connected configuration.
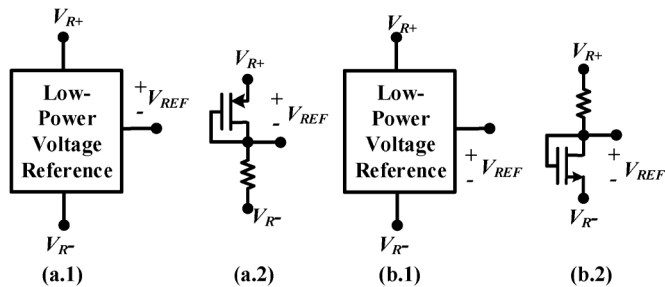
Fig. 9. Examples of: (a) *p-type* and (b) *n-type* VR circuits.

On the other hand, if the source voltage swing $V_S$ is larger than $V_D$, as shown in Fig. 8(b.1), it will be better to create an *out-of-phase* voltage swing $V_G$ based on $V_S$ using an $A_v < 0$ IPVM and feed it to the gate of the rectifying transistor, as shown in Fig. 8(b.2). This creates a $V_{\mathrm{GS}} = (1 + |A_v|) \cdot V_{\mathrm{DS}}$ voltage swing. Even though the IPVM has an *out-of-phase* voltage gain, the $V_{\mathrm{GS}}$ and $V_{\mathrm{DS}}$ are still *in-phase*. Also, since $V_{\mathrm{GS}} = (1 + |A_v|) \cdot V_{\mathrm{DS}}$, the magnitude of the voltage gain of this *out-of-phase* IPVM only needs to be greater than zero to create a greater-than-$V_{\mathrm{DS}}$ voltage swing.

For the pMOS IGR, if the drain voltage swing $V_D$ is greater than $V_S$, as shown in Fig. 8(c.1), we would like to create an *in-phase* $V_G$ voltage swing based on $V_D$ using an $A_v > 1$ IPVM, as shown in Fig. 8(c.2). This creates an *in-phase* $V_{SG}$ equal to $A_v \cdot V_{SD}$. However, if the source voltage swing $V_S$ is greater than $V_D$, as shown in Fig. 8(d.1), it will be better to create an *out-of-phase* voltage swing $V_G$ based on $V_S$ using an $A_v < 0$ IPVM and feed it to the gate of the rectifying transistor, as shown in Fig. 8(d.2). This creates an *in-phase* $V_{SG}$ equal to $(1 + |A_v|)V_{SD}$.

In Fig. 8(a.2), (b.2), (c.2), and (d.2), a low-power voltage reference (VR) is used to provide a gate bias voltage for internal threshold voltage cancellation. For the pMOS transistor, Fig. 9(a.1) is used to generate a reference voltage $V_{\mathrm{REF}}$ output between the positive supply terminal $V_R+$ and the output terminal. For the nMOS transistor, Fig. 9(b.1) is used to generate a reference voltage $V_{\mathrm{REF}}$ output between the output terminal and the negative supply terminal $V_R-$. For both cases, design examples from [14] are shown in Fig. 9(a.2) and (b.2).

To simplify the drawings of schematics in later sections, several symbols are introduced in Fig. 8 to represent a single-transistor IGR with an ITC. Fig. 8(a.3) symbolizes the schematic of Fig. 8(a.2). A thick line on the anode identifies the terminal with greater ac voltage swing. A pin-line ending at $V_R+$ from the side denotes the positive supply pin for the VR. Similarly, Fig. 8(b.3) shows the symbol for Fig. 8(b.2) with a thick line on the cathode to identify the terminal with greater ac voltage swing. For PMOS-IGR, the symbols are similar with an additional circle at the head of the negative supply pin.

## V. MULTIPLE-TRANSISTOR IGR

To extend the single-MOSFET IGR into a multiple-stage Dickson's rectifier, as shown in Fig. 10, the most straightforward method is to replace each diode in Fig. 10 using the most suitable single-MOSFET IGR from Fig. 8. To exemplify this design process and to point out important implementation issues,
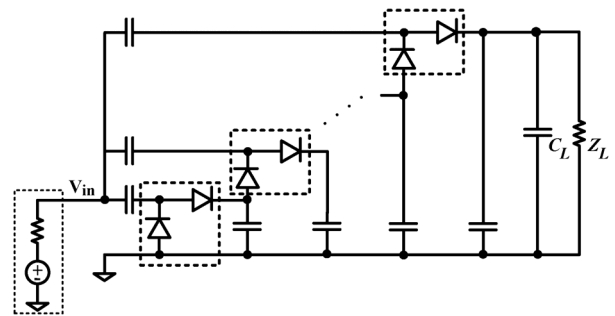


Fig. 10. Multiple-stage rectifier. Each stage can be implemented using either one of the single-MOSFET IGRs from Fig. 8.
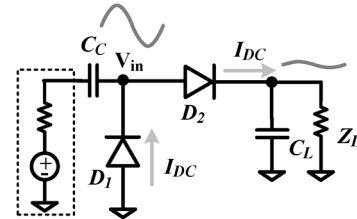


Fig. 11. Single-stage Dickson's rectifier.

let us first focus on converting the single-stage voltage-multiplier in Fig. 11 into an IGR using single-MOSFET IGRs. Since there is diode $D_1$ and diode $D_2$ in Fig. 11 and each of them can be either *p-type* or *n-type*, there will be four totally different implementations, as shown in Fig. 12(a), (b), (d), and (e). If $D_1$ is *p-type* and $D_2$ is *n-type*, then this implementation is called a *pn-type* rectifier. The rest of the implementations follow the same naming rule.

The first issue with this replacement is that each diode needs one IPVM, so a total of two IPVMs will be required for a single-stage IGR. If we continue this replacement to the multiple-stage rectifier, the total layout area will be excessively large.

Several unitary IPVMs with similar voltage gain can be merged and shared through the use of ac-coupling capacitors, as shown in Fig. 13. The merged IPVM is a parallel equivalent circuit. Since the output is usually connected to VR-biased transistor gates, the ac-coupling capacitors $C_{C,n}$ where $n = 1$ to $N$ are used to isolate dc bias voltages between different output terminals. It can be seen that the two single-transistor IGRs in Fig. 12(b) use their own unitary $A_v < 0$ IPVMs. These two unitary IPVMs can be merged into one so the schematic in Fig. 12(b) now becomes the schematic in Fig. 12(c). The same process is carried out to convert the schematic in Fig. 12(e) into a new schematic in Fig. 12(f).

In a differential IGR design, there will be both positive ($V_{\mathrm{RF,in}}+$) and negative ($V_{\mathrm{RF,in}}-$) input voltages. Besides, $V_{\mathrm{RF,in}}+$ and $V_{\mathrm{RF,in}}-$ will need different IPVMs with both positive and negative $A_v$. Merging them using a parallel equivalent circuit method in Fig. 13 will still end up with four different IPVMs, as shown on the left-hand side of Fig. 14. Since all signals are differential, we can acquire the approximate output swings $V_{\mathrm{RF,out1}}+$, $V_{\mathrm{RF,out2}}+$ from the positive output terminal, and acquire the approximate output swing $V_{\mathrm{RF,out1}}-$, $V_{\mathrm{RF,out2}}-$ from the negative output terminal of only one differential IPVM, as shown on the right-hand side in Fig. 14. The ac-coupling capacitors $C_{C,n}$ where $n = 1$ to
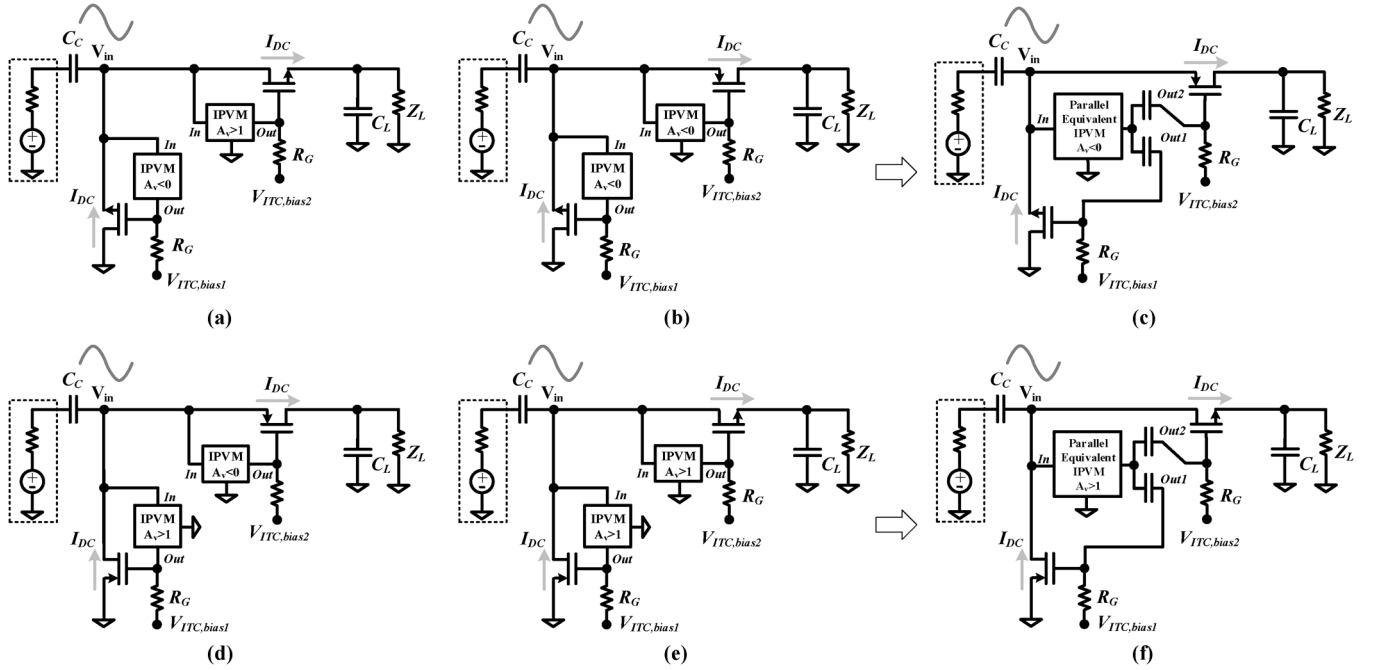
Fig. 12. Single-stage IGR has four different implementations, which are: (a) *nn-type*, (b) *np-type*, (d) *pp-type*, and (e) *pn-type*. Merging two unitary IPVMs in (b) and in (e) into one parallel equivalent IPVM becomes (c) and (f), respectively.
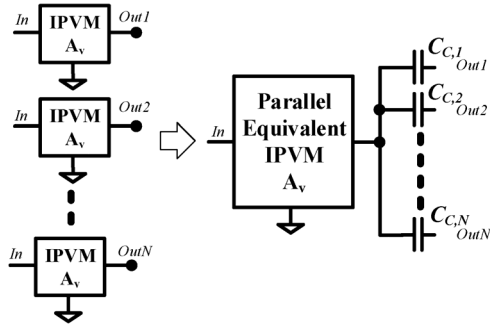


Fig. 13. Merging several IPVMs with similar $A_v$ into one parallel equivalent IPVM with output ac-coupling capacitors $C_{C,n}$ where $n = 1$ to $N$. When merging the IPVMs, the admittance of each IPVM is scaled by $N$ and the voltage swing of each node is kept the same.
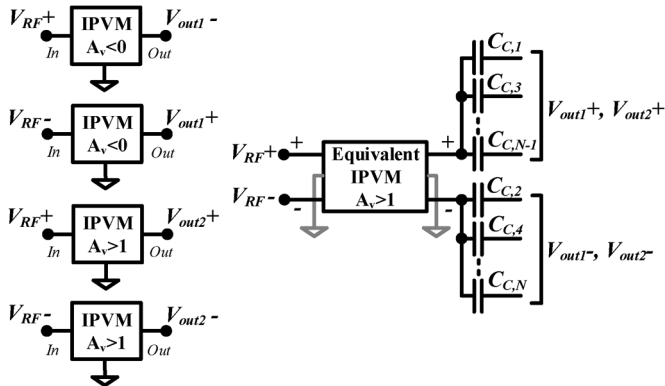


Fig. 14. Merging several positive- and negative-$A_v$ IPVMs using one approximately equivalent IPVM with output ac-coupling capacitors $C_{C,n}$, where $n = 1$ to $N$.

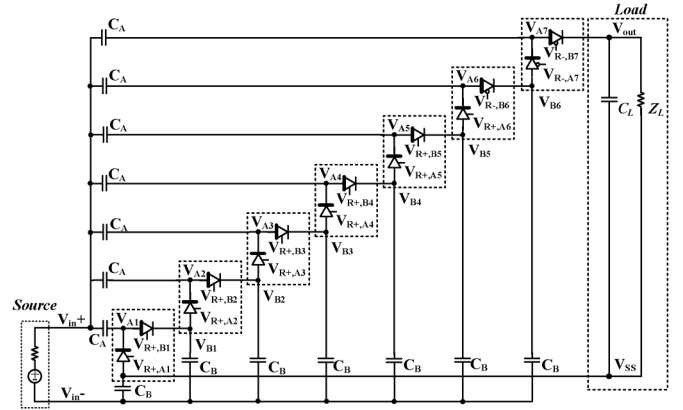$N$ will also be necessary to isolate dc bias voltages between different output terminals.



Fig. 15. Multiple-stage IGR with bias pins unconnected.

## VI. IITC BIAS SCHEME

In this paper, a *seven*-stage IGR is studied and designed to verify the proposed concepts. 60 GHz is chosen as the design frequency for the unlicensed industrial–scientific–medical (ISM) band. The number of stages is *seven*, which is chosen *a priori* to fit in the proximity of the physical IPVM, as explained in Section VII. The initial architecture of the proposed IGR is shown in Fig. 15. The bias pin $V_{R\pm,An}$ and $V_{R\pm,Bn}$ (where $n = 1$ to 7) of each single-MOSFET IGR in this figure is left unconnected to explain the bias scheme in this section. The input matching network is not placed and the IPVM is not merged at this point.

All IGR stages other than the last two stages are implemented using nMOS transistors due to their higher $f_T$. The last three rectifying transistors have to be implemented in pMOS transistors; otherwise, there will not be sufficient positive dc voltage to supply the nMOS low-power VR. The schematic of each stage
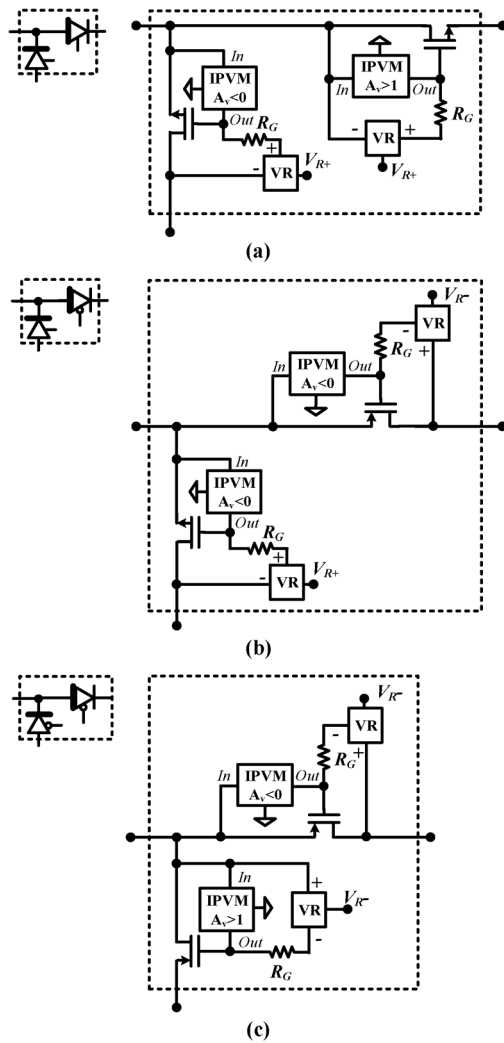
Fig. 16.   Block diagram of the IGR.



Fig. 17.   Bias-scheme diagram for the: (a) conventional ITC and (b) proposed IITC.
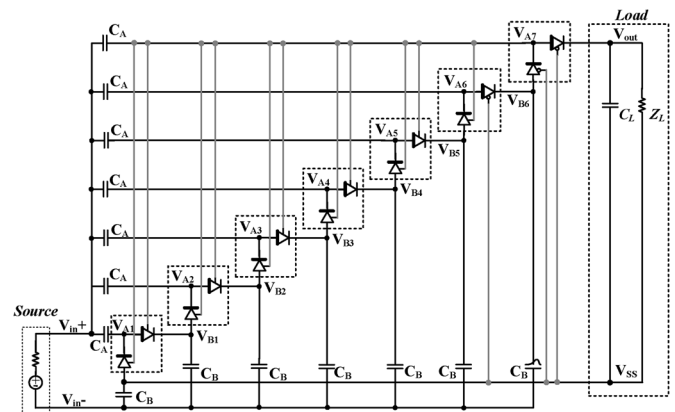


Fig. 18.   Schematic of Fig. 15 with conventional ITC bias scheme.

is shown in Fig. 16. Note, the IPVMs in these single-MOSFET IGRs are still not merged in these figures.

To prepare for connecting the supply pins ($V_{R\pm,An}$ or $V_{R\pm,Bn}$), a bias-scheme diagram is used for illustration in Fig. 17. This diagram can be composed by denoting the relative voltage levels of each internal nodes ($V_{An}$ or $V_{Bn}$, $n = 1$ to 7) along the $y$-axis, with the $x$-axis being the ground level. In Fig. 15, $V_{An} \approx ((n - 0.5)/7) \times V_{\text{out}}$ and $V_{Bn} \approx n/7 \times V_{\text{out}}$. A secondary $x$-axis is placed at the top of this diagram to represent most positive voltage $V_{\text{out}}$.

We can place the voltage of each supply pin ($V_{R\pm,An}$ or $V_{R\pm,Bn}$) on a proper site inside this diagram to illustrate dc bias design. For a conventional ITC design, supply pins of all nMOS single-MOSFET IGRs are connected to $V_{\text{out}}$, and the supply pins of all pMOS single-MOSFET IGRs are connected to $V_{SS}$, as shown in Fig. 17(a). Applying this bias scheme to the circuit in Fig. 15 will translate it into the circuit of Fig. 18.

Though the VR in each single-MOSFET IGR consumes little power, static subthreshold leakage current due to bias is normally reduced through the use of long-channel transistors. However, the CMOS gate oxide in a 65-nm CMOS process introduces nontrivial gate leakage current when the gate area is increased after the channel length is increased.
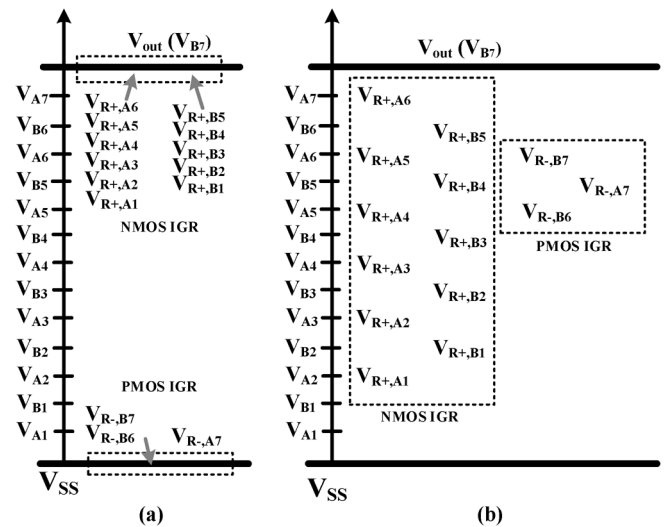
Since a low-power VR will work as long as sufficient voltage difference is provided, an alternative way to reduce dc power consumption can be achieved by connecting each bias pin $V_{R\pm,An}$ to a lower dc voltage under $V_{\text{out}}$, and each $V_{R\pm,Bn}$ to a higher dc voltage over $V_{SS}$. In this design, each bias pin $V_{R\pm,An}$ is chosen as *three* IGR-dc voltage drops above the nMOS source, and each $V_{R\pm,Bn}$ is also chosen as *three* IGR-dc voltage drops below the pMOS source. This corresponds to the IITC bias scheme, as shown in Fig. 17(b), and its corresponding circuit is shown in Fig. 19. Simulation results of the RF input power $P_{\text{in}}$ to dc output voltage $V_{\text{out}}$ for an IGR based on the conventional ITC and the other one based on the proposed *three*-IGR-voltage-drop IITCs is presented in Fig. 20. The IGR based on *three*-IGR-voltage-drop IITCs used in this simulation uses the final schematic shown in Fig. 22. This final design is used as a baseline and is modified into a new IGR based on the conventional ITC bias scheme. All device sizing used in both simulations are the same, except for metal interconnections for their VRs.

From this simulation, it can be found that using the interleaved-ITC improves the sensitivity by 3 dB. Besides, if we reduce the IITC bias scheme to a *two*-IGR-voltage-drop IITC bias scheme, a slightly worse sensitivity will be achieved due to insufficient voltage to bias the VR. If we change it to the
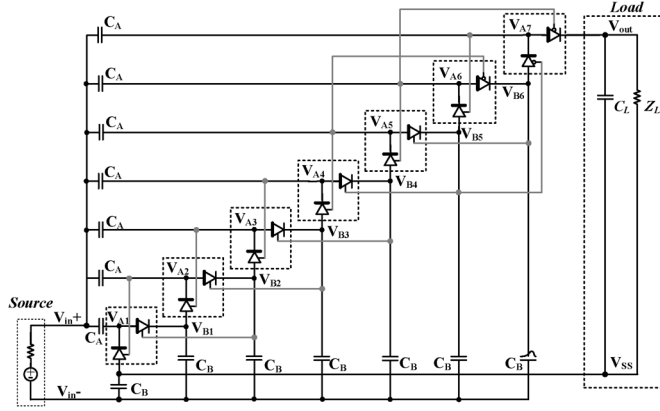
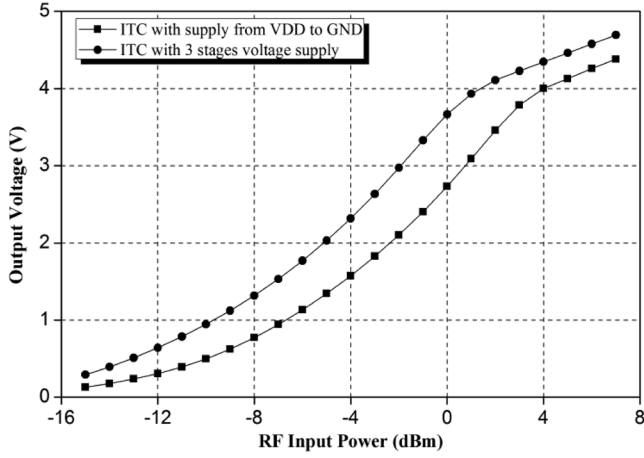Fig. 19. Schematic of Fig. 15 with the proposed IITC bias scheme.



Fig. 20. Simulation results of a seven-stage rectifier using the conventional ITC and the proposed IITC.
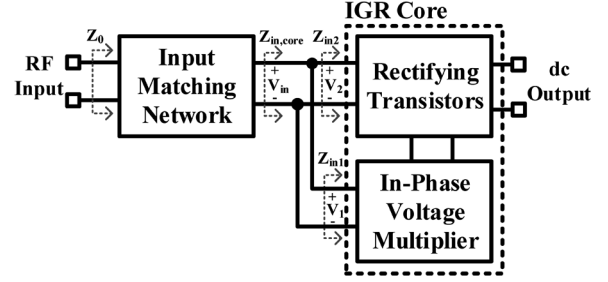


Fig. 21. Block diagram of a complete IGR. The IGR core includes the rectifying transistors and the IPVM.

TABLE I
COMPONENT VALUES OF THE SCHEMATIC IN FIG. 22

| Input Matching | | | |
|---|---|---|---|
| $L_{Series}$ | 83 $pH$ | $C_{Shunt}$ | 114 $fF$ |
| **IPVM Network** | | | |
| $C_1$ | 126 $fF$ | $L_2$ | 216 $pH$ |
| $L_1$ | 125 $pH$ | $M$ | 83 $pH$ |
| **Core Rectifying Transistors** | | | |
| $W_n$ | 900 $nm \times 8$ | $L_n$ | 60 $nm$ |
| $W_p$ | 900 $nm \times 18$ | $L_p$ | 60 $nm$ |
| **VR for NMOS** | | | |
| $W_n$ | 400 $nm$ | $L_n$ | 600 $nm$ |
| $R_{B,nmos}$ | 500 $k\Omega$ | | |
| **VR for PMOS** | | | |
| $W_p$ | 400 $nm$ | $L_p$ | 600 $nm$ |
| $R_{B,pmos}$ | 500 $k\Omega$ | | |
| **Others** | | | |
| $C_{C,nmos}$ | 60 $fF$ | $C_{C,pmos}$ | 120 $fF$ |
| $C_A = C_B$ | 93 $fF$ | $R_G$ | 10 $k\Omega$ |

*four*-IGR-voltage-drop IITC bias scheme, a slightly worse sensitivity will result due to a larger bias power consumption and the use of an additional pMOS rectifying transistor.

## VII. MILLIMETER-WAVE IGR SCHEMATIC DESIGN

In Fig. 19, each single-MOSFET IGR has its own IPVM, which is costly in area. These unitary IPVMs are merged based on the procedures illustrated in Fig. 14. In addition, the complete IGR will need an input matching network to convert the IGR core impedance $Z_{in,core}$ to the external port impedance $Z_0 = 100\ \Omega$, as shown in Fig. 21. After the merging of unitary IPVMs and the insertion of the input matching network, a final schematic of the reported *seven*-stage IGR is illustrated in Fig. 22. The component values for each device are shown in Table I. The width and length of transistors are denoted by $W_{n/p}$ and $L_{n/p}$ with either subscript $n$ or $p$ to represents nMOS and pMOS, respectively. $L_{Series}$ and $C_{Shunt}$ are the input matching components. In the IPVM network, $C_1$ is the series capacitor, $L_1$ is the primary inductor of the transformer, $L_2$ is the secondary inductor of the transformer, and $M$ is the mutual inductance. $R_{B,nmos}$ and $R_{B,pmos}$ are the current limiters in the VR circuits. $C_{C,nmos}$ and $C_{C,pmos}$ are the gate coupling capacitors of the rectifying transistors. $C_A$ and $C_B$ are the ac-coupling capacitors and $R_G$ is the ac signal blocker.

From the output terminals of the merged differential IPVM to the gate of each rectifying transistor, a coupling capacitor

$C_{C,nmos}$ or $C_{C,pmos}$ is necessary to isolate different gate dc bias voltages from each transistor, as shown in Fig. 22. The three pMOS rectifying transistors have doubled gate widths compared to the gate widths of nMOS rectifying transistors to match their conductance. $C_{C,pmos}$ is also two times the value of $C_{C,nmos}$ to match their voltage coupling factor $A_{coupling}$. $C_{C,nmos}$ and $C_{C,pmos}$ correspond to $C_{Cn}$ with integer $n$ in Fig. 14. The voltage coupling factor $A_{coupling}$ can be calculated by

$$A_{\text{coupling,nmos}} \equiv \frac{v_{g,\text{nmos}}}{v_{\text{IPVM,out}}\pm} = \frac{C_{C,\text{nmos}}}{C_{G,\text{nmos}} + C_{C,\text{nmos}}} \approx$$
$$A_{\text{coupling,pmos}} \equiv \frac{v_{g,\text{pmos}}}{v_{\text{IPVM,out}}\pm} = \frac{C_{C,\text{pmos}}}{C_{G,\text{pmos}} + C_{C,\text{pmos}}} \quad (5)$$

where $A_{coupling,nmos}$ and $A_{coupling,pmos}$ are the coupling factors $A_{coupling}$ for nMOS and pMOS, respectively. $v_{g,nmos}$ and $v_{g,pmos}$ are the coupled ac voltage swings at the gates of nMOS and pMOS transistors, respectively. $v_{IPVM,out}+$ and $v_{IPVM,out}-$ are the voltage swings at the IPVM positive and negative output terminals, respectively. $C_{G,nmos}$ is the equivalent total parasitic capacitance looking into the gate of a single nMOS transistor. From the simulation, $C_{G,nmos}$ is 6.8 fF. $C_{G,pmos}$ is twice the value of $C_{G,nmos}$.

In order to reduce the voltage drop across the coupling capacitors $C_{C,nmos}$ and $C_{C,pmos}$, $A_{coupling}$ should be close
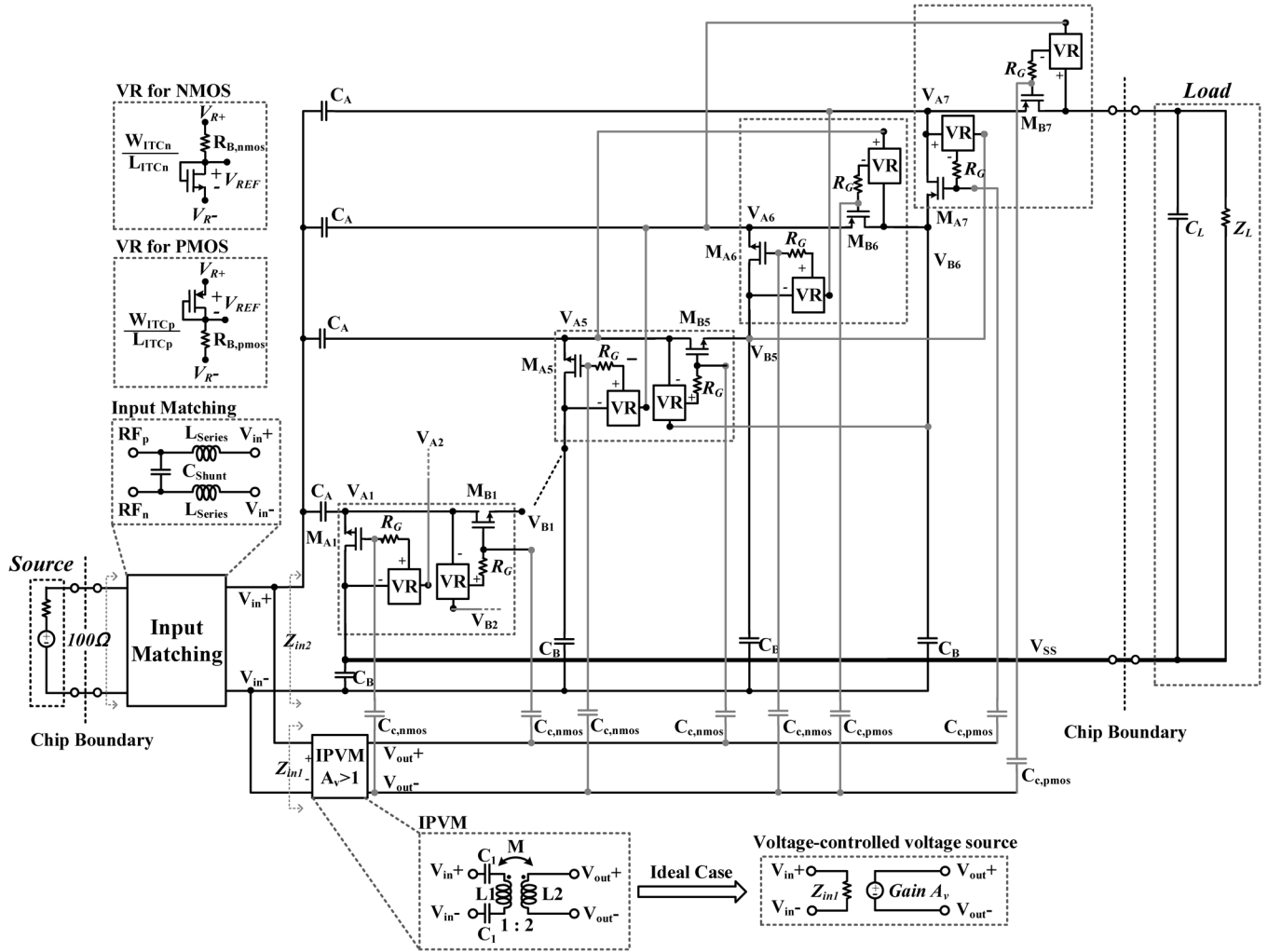
Fig. 22.   Complete schematic of the reported millimeter-wave *seven*-stage IGR. The VCVS is used in the ideal case simulation.

to unity. This means large coupling capacitors are preferable. However, if the coupling capacitors are too large, $C_{C,\text{pmos}}$ will reach self-resonant frequency (SRF). Besides, the layout area of the complete *seven*-stage core will be too large for millimeter-wave operations. In our design, $C_{C,\text{nmos}}$ is chosen as 60 fF and $A_{\text{coupling,nmos}}$ is roughly 0.9. Increasing the $C_{C,n}$ above 60 fF results in little improvements in $A_{\text{coupling,nmos}}$. Avoiding unnecessary large capacitors can also prevent the uncertainties in modeling high-frequency capacitors. The $C_{C,\text{pmos}}$ used has an SRF of 136 GHz.

Unlike gate coupling capacitors, drain coupling capacitors ($C_A$ and $C_B$) store charges in one-half of the $V_{\text{in}}$ period, and discharge to the next stage in the other half of the $V_{\text{in}}$ period. The major design consideration for choosing $C_A$ and $C_B$ in addition to the layout area and SRF is the $RC$-time constant in each rectifier's charge–discharge cycle. If the drain coupling capacitors are too small, the maximum charge transfers in each half period will also be small. This limits the rectifier's output current and efficiency. Since the conductance of the nMOS and pMOS transistors are matched, their equivalent *drain-to-source resistance* will be the same. Thus, same drain coupling capacitors are used for both nMOS and pMOS transistors. The ac voltage gain across $C_A$ and $C_B$ is $A_{\text{coupling,drain}}$. Due to the capacitive

divisions from both the gate and drain capacitors, the effective IPVM gain $A_{\text{eff}}$ for the rectifying transistors will be slightly different from the IPVM gain $A_V$. It is defined as

$$A_{\text{eff}} \equiv \frac{V_{\text{GS}}}{V_{\text{DS}}} = A_V \times \frac{A_{\text{coupling}}}{A_{\text{coupling,drain}}}. \qquad (6)$$

In order to bias the gate rectifying transistor from the VR, a 10-k$\Omega$ $R_G$ resistor is used. This resistor is large enough to isolate ac signals from the VR. For the VR part, $R_{B,\text{nmos}}$ and $R_{B,\text{pmos}}$ limit its current consumption. The larger the $R_{B,\text{nmos}}$ and $R_{B,\text{pmos}}$ are, the smaller the current that the VRs consume. In this design, both of them are chosen as 500 k$\Omega$. This resistance is large enough without requiring excessive layout area. In addition, few metal interconnections are used so as to prevent their parasitic capacitance from loading sensitive internal nodes.

The effective load capacitance at the positive output terminal of the IPVM is

$$C_{L+,\text{IPVM}} \approx 5 \cdot C_{\text{GS,nmos}} + 5 \cdot C_{\text{GD,nmos}}(1 + 1/A_{\text{eff}})$$
$$+ C_{\text{GS,pmos}} + C_{\text{GD,pmos}}(1 + 1/A_{\text{eff}}) \quad (7)$$

for a total of six nMOS transistors and one pMOS transistor connected. Similarly, load capacitance for the negative output terminal of the IPVM is

$$C_{L-,\text{IPVM}} \approx 6 \cdot C_{\text{GS,nmos}} + 6 \cdot C_{\text{GD,nmos}}(1 + 1/A_{\text{eff}})$$
$$+ 2 \cdot C_{\text{GS,pmos}} + 2 \cdot C_{\text{GD,pmos}}(1 + 1/A_{\text{eff}}). \quad (8)$$

This is an approximate expression because the coupling capacitors $C_{C,\text{nmos}}$ and $C_{C,\text{pmos}}$ will slightly decrease $C_{L+,\text{IPVM}}$ and $C_{L-,\text{IPVM}}$ from the right-hand sides of (7) and (8). The IPVM sees $C_{L,\text{IPVM}}$, which is the series equivalent capacitance of $C_{L+,\text{IPVM}}$ and $C_{L-,\text{IPVM}}$. From the simulation results, $C_{L,\text{IPVM}}$ is 25 fF.

In this design, the IPVM network is designed first due to its requirement of a 1:2 transformer with a high SRF. This ratio is chosen at an early design stage since we initially and conceptually postulate an larger turn ratio can generate greater $V_{\text{GS}}$ swing. As a result, $V_{\text{GS}} \approx 2 \times V_{\text{DS}}$ can be generated to increase the performance. With the selection of transformer being made, the IPVM network in Fig. 5(a) is designed based on the extracted transformer model. The larger the transformer's outer diameter is, the smaller $C_{\text{shunt}}$ can be used to absorb $C_{L,\text{IPVM}}$. Besides, the transformer has its own shunt parasitic capacitance $C_{\text{TFM,shunt}}$, which is directly related to the SRF. In this design

$$C_{\text{shunt}} = C_{\text{TFM,shunt}} + C_{L,\text{IPVM}}. \quad (9)$$

Since the IPVM used in this IGR contains a 1:2 transformer, and its SRF is kept above 60 GHz, the outer diameter of the transformer is limited to be smaller than 70 $\mu$m built from a 3.4-$\mu$m copper layer and a 0.9-$\mu$m aluminum underpass layer 3.7 $\mu$m above the 10 $\Omega \cdot$ cm-resistivity *p-type* silicon substrate. The optimal number of stages and IPVM design to achieve minimal sensitivity are still subject to future studies.

Therefore, the transformer inside the chosen IPVM topology should have an SRF sufficiently larger than 60 GHz to leave room for the absorbing $C_{L,\text{IPVM}}$, and this limits the outer diameter to be below 70 $\mu$m. If the outer diameter is too small, the $C_{\text{shunt}}$ can be made large. However, the coupling factor of the transformer itself will be worsened, which lowers the IPVM voltage gain $A_v$. In this design, a 65-$\mu$m outer diameter 1:2 transformer is chosen with a 19-fF $C_{\text{shunt}}$. According to HFSS simulation, the one-turn main inductor is 125 pH, the two-turn secondary inductor is 216 pH, and their mutual inductance is 82.6 pH. From coupling factor equation $k = M/\sqrt{L_{\text{outer}} \times L_{\text{inner}}}$, $k$ is 0.5 in this design. It introduces a 2.2$\times$ post-simulated differential IPVM voltage gain at 60 GHz.

The simulation of the IPVM with a load capacitor equivalent to $C_{L,\text{IPVM}}$ at 60 GHz can be found in Fig. 23. In this ac simulation, the IPVM is HFSS simulated, as shown in Fig. 27, and both the coupling capacitors and the transistors are parasitics extracted using foundry-provided parasitic extraction (PEX) rules. It can be seen that the voltage transfer function of the proposed IPVM network reaches an *in-phase* condition at 58 GHz with a 2.2 input-to-output voltage gain. The phase response deviates from 0° when the signal frequency is different. However,
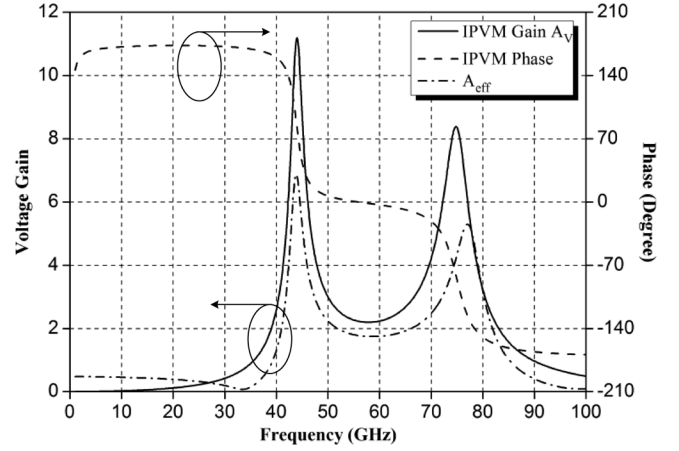


Fig. 23. Voltage transfer function of the proposed differential IPVM network. The load capacitor is a fixed value, which is equivalent to the $C_{L,\text{IPVM}}$ at 60 GHz,, where $C_{L,\text{IPVM}}$ is 25 fF. $A_{\text{eff}}$ is the effective IPVM gain for rectifying transistors defined by $V_{\text{GS}}/V_{\text{DS}}$.



Fig. 24. Transient waveform of $V_{\text{GS}}$, $V_{\text{DS}}$, and the charging current $I_{\text{DS}}$ when the IGR is working in-phase at 60 GHz with a 0.8-V dc output voltage.

a 52–62-GHz bandwidth can be achieved with ±4° phase deviations. It should also be pointed out that on two edges of the IPVM bandwidth, even though the phase deviates from the *in-phase* condition, the magnitude response gets larger. This is a *preferable* property of the proposed IPVM. Even though more leakage current will be generated due to larger phase mismatches between $V_{\text{GS}}$ and $V_{\text{DS}}$, a larger forward current can also be generated due to the larger $A_v$ at the edges of IPVM bandwidth. This property helps increase the bandwidth of the IGR core circuitry.

The operation of the IGR can be better understood through transient simulations. Fig. 24 shows the $V_{\text{GS}}$, $V_{\text{DS}}$, and $I_{\text{DS}}$ waveforms of $M_{A2}$ when driven by a 60-GHz source with 560-mV peak-to-peak voltage. From Fig. 23, the IPVM creates an *in-phase* condition with an effective gain $A_{\text{eff}} = 1.8$. This corresponds to $V_{\text{GS}} = |A_{\text{eff}}| \cdot V_{\text{DS}}$, which can be clearly seen in the transient simulations of $V_{\text{GS}}$ and $V_{\text{DS}}$ in Fig. 24. Besides, $V_{\text{GS}}$ and $V_{\text{DS}}$ are *in-phase*. This creates a large forward-conduction current and little reverse leakage current, as shown in $I_{\text{DS}}$ waveforms in the same figure. At high frequency, instantaneous leakage currents are required to charge and discharge the parasitic capacitors in each transistor, and the magnitude of
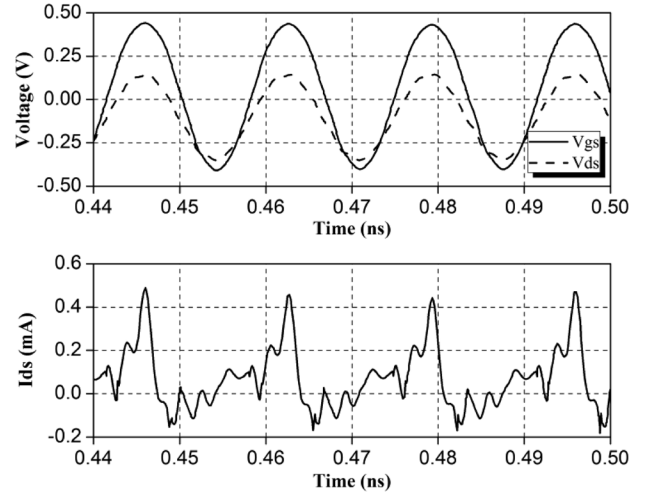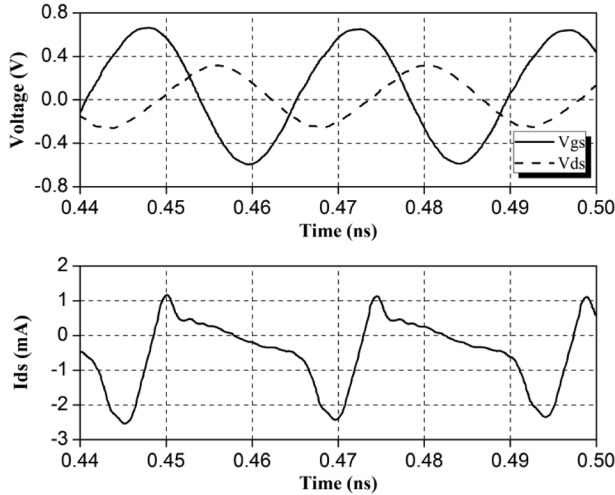
Fig. 25.　Transient waveforms of $V_{GS}$, $V_{DS}$, and the charging current $I_{DS}$ when the IGR is working at 41 GHz with a 0.8-V dc output voltage.
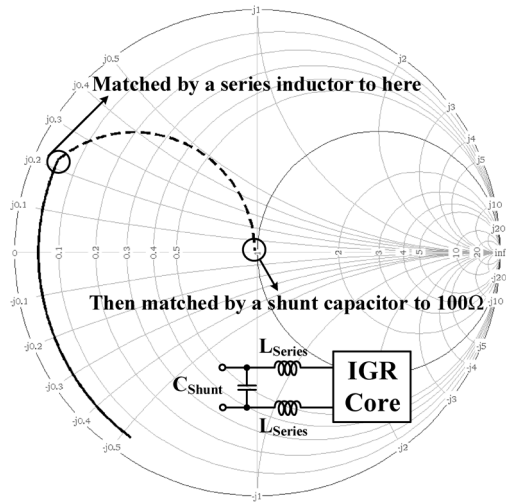


Fig. 26.　L-section input matching design for the proposed IGR.

the instantaneous $I_{DS}$ is larger compared to the low-frequency $I_{DS} - V_{DS}$ curve in Fig. 4. However, the dc component of reverse leakage $I_{DS}$ will still be very small due to the fact that the transistor is deeply cut off.

An *out-of-phase* condition is demonstrated in Fig. 25 at the operating frequency of 41 GHz. Under the circumstances, the IPVM creates a phase of 140° between $V_{GS}$ and $V_{DS}$ with an effective gain $A_{eff} = 2$. This corresponds to $V_{GS} = (|A_{eff}|\angle 140°) \cdot V_{DS}$. This *out-of-phase* condition creates a large reverse leakage current and a small forward-conducting current. Unlike conventional approaches, an IGR core can discharge the load capacitor and result in negative output voltage, as shown in this case. This phenomenon can happen at an *out-of-band* frequency where the IPVM phase shift is greater than 90° from its center frequency. However, this is practically not an issue in a complete IGR design. A negative output load voltage will be discharged through the forward-conducting substrate contacts, and a narrowband input matching network will dramatically reduce the *out-of-band* RF power reaching the IGR core.

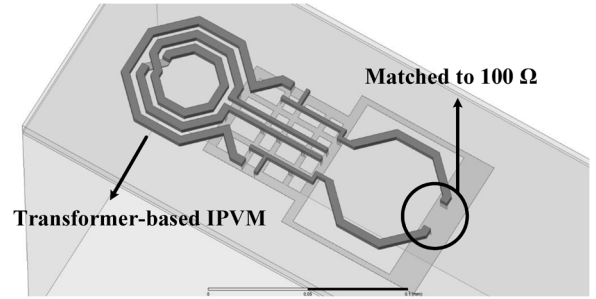In this design, a simple L-section impedance matching network is used to match the IGR core small-signal input



Fig. 27.　3-D structure of the IPVM and the input matching networks.

impedance to the 100-$\Omega$ external impedance. It includes a first differential inductor connecting to the core and a shunt capacitor at the port, as shown in Fig. 26. The values of $C_{Shunt}$ and $L_{Series}$ are shown in Table I. In general, the input impedance of any rectifiers is nonlinear and is dependent on the input power. However, this design targets a minimal sensitivity, and hence, a small-signal input matching is carried out. The IGR core small-signal input impedance is equal to $Z_{in1}$ and $Z_{in2}$ connected in parallel (see Fig. 22). Here, $Z_{in1}$ is the input impedance of the IPVM and $Z_{in2}$ is the input impedance of drain/source terminals of the rectifier core circuit. At the center frequency,

$$Z_{in1} = 175\ \Omega \| 1/(j\omega(79\ fF)) \qquad (10)$$

and

$$Z_{in2} = 766\ \Omega \| 1/(j\omega(186\ fF)). \qquad (11)$$

The real part of $Z_{in1}$ is large, as explained in Section III. Its imaginary part comes from the equivalent parasitic shunt capacitance in $C_1$ inside the IPVM. The differential equivalent input capacitance $C_{in2}$ of $Z_{in2}$ is equal to 186 fF. It comes mainly from the $C_{GS}$ in the rectifying nMOS and pMOS transistors

$$
\begin{aligned}
C_{in2} \approx\ & \frac{1}{2} \cdot (11 \cdot C_{GS,nmos} + 3 \cdot C_{GS,pmos}) \cdot (1 + A_{eff}) \\
& + \frac{1}{2} \cdot (11 \cdot C_{GD,nmos} + 3 \cdot C_{GD,pmos}) \cdot (1 - A_{eff}) \\
& + 11 \cdot C_{DS,nmos} + 3 \cdot C_{DS,pmos}.
\end{aligned} \qquad (12)
$$

As a consequence, the small-signal input impedance of the IGR core is mainly capacitive. This capacitance is absorbed by the input matching network, and will not affect the operation of IGR core circuits. The input matching network is simulated by Ansoft HFSS using the 3-D structure, as shown in Fig. 27.

To understand the advantages of the proposed IGR, simulations have been made to compare the performance of rectifiers with and without an IPVM. Several different rectifiers are simulated and compared. In these simulations, every component is the same, except for the IPVM part and the input matching part. In the first simulation, no IPVM is used. All rectifying transistors are ac-coupled diode-connected with ITC. In the second simulation, an ideal VCVS with $A_v = 2$ is used, as also shown in Fig. 22, with various input impedance $Z_{in1}$. In the last simulation, the circuit of our final design is used. The IPVM is HFSS simulated. In these simulations, ideal lossless conjugately matched L-section input matching networks are independently
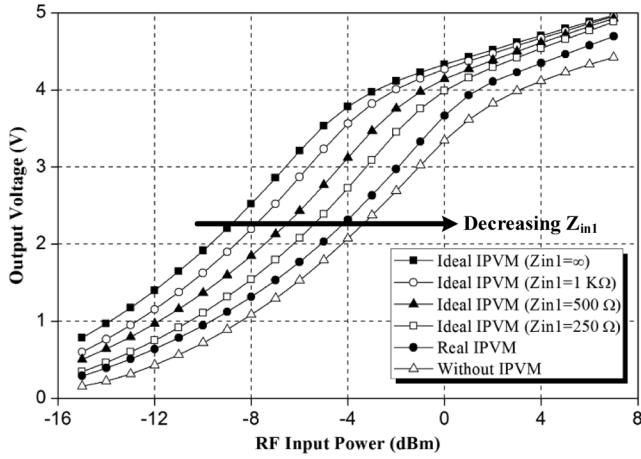
Fig. 28. IGR output voltage comparisons with and without IPVM networks. The various input impedances of an ideal IPVM are also presented.



Fig. 29. Output voltage comparisons among several rectifiers using different circuit techniques.

designed to provide a fair comparison of the core circuits. Their simulation results are plotted in Fig. 28. From this figure, the ideal VCVS-case with infinite $Z_{in1}$ achieves the best sensitivity. This suggests boosting the gate voltage swing does help significantly in improving sensitivity. Moreover, the lower the $Z_{in1}$ is, the lower the impedance between the input matching network and IGR core will be. A lower impedance at this node results in a smaller voltage swing for the same RF input power. Therefore, it is shown that the sensitivity is worse for a lower $Z_{in1}$. The difference between an ideal VCVS and the real IPVM is the inevitable passive loss, which lowers the effective core input impedance. Given this loss, the real IPVM still improves the sensitivity of a conventional ITC rectifier by an average of 1 dB in most input power levels. However, efforts should be made in the future to reduce the passive loss of the IPVM.

More insights can be discovered if the IITC and IPVM are used separately. Fig. 29 shows the rectifiers' performance with different combinations of the IITC and IPVM. First of all, the IITC and IPVM can individually improve the power sensitivity by a big margin comparing to the conventional rectifier. Moreover, the IPVM technique prevails over the IITC technique in the low input power region because IITC consumes power and cannot be turned on when the voltage level is not enough. However, the output voltage grows fast using IITC as the input power increases and eventually IITC becomes better than the IPVM technique in the high input power region. The IGR, which uses both IITC and IPVM techniques, improves the performance in the high input power region, but it is worse than the IPVM-only case in the low input power region. This is because IITC generates additional leakage current, which degrades low power performance. On the other hand, the loss of the IPVM influences significantly on the sensitivity performance. An output voltage simulation of the IGR using an ideal IPVM and the same IITC circuitry is also provided in Fig. 29, which implies that there is a room to improve the IGR. Efforts should be made on improving the IPVM networks in the future, as emphasized earlier.

## VIII. EXPERIMENTAL RESULTS

The design in Fig. 22 is implemented in TSMC 65-nm RF CMOS technology. Most of the layout area of this IGR is used for the IPVM and the input matching network, as shown in the
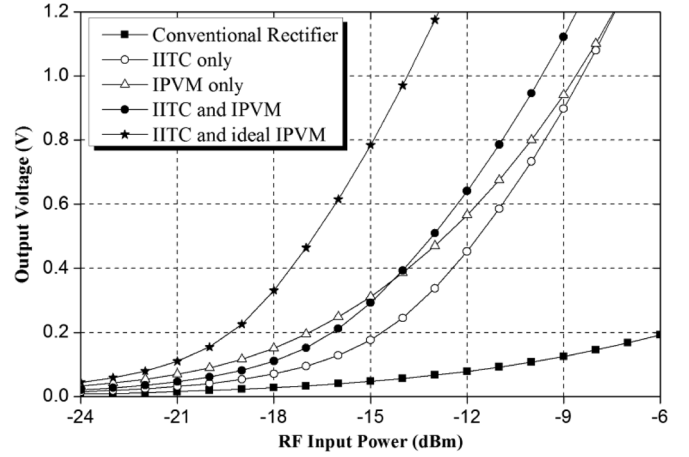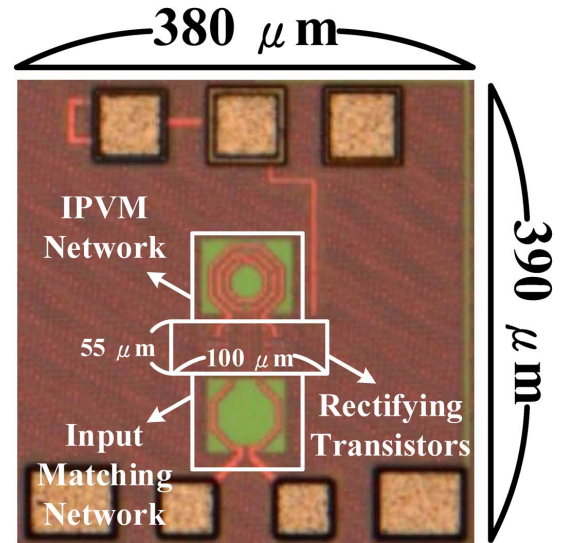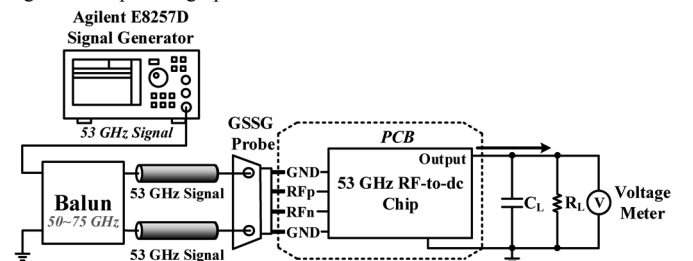


Fig. 30. Chip micrograph.



Fig. 31. Measurement setup of this IGR driving a load capacitor and a load resistor.

micrograph in Fig. 30. The *seven*-stage rectifying transistors, VRs for biasing, and coupling capacitors only occupy an area of 380 $\mu$m × 390 $\mu$m.

Two different measurement setups are used to evaluate the performance of the implemented integrated circuit (IC). In the first typical setup shown in Fig. 31, a load capacitor is directly connected to the dc output port of the IC. Depending on experiments, various resistors are used to mimic actual load circuits. The output voltage is measured by a voltage meter. This IGR IC is designed with differential input pads for further integration with an on-chip antenna. In both setups, the single-ended input signals are converted to differential signals
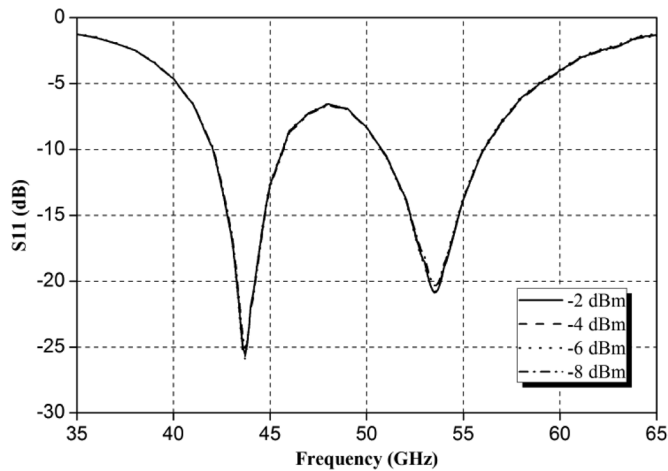
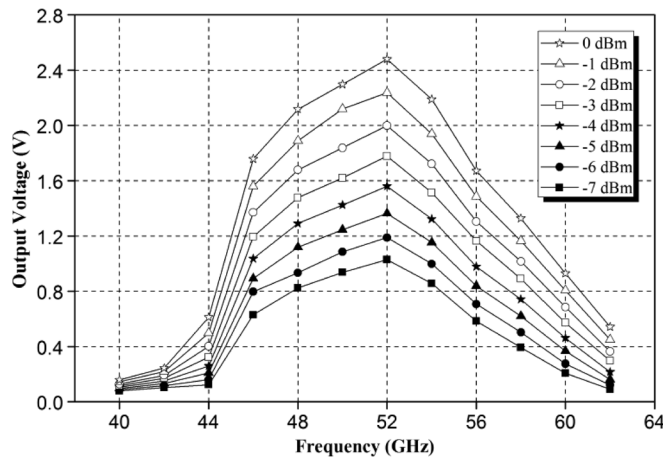Fig. 32. Measured $S_{11}$ of the *seven*-stage IGR.



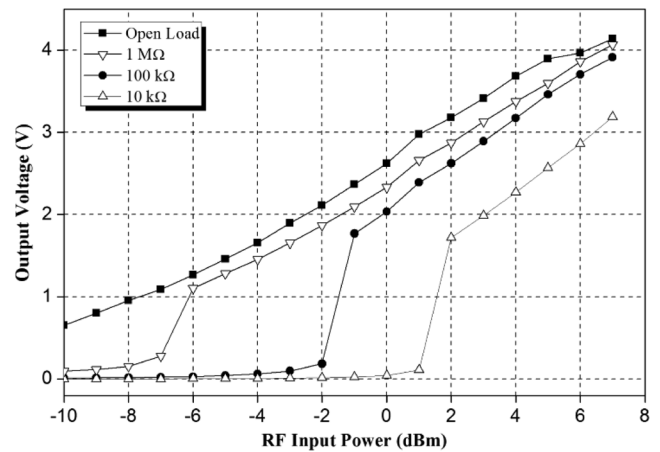Fig. 33. Output voltage driving an open load at different frequencies.



Fig. 34. Measured IGR output voltage with various load resistors at 53-GHz RF input.
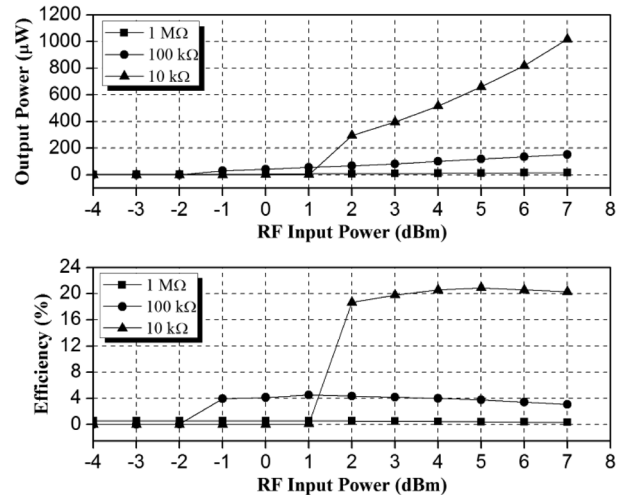


Fig. 35. Output power and efficiency of the IGR driving various load resistors at 53 GHz.

using a 50–75-GHz wideband balun before being applied to the ground–signal–signal–ground (GSSG) probe. All measurement is accomplished using differential probes.

The input matching behavior is first measured using an Agilent E8361A network analyzer. Since the input impedance of an IGR is nonlinear, the measured input $S_{11}$ for different input power levels is shown in Fig. 32. At small input power, this IC achieves $-20$ dB of $S_{11}$ at 53 GHz and different input power levels from $-8$ dBm up to $-2$ dBm result in the same $S_{11}$.

When the output is open loaded, output dc voltage for different RF input power and different frequencies are shown in Fig. 33. From the measurement, this design is most sensitive from 46 to 56 GHz, and the peak sensitivity is achieved at 53 GHz. The 3-dB bandwidth of the output dc voltage is from 46 to 56 GHz. To further explore the $V_{\text{out}}$ versus different input power levels when driving different load resistors at peak-sensitivity frequency, different input power has been applied to an open, 1-, 100-, and 10-k$\Omega$ resistive loads, and the measurement result is shown in Fig. 34. From this figure, this IGR can give a 1.1-V output on an open load using a $-7$-dBm input power. For large input power, a large dc output voltage can be generated. This voltage is distributed across all transistors, and the instantaneous $V_{\text{GD}}$ and $V_{\text{GS}}$ will still be much less than $V_{\text{out}}$. From the measurement, it is found that this IGR can provide a 4-V output voltage without reliability issues. Besides, the reverse

substrate PN junction breakdown voltage is much greater than 4 V.

When the load resistance is decreased, the IGR sensitivity drops. From the output voltage measurement at various load resistors, we can calculate output power and efficiency for different input power levels, as shown in Fig. 35. From this figure, the smaller the load resistance is, the higher the power-conversion efficiency can be achieved. This is valid only for the loads larger than 10 k$\Omega$, which achieves the peak power-conversion efficiency of the IGR.

To understand the optimal load resistance for delivering maximum output dc power, a second setup is used, as shown in Fig. 36. In this setup, the load capacitor is mainly served as an output bypass capacitor before being connected to the dc measurement cables. A voltage source is placed across the output port, and an internal current meter is used to measure the dc current flowing into the voltage source. Note that the optimal load resistor to achieve maximum efficiency is different when a different input power is applied. Several experiments have been carried out, and the results for 0- and 7-dBm input power are shown in Fig. 37. The results show that at 0-dBm input power, the IGR can provide 91-$\mu$W maximum output power at 9.1% efficiency. This is achieved with an equivalent 10-k$\Omega$ load. Since
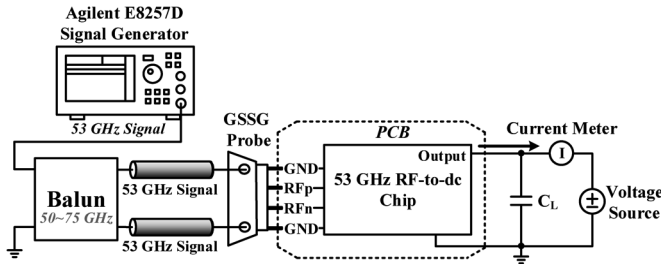
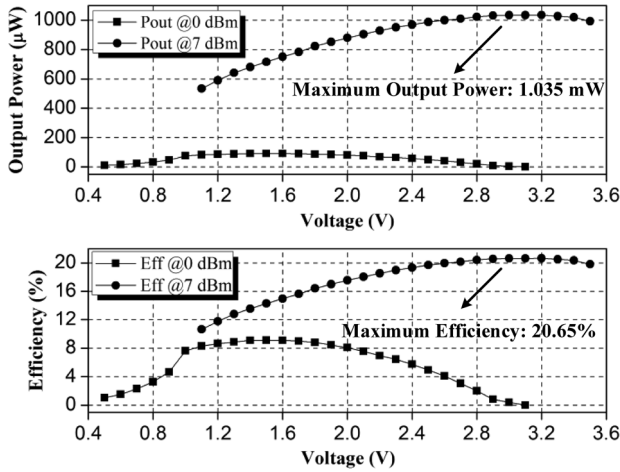Fig. 36. Measurement setup to find optimal load resistance.



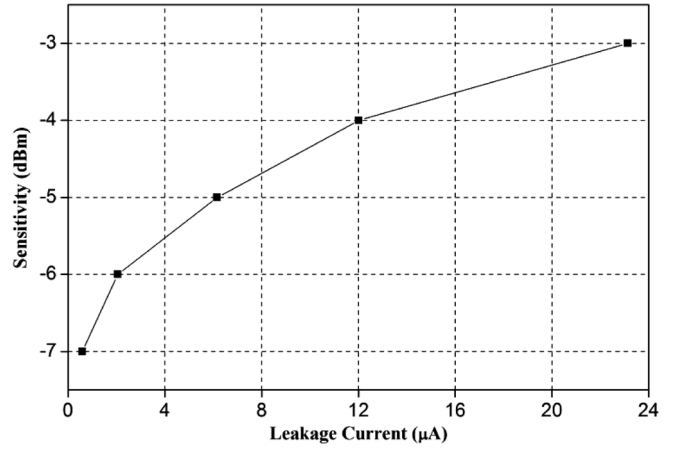Fig. 37. Measured IGR output power and efficiency at 53-GHz RF input.
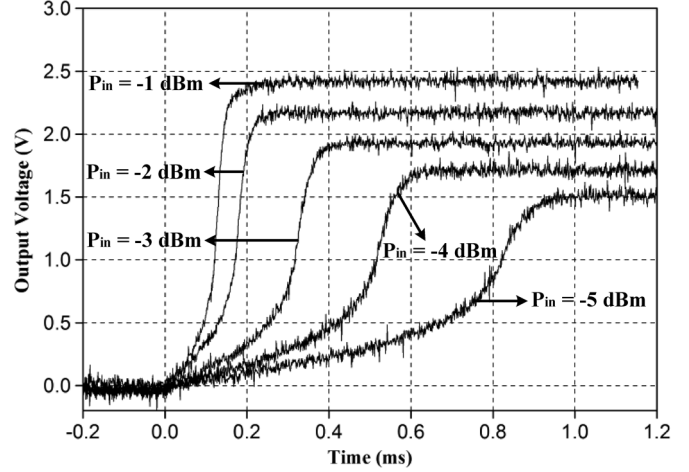


Fig. 38. Measured IGR sensitivity when the output voltage is 1.2 V at 53-GHz RF input.



Fig. 39. Transient voltage waveform measurements when charging a 610-pF $C_L$ at various input power levels.

the maximum sensitivity of the 10-kΩ load is at 2 dBm, these two values are not shown in Fig. 35. At 7-dBm input power, the IGR IC can provide an output power up to 1.035 mW with the maximum efficiency of 20.65%. This is realized at a 10-kΩ load. Note that, at 7-dBm input power, the low voltage $V_{out}$ cannot be sustained by the voltage source due to the fact that the output current feeding into the voltage source is too large. Thus, the measurement data for low $V_{out}$ is not included in Fig. 37.

The measurement setup using a voltage source also provides an additional benefit in terms of finding sensitivity for different load leakage current. Sensitivity of a rectifier is a function of both the required output voltage and the specified leakage current. To find out the relationship between the load leakage current versus input sensitivity at 1.2-V dc output voltage, the output current from the IGR can be recorded with various RF input power levels, as shown in Fig. 38. For example, it can be clearly seen that in order to achieve an output voltage of 1.2 V with 0.6-μA leakage current, the IGR needs a −7-dBm input power.

This IC is intended to be used in a millimeter-wave RFID tag with a 610-pF on-chip capacitor. To understand the transient performance when the IGR is driving this load capacitor, the output transient voltage waveform is recorded. From the measurement, it is found that less-than 1 ms is required to charge up the capacitor to steady state when the input power is greater than −5 dBm, as shown in Fig. 39. When the output voltage is smaller than 0.4 V, the supply voltage is too small to bias VR. This results in a slower charging slope in the initial charging period.

The only reliability issue for this IGR is that the IPVM can generate a large voltage swing, which may damage the gates of

TABLE II
SUMMARY OF THE MILLIMETER-WAVE RF-TO-DC RECTIFIER PERFORMANCE

|  | **This Work** | [23] | [21] |
|---|---|---|---|
| Technology | 65 $nm$ | 90 $nm$ | 65 $nm$ |
| Number of Stages | 7 | 10 | 3 |
| Operating Frequency | $46 - 56\ GHz$ | $45\ GHz$ | $70 - 72\ GHz$ |
| Peak Efficiency | 20.65% @7 $dBm$ | 0.5% @2 $dBm$ | 8% @5 $dBm$ |
| Input Sensitivity | $-7\ dBm$ @0.6 $\mu A$, 1.2 $V$ | 2 $dBm$ @700 $\mu A$, 0.9 $V$ | 5 $dBm$ @1.6 $V$ |

rectifying transistors. The maximally achievable input power is limited to 7 dBm by our measurement equipments, and no IGR gate breakdown is observed at this input power level. In the future, if a higher power level is required, a gate protection circuitry will be required at the IPVM output. In the system level, a high output voltage level from IGR might break other circuit blocks so an over-voltage protection circuitry will be necessary.

The center frequency of the implemented IC is shifted from 60 to 53 GHz in the measurement. In the prefabrication post-simulation, method of moments (MoM) capacitors are extracted at gate level and are not included in the electromagnetic (EM)

TABLE III
RELATIONSHIP BETWEEN $V_{\mathrm{GS}}$ VERSUS $V_{\mathrm{DS}}$ AND $V_{DD}$ IN A SINGLE-NMOS RECTIFIER

| Architecture | $V_{GS}$ as a function of $V_{DS}$ | Overdrive Voltage |
|---|---|---|
| Diode-Connected | $V_{GS} = V_{DS}$ | $V_{DS} - V_{th}$ |
| Internal Threshold Voltage Cancellation | $V_{GS} = V_{DS} + V_{ITC,BIAS}$<br>$V_{ITC,bias}$ is a function of $V_{DD}$ | $V_{DS} + V_{ITC,bias} - V_{th}$ |
| Active Diode | $V_{GS} = V_{DD}$ for $V_{DS} > 0$<br>$V_{GS} = 0$ for $V_{DS} < 0$ | $V_{DD} - V_S$ |
| Inductor Peaking | $V_{GS} = V_{DS} \times A_v \angle \theta$<br>$A_v$ is the passive voltage gain.<br>$\theta$ is the passive phase shift. | $V_{DD} - V_S \times A_v \angle \theta$ |
| In-Phase Gate-Boosting | $V_{GS} = A_v \cdot V_{DS} + V_{ITC,bias}$ | $A_v \cdot V_{DS} + V_{ITC,bias} - V_{th}$ |

simulations due to their excessive complexity. At this stage, a 3-GHz frequency drift is found. There will be parasitic coupling capacitors between the ac-coupling MoM capacitors and the IPVM transformer. These parasitic capacitors will reduce the center frequency by another 2 GHz. The MoM capacitors to adjacent internal wirings are also ignored, such as $V_{A,n}$ and $V_{B,n}$ in Fig. 22. This contributes to another 2 GHz of frequency drift.

The performance comparisons between this IC and related works are presented in Table II. Reference [23] implements a traditional rectifier without boosting the voltage swing. On the other hand, [21] applies an inductor-peaking method to boost the voltage swing so the peak efficiency is much higher than [23]. However, since the inductor-peaking method introduces no *in-phase* condition between $V_{\mathrm{DS}}$ and $V_{\mathrm{GS}}$, the efficiency and the sensitivity performance are limited. By applying the proposed IGR, which not only boosts the voltage swing, but also creates an *in-phase* condition, our IC achieves a state-of-the-art sensitivity, peak efficiency, and maximum output power in the category of millimeter-wave RF-to-dc rectifiers.

## IX. CONCLUSION

Any impedance conversion network that satisfies the IPVM criteria can be used to generate a large $V_{\mathrm{GS}}$ from the driving $V_{\mathrm{DS}}$ in a passive manner for the rectifying transistors. When the IPVM is used to form the IGR, the rectifier will achieve a lower forward resistance, lower reverse leakage current, and lower effective threshold voltage. Each of these properties will improve the sensitivity and PCE of the IGR. These properties are verified through several simulation comparisons. The relationship between $V_{\mathrm{GS}}$ and $V_{\mathrm{DS}}$ for several known single-transistor rectifiers is compared and summarized in Table III. The IGR architecture provides a large *in-phase* swing as the active-diode rectifier in a passive manner. One millimeter-wave IGR design is implemented in the 65-nm RF CMOS process and is experimentally verified. This design achieves a state-of-the-art 20% PCE with 7-dBm input power at 53-GHz center frequency. The IGR is an effective architecture to improve sensitivity and PCE in a high-frequency RF-to-dc rectifier. Though a larger $V_{\mathrm{GS}}$ can reduce the reliability of a MOSFET, no reliability issues are found at 7-dBm input power. Future studies should be made on the optimization of number of stages, device sizings, IPVM, VR circuits, which require smaller supply voltages, and gate–oxide protection circuitry. Efforts should also be made

to reduce the passive loss of the IPVM. The IGR can be implemented in a typical RF CMOS process without additional photo-mask. This allows integration of the IGR into a complete millimeter-wave-powered system with high sensitivity and PCE in the near future.

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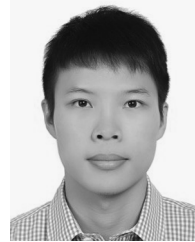
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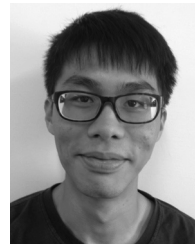
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