Effect of Annealing on Defect Elimination for High Mobility Amorphous Indium-Zinc-Tin-Oxide Thin-Film Transistor

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***Abstract*— This letter studies the correlation of postannealing treatment on the electrical performance of amorphous In-Zn-Sn-O thin-film transistor (a-IZTO TFT). The 400 °C annealed a-IZTO TFT exhibits a superior performance with field-effect mobility of 39.6 cm^2/Vs, threshold voltage (V_{th}) of −2.8 V, and subthreshold swing of 0.25 V/decade. Owing to the structural relaxation by 400 °C annealing, both trap states of a-IZTO film and the interface trap states at the a-IZTO/SiO_2 interface decrease to 2.16×10^{17} $cm^{-3}eV^{-1}$ and 4.38×10^{12} cm^{-2} eV^{-1}, respectively. The positive bias stability of 400 °C annealed a-IZTO TFTs is also effectively improved with a V_{th} shift of 0.92 V.**

***Index Terms*— In-Zn-Sn-O TFTs, high mobility TFTs.**

I. Introduction

IN RECENT years, thin film transistors (TFTs) using amorphous transparent oxide semiconductor (TAOS) have attracted a lot of attention as a backplane technology for large-sized liquid-crystal displays (LCDs). Amorphous indium-gallium-zinc oxide (a-IGZO), the most popular material proposed by H. Hosono et al. at 2004, has been widely developed according to its transparency, high mobility and better bias stability [1], [2]. The average field-effect mobility of TFT with sputter-deposited a-IGZO thin film as a channel layer is around 20 cm^2/Vs and it's not high enough (≧30 cm^2/Vs) for future display applications such as ultra-high definition (UHD) display, active matrix organic light-emitting diode displays (AMOLEDs) and system driving circuits integrated with the TFT array process [3], [4]. Compared with other amorphous oxide semiconductor materials, amorphous indium-zinc-tin oxide (a-IZTO) is promising candidate for achieving high mobility oxide TFTs. The electron transport through extensive s-orbital overlap between metal elements of In and Sn can render excellent conductivity path due to the isotropic connection with other cations even in amorphous state. Some of the previous studies have demonstrated the a-IZTO TFTs with the mobility higher than 30 cm^2/Vs [5], [6]. However, few details were reported regarding the electrical performance and further electrical improvement in a-IZTO TFTs.

In this study, we investigate the electrical performance and reliability of a-IZTO TFT device by thermal annealing process. The effect of thermal annealing on the reduction of bulk trap states in a-IZTO thin film and the interface trap states between silicon dioxide and a-IZTO thin film is also discussed in detail.

II. Device Fabrication

The inverted-staggered a-IZTO TFT devices were fabricated for this study. A 100-nm-thick thermal oxide was first grown on an RCA-cleaned n+ heavily doped silicon substrates in a horizontal thermal furnace as the gate insulator layer. Then, the 10-nm-thick a-IZTO channel layers were deposited by using RF magnetron sputtering with power 70 W using IZTO target of In:Sn:Zn:O = 4:4:1:15 at.%. The argon and oxygen flow rate during the sputtering is 10 sccm and 0.1 sccm, respectively. The source and drain electrodes of 100-nm-thick ITO were formed by RF magnetron sputtering. Finally, these samples were annealed sequentially using 200 °C, 300 °C and 400 °C for half hour in a thermal furnace with nitrogen flow rate of 80 sccm. All the thin films were patterned by shadow masks. The electrical properties were measured using Keithley SCS 4200 semiconductor parameter analyzer in the dark chamber at room temperature. The 30-nm-thick a-IZTO thin films were deposited on the glass substrate and then annealed at different temperatures to analyze the film structure by using X-ray diffractometer (XRD).

III. Results and Discussion

Figure 1 shows XRD spectrum of IZTO thin films on glass substrate with and without post-annealing treatment. The rough peak at 22 °C is the signal of glass substrate, which is not relative to the IZTO thin film. No any sharp peaks was observed in the spectra, indicating that the IZTO thin film is originally amorphous type whatever it was the as-deposited or even post-annealed at 400 °C. The curves of drain current (I_D) versus gate voltage (V_G) of a-IZTO TFT

Manuscript received May 29, 2014; revised August 5, 2014 and August 27, 2014; accepted August 29, 2014. Date of publication September 16, 2014; date of current version October 21, 2014. This work was supported by the Ministry of Science and Technology, Taiwan, under Contract 100-2628-E-009-016-MY3 and Contract 103-2221-E-009-010-MY3. The review of this letter was arranged by Editor W. S. Wong.

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Digital Object Identifier 10.1109/LED.2014.2354598

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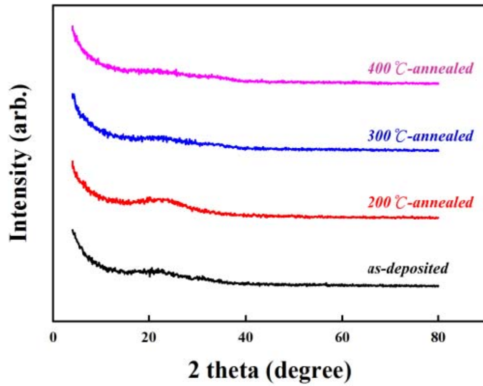

Fig. 1. XRD spectrum of IZTO thin films on glass substrate after annealing processes at 200 °C, 300 °C and 400 °C, respectively.

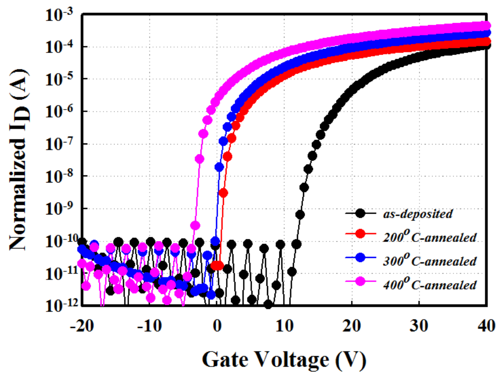

Fig. 2. Transfer characteristics of a-IZTO TFT devices operated in saturation region (V_D = 10 V). The features include the as-deposit, 200 °C, 300 °C and 400 °C-annealed a-IZTO TFTs.

before and after thermal annealing at 200 °C, 300 °C and 400 °C for half hour are shown in Fig. 2. The field effect mobility (μ_{EF}) was 10.3 cm^2/Vs, 18.7 cm^2/Vs, 27.19 cm^2/Vs and 39.6 cm^2/Vs for the as-deposited, 200 °C-annealed, 300 °C-annealed and 400 °C-annealed ones, respectively. These values of mobility are much higher than the a-IGZO TFTs with similar process conditions in the previous research documents [7], [8]. Also, the V_{th} and sub-threshold swing ($s.s.$) decreased from 12 V to −2.8 V and 1.05 V/decade to 0.25 V/decade, respectively, as the annealing temperatures increase. This performance enhancement of TFT devices was not caused by the crystallization of IZTO channel layer, which has been revealed from Fig. 1. It could be attributed to the reduction in subgap defects of a-IZTO thin film during thermal annealing below 400 °C, due to the structural relaxation mechanism [9]. This phenomenon explains that the mobility and sub-threshold of a-IZTO TFT can be improved after thermal annealing. The electrons can more easily transport in a-IZTO channel layer due to fewer subgap states and interface traps at the interface between the channel layer and gate insulator. Compared with the as-deposited condition, the negative V_{th} shift of a-IZTO TFT device after annealing process could be caused by the formation of high concentration of electrons in the a-IZTO thin film.

In order to calculate the accurate value of trap states (N_t) and the interface states (D_{it}), the following formula of

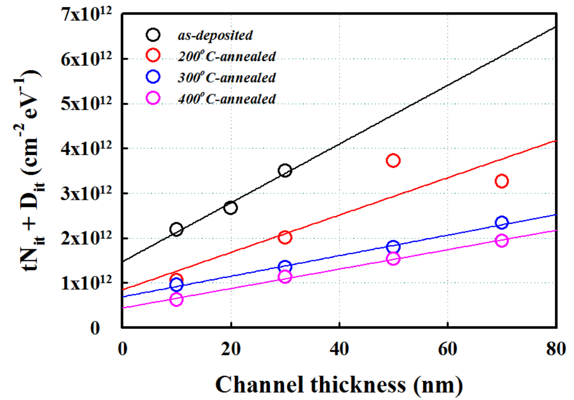

Fig. 3. The relation of $D_{it} + tN_t$ versus different a-IZTO channel thickness ranging from 10 nm to 70 nm. The symbols represent the experimental data, while the lines are the simulation fitting to equation (1). N_t and D_{it} can be calculated from the slope and the intercept value with y-axis of the fitting line, respectively.

sub-threshold swing can be used [10]:

$$s.s. = Log_e 10 \cdot \frac{k_B T}{e} \cdot [1 + \frac{e(D_{it} + tN_t)}{C_{ox}}] \quad (1)$$

where e is the elementary electric charge, k_B the Boltzmann constant, T the temperature, t the channel thickness and C_{ox} the gate insulator capacitance per unit area. N_t is the volume density of the shallow traps in the a-IZTO channel layer and D_{it} is the area density of the interface traps at the a-IZTO/SiO_2 interface. As for different annealing temperatures, the values of $D_{it} + tN_t$ associated with fitting curves are shown in Fig. 3 as the channel thicknesses range from 10 nm to 70 nm. These fitting curves are plotted according to eq. (1), where N_t and D_{it} could be estimated from the slope and the intercept value with y-axis of the fitting line, respectively. The value of N_t was 8.9 $\times 10^{17}$ cm^{-3}eV^{-1} for the a-IZTO TFT without any annealing, while it is significantly decreased to 4.16 $\times$ 10^{17} cm^{-3}eV^{-1}, 2.29 $\times$ 10^{17} cm^{-3}eV^{-1} and 2.16 $\times$ 10^{17} cm^{-3}eV^{-1} for the annealing at 200 °C, 300 °C and 400 °C, respectively. The higher annealing temperature could actually fix and reduce some of the defects in the a-IZTO thin film. This result also accorded with the observation that electrical performance of a-IZTO TFT device is promoted after high temperature annealing. Furthermore, the D_{it} can also be improved from the post annealing treatment at the same time. The value of D_{it} is decreased from 2.71 $\times$ 10^{12} cm^{-2}eV^{-1} to 8.46 $\times$ 10^{11} cm^{-2}eV^{-1}, 6.8 $\times$ 10^{11} cm^{-2}eV^{-1} and 4.38 $\times$ 10^{12} cm^{-2}eV^{-1} for the 200 °C, 300 °C and 400 °C annealed TFT devices, respectively.

Figure 4 shows the positive bias stability test of a-IZTO TFTs with 15 V gate voltage for 1000 sec. This experiment was performed at a vacuum measurement chamber to dismiss from the influence of oxygen or moisture in the environment. The V_{th} shifts were fitted by the stretched-exponential equation as following [11]:

$$\Delta V_{th} = V_o\{1 - \exp[-(\frac{t}{\tau})^{\beta}]\} \quad (2)$$

where the V_o is the V_{th} shift at infinite time, β is stretched exponential exponent, τ is the characteristic trapping time

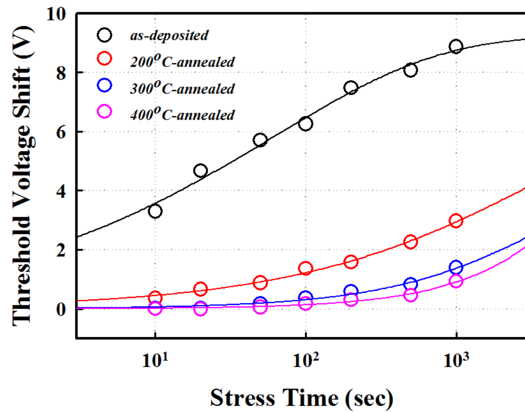

Fig. 4. Threshold voltage shift of a-IZTO TFTs with different annealing temperatures as a function of gate bias stress durations. The electric field of gate bias stress was fixed at 1.5 MV/cm (Vgate = 15 V). The symbols represent the experimental data, while lines are the simulation fitting to stretched-exponential model.

of carriers. The fine fitting of the V_{th} shift indicated the mechanism of bias stability was due to charge trapping at the a-IZTO/SiO_2 interface or gate dielectric. The last could be eliminated according to the high quality thermal oxide in this experiment. The τ fitted from the model of as-deposited TFTs was 61 s, and increased to 3.13×10^3 s, 3.55×10^3 s and 2.9×10^4 s after the annealing at 200 °C, 300 °C and 400 °C, respectively. The result of prolonged trapping time of carriers revealed that the charge could hardly trap at the interface with fewer defect states which were effectively reduced by post-annealing treatment. The extracted values of D_{it} of a-IZTO TFT with different channel thickness were consistent with the result of positive bias stability test.

IV. Conclusion

In this letter, we have studied the evolution of trap states during thermal annealing process for the high carrier mobility a-IZTO TFT device. The thermal annealing process provides the energy for structure relaxation of a-IZTO thin film, which obviously reduces both defect states in the a-IZTO channel and at the a-IZTO/SiO_2 interface. The numerical calculation extracted from the sub-threshold swing was used to evaluate the trap states in this work. The τ values obtained from the bias-stressed TFT by fitting the stretched-exponential model indicated the thermal annealing at 400 °C can exhibit the highest effectiveness to reduce the a-IZTO/SiO_2 interface states. Based on the proposed information, the evolution of defect elimination during thermal annealing process can be quantified and applied for the a-IZTO TFT technology. By comparing these results with our previous study on a-IGZO thin film, the a-IZTO TFT is highly promising for achieving the requested characteristics of high carrier mobility and operation reliability for the applications of next-generation flat panel displays.

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