Submicron Cu/Sn Bonding Technology With Transient Ni Diffusion Buffer Layer for 3DIC Application

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***Abstract*— A submicron Cu/Sn bonding with transient Ni buffer layer at 225 °C is demonstrated to overcome current 5-μm Cu/Sn physical limitation. The 10-nm Ni layer suppresses immense Cu/Sn interdiffusion during heating step prior to major bonding process. When the temperature is close to the Sn melting point, the Ni layer dissolves and molten Sn gives successful submicrometer Cu/Sn bonding. The excellent mechanical strength and electrical performance of this scheme show the great potential for future and highly dense 3D interconnects.**

***Index Terms*— 3D integration, Cu/Sn bonding, transient Ni buffer layer.**

I. Introduction

Due to classical physics transport limitation and expensive extreme ultraviolet (EUV) lithography instrument, 3D integration has been widely recognized as a mainstream technology for next generation of Si fabrication [1]–[3]. Among 3D interconnects, thousands of 10-μm diameter Cu TSV and fine pitch Cu pillar (Sn bump) pairs in a 100-μm depth Si interposer are demonstrated to improve a wider bandwidth multi-function and large pin-out chip [4], [5]. However, current Cu pillars pitch larger than 20-μm cannot satisfy increasing CMOS device density [6], [7]. Although highly dense pairs of TSV and bump are required to realize vertical interconnection, there is still no clear solution to achieve the bump miniaturization. For example Cu-Cu bonding shows a great potential for 3D application. However, a clean pre-bonding Cu surface and >300 °C bonding temperature are usually required. High cost and low yield are the bottleneck of this approach [8], [9]. Instead of Cu solid metal bonding (SMB), Cu pillar Sn bump using solid liquid interdiffusion (SLID) or transient liquid phase (TLP) bonding is a mature technology with strong benefits of wider roughness tolerance, less bonding duration and low fabrication cost in Si packaging [10]–[13]. However currently $\sim$2.5-μm minimum thickness of Cu_6Sn_5 η-IMC after one reflow in [14] and [15] is reported to form on one side, meaning that Cu pillar Sn bump will face the bottleneck when total bump thickness is smaller than 5-μm. This is because the stiff and rough η-phase Cu_6Sn_5 IMC formation gives rise to a poor solid metal contact in the following major bonding steps after Sn consumption.

In this letter, a novel submicron Cu/Sn bonding technology is proposed and developed to break current Cu/Sn physical limitation. With the transient existence of 10-nm Ni buffer layer, the suppression of Cu/Sn inter-diffusion rate during heating step enhances the mechanical strength significantly after bonding process. With good electrical and reliability results, submicron Cu/Sn technology enables dense vertical interconnects for 3D integration applications.

II. Evaluation of Cu/Sn Bonding and Pull Test Results

300-nm Cu film, optional 10-nm Ni buffer layer, and 400-nm Sn film are deposited sequentially on silicon wafers with 300-nm layer of silicon oxide. Symmetric Cu/Sn wafers without surface pre-treatment are bonded facetoface at 225-300 °C with a pressure of 1.26 MPa (183 psi). In addition to electrical and reliability tests, the bonded wafers are inspected by SAT SEM, AES for quality analysis and pull test for mechanical strength evaluation.

The cross-sectional SEM image in Fig. 1(a) shows a perfect 1.31-μm thick Cu/Sn bonded structure without visible bonding interface. Fig. 1(b) shows the pull test diagram of the 2.25 cm^2 bonded Cu/Sn chip with a 10-nm Ni buffer layer and the sample remains intact after being tested. As illustrated in Table I, both sample 1 and 2 (below and above $T_{m(Sn)} = 231.9$ °C) with 10-nm Ni have great enhancement on mechanical properties. In the contrast, the sample 3 and 4 without Ni buffer layer failed during sample preparation before test although the process temperature was increased to 300 °C.

In order to evaluate the Ni buffer layer effect on binary Cu/Sn inter-diffusion distribution at the moment right before the major bonding step, two complete Cu/Sn bonded wafers, with and without 10-nm Ni buffer, are inspected by SAT, as shown in Fig. 2(a) and (b). In addition, 300/400-nm thick

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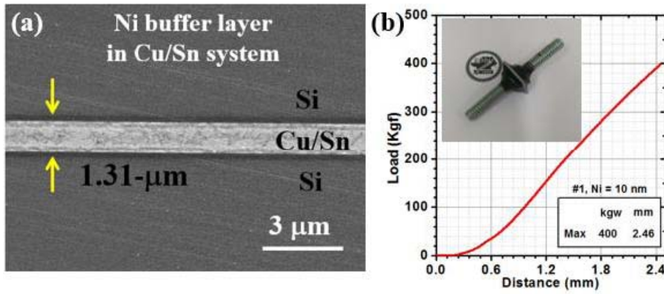

Fig. 1. (a) Cross-sectional SEM image and (b) pull test diagram of the 1.5 × 1.5 cm^2 chip based on 300/400-nm-thick Cu/Sn pad bonding with 10-nm Ni buffer layer after 225 °C bonding.

TABLE I
BONDING STRENGTH TEST RESULTS AFTER THREE BONDING TEMPERATURES WITH AND WITHOUT Ni 10 nm BUFFER LAYER IN Cu/Sn SYSTEM

	Cu/Sn System (300/400 nm)	*Process Temperature*	*Bonding Strength Test*	*Failure Location*
1	**with 10-nm Ni**	225 °C	Exceeding 400 Kgf	Not failure
2	**with 10-nm Ni**	250 °C	229.3 Kgf	Si/glue
3	**w/o 10-nm Ni**	250 °C	De-bond	IMC/IMC
4	**w/o 10-nm Ni**	300 °C	De-bond	IMC/IMC

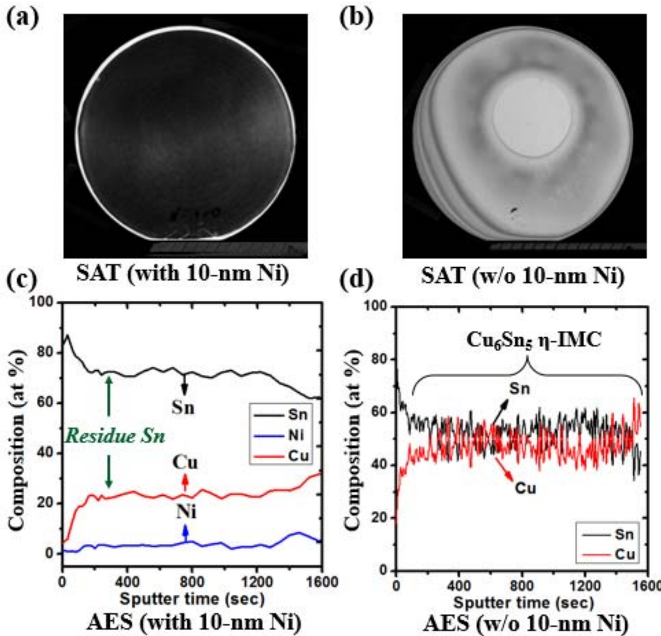

Fig. 2. Scanning acoustic tomography images of Cu/Sn wafer bonding (a) with Ni and (b) without Ni buffer layer. Auger depth profiles of Cu/Sn wafer bonding (c) with Ni and (d) without Ni buffer layer.

Cu/Sn samples with and without Ni layer were annealed at 250 °C for 1 min with a heating rate of 2 °C/sec to simulate the bonding procedure. Corresponding AES results are shown in Fig. 2(c) and (d). Based on the evidences of Auger depth profile, Cu_6Sn_5 η-IMC product in Cu/Sn system forms around whole chip surface right after heating step, resulting in rough surface and even bonding failure, as shown in Fig. 2(d).

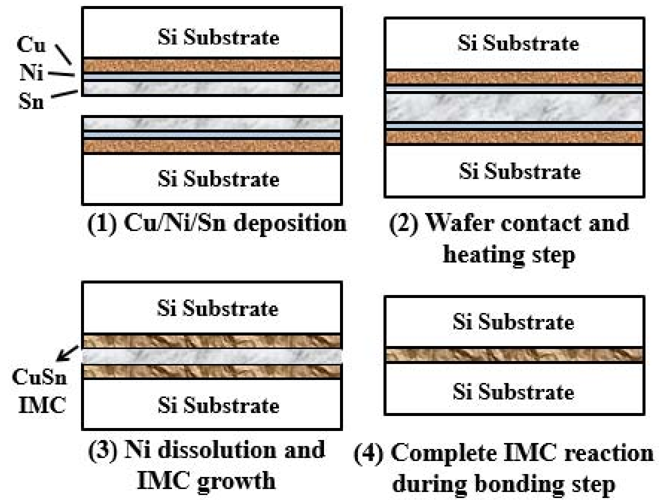

Fig. 3. Schematic diagram of Cu/Sn bonding with Ni buffer layer.

In contrast, for the sample with 10nm Ni in between Cu/Sn, more than half residue Sn composition is observed at the surface, as shown in Fig. 2(c).

III. PROCEDURE OF BONDING PROCESS

With the excellent bonding quality by the contribution of Ni behavior, submicron Cu/Sn bonding could be one of the most suitable interconnect technologies with TSVs for next generation of 3D interconnection. Figure 3 shows the schematic diagram of Cu/Sn bonding procedure. Since an ultra-thin Ni layer reduces three orders of magnitude of Cu and Sn atoms interdiffusion [10], [16], the pure Sn atoms remain at the original bonding interface during heating process. However, when the temperature is heated up close to Sn melting point, transient Ni buffer will dissolve towards Sn. In other words, Cu and Sn start to vigorously inter-diffuse and form IMC in a very short time right after Ni buffer layer vanishing, as shown in Fig. 3(c). Finally, both sides of quasi molten Sn provide the TLP process and give a complete wafer bonding result.

IV. ELECTRICAL PERFORMANCE AND QUALITY INVESTIGATION

Electrical performance and reliability investigations of bonded structures using this novel submicron Cu/Sn bonding are evaluated by Kelvin structure with a 10×10 μm^2 contact area. Fig. 4 shows the schematic of Kelvin test structure and corresponding measurement results. A specific contact resistance (R_{sc}) of $\sim 15 \times 10^{-8}$ Ω-cm^2 between the sweeping current from 0 to 100 mA indicates a good bonding interface quality for 3D integration [9]. Next, the bonded samples are tested with 100 hours under 200 mA DC current stressing, 500's TCT (−55 to 125 °C), and 96 hours un-bias HAST (85 % RH, 130 °C) to investigate the feasibility of applying this scheme in actual 3D integration process. Fig. 5(a) shows that only 7.8% and 6.9% R_{sc} reduction of 250 and 225 °C bonded samples after 100 hr DC current stressing, indicating the remaining bonding interface are further removed during

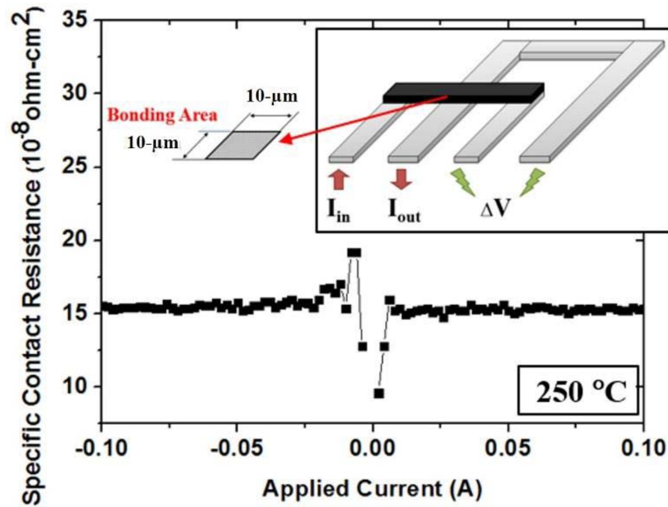

Fig. 4. Specific contact resistance of the sample bonded at 250 °C.

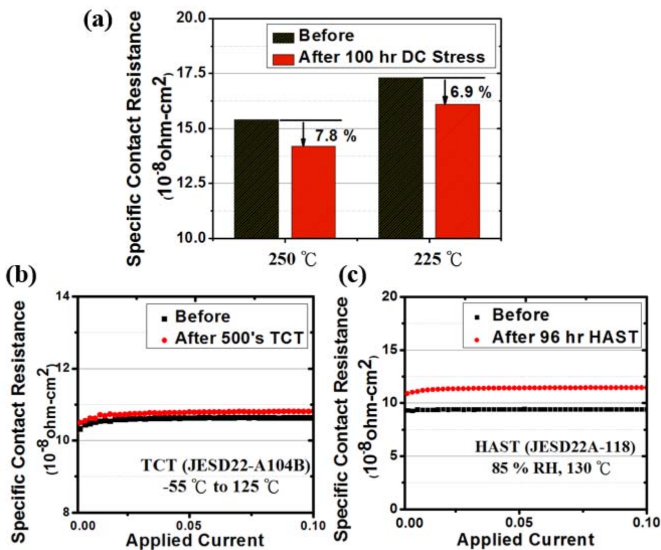

Fig. 5. Specific contact resistances of samples before and after (a) 200 mA DC current stressing bonded at 225 °C and 250 °C, (b) 500's TCT (JESD-A104B, −55 to 125 °C), and (c) 96 hour un-bias HAST (JESD22A-118B, 85% RH at 130 °C).

current stressing, which has been observed in the previous study [17]. Fig. 5(b) show the novel Cu/Sn structure qualifies 500's TCT even with a slight resistance reduction. After 96 hours un-bias HAST, as shown in Fig. 5(c), the resistance is kept around the same value. The slight resistance increase can be improved by guard ring and hybrid bonding [17]. The successful submicron Cu/Sn bonding using Ni transient layer shows good electrical mechanical and reliable properties, demonstrating the feasibility of next generation interconnect.

V. Conclusion

A novel submicron Cu/Sn bonding technology is successfully demonstrated, breaking current Cu/Sn physical limitation. By the insertion of transient 10-nm Ni buffer layer, Cu/Sn inter-diffusion during heating step is suppressed. Robust bond strength and reliable electrical property can be achieved, showing the feasibility in future 3D interconnect applications.

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