# A 13.56 MHz 40 mW CMOS High-Efficiency Inductive Link Power Supply Utilizing On-Chip Delay-Compensated Voltage Doubler Rectifier and Multiple LDOs for Implantable Medical Devices

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***Abstract*—In this paper, a 13.56 MHz CMOS near-field inductive link power supply (ILPS) that can deliver 20 mA output current for implantable medical devices (IMDs) is proposed and fabricated. In the proposed ILPS, the pair of inductive link coils is constructed in the spiral shape with a ferrite core to save space and increase efficiency. Experimental results have shown that the near-field coils can transmit power at the resonant frequency of 13.56 MHz with the transmission efficiency up to 76.3%. The CMOS power regulator is composed of active voltage doubler rectifier (VD) and low-dropout regulators (LDOs). In the active VD with the comparator, the input offset voltage is adjustable for delay compensation and a start-up control circuit is added to achieve robust start-up mechanism. On-chip delay compensation control with SR-latches is proposed to prevent from error glitch switching on offset voltage control and achieve accurate delay compensation so that the reverse current conduction can be avoided and the efficiency can be increased. Three fully-integrated LDOs with rectifier output voltage of 2 V to 1.8 V are realized for analog (ALDO), digital (DLDO), and reference-voltage (RLDO) circuits. Thus the performance of individual LDO can be optimized. The measured output ripple voltage of the active VD is 10.4 mV. The power conversion efficiency (PCE) is 85% under 20 mA output current. The measured dropout voltage is 384 mV. As compared with other designs, the proposed ILPS has lower ripple voltages, lower dropout voltage, and higher PCE.**

***Index Terms*—Active voltage doubler rectifier, fully-integrated LDOs, implantable medical devices, inductive link power supply, 13.56 MHz ISM band.**

## I. Introduction

In RECENT years, implantable medical devices (IMDs) have become more and more important in the treatment of intractable diseases or disorders, especially neurological ones. Such neural prosthetic IMDs utilize electrical pulses to stimulate neural cells and restore neural functions. Several examples are cochlear implants [1], retinal prostheses [2], and closed-loop epilepsy control [3]. These IMDs usually have high power consumption greater than several mWs. Since they are implanted into the human body, a long-term reliable power supply is required to avoid the frequent surgery for the battery replacement. However, current battery technology cannot sustain for an enough long time. Therefore wireless power transfer can be a useful solution for IMDs [4]. The near-field inductive energy transfer has become the most widely used method for the neural prosthetic IMDs to recharge the chargeable battery or directly provide the required power from medium to high levels [1]–[3].

A near-field inductive link power supply (ILPS) can be divided into three different parts as: power amplifier, near-field coils, and power regulator. The power amplifier amplifies the RF signal to drive the near-field coils. The near-field coils transmit the RF signal through the skin. In the design of near-field coils, the coil size which could be confined by the physical sizes of IMDs, is an important design factor that mainly determines both power conversion efficiency (PCE) and maximum transmission distance. The power regulator which converts the received signal into DC voltage to supply the IMD, consists of low-dropout regulators (LDOs) and active rectifier or passive rectifier [5]. In the reported CMOS ILPSs [3], [6]–[11], active rectifiers with power MOS devices, comparators and control circuits are adopted to convert AC power into DC power. Since the power MOS devices has both turn-on and turn-off delay times, the comparators should accurately control switch timing to obtain proper forward current conduction and avoid reverse current conduction. Thus the efficiency can be increased. Several techniques have been proposed for the delay compensation [3], [7]–[11]. In [7], the negative feedback control is used to compensate only the turn-off delay. But the PCE is degraded obviously with the increased output loading. The active rectifier using offset-controlled high speed comparators was proposed in [8], where both turn-on delay and turn-off delay are compensated by using off-chip control signals. Such off-chip control signals are not feasible for IMDs.

It is known that the input voltage of a full-wave active rectifier must be larger than its output DC voltage. As compared with that of a full-wave active rectifier, the input voltage of an active

Manuscript received January 25, 2014; revised May 07, 2014 and July 27, 2014; accepted August 15, 2014. Date of publication September 29, 2014; date of current version October 24, 2014. This paper was approved by Guest Editor Zhihua Wang. This work was supported in part by the Ministry of Science and Technology (MOST), R.O.C., under project MOST 103-2220-E-009-006, MOST 103-2220-E-009-001, and in part by the "Aim for the Top University Plan" under Biomedical Electronics Translation Research Center of National Chiao Tung University and Ministry of Education, Taiwan, R.O.C.

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Digital Object Identifier 10.1109/JSSC.2014.2356459

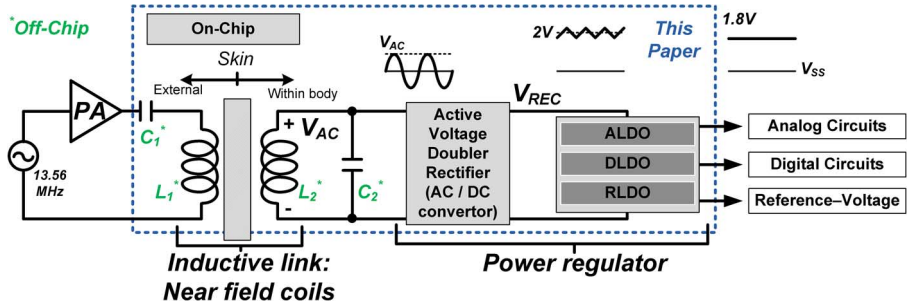



Fig. 1. The block diagram of the proposed ILPS.

voltage doubler rectifier (VD) can be lower than its output DC voltage, leading to more reliable operation in the weakly coupled inductive link environment. Active VDs using offset-controlled comparators were proposed in [9], [10], where turn-on and turn-off delay compensation requires off-chip control signals. Moreover, their dropout voltages are large. In [11], the zero-crossing-point (ZCP) prediction (or phase-lead method) is proposed to compensate the switching delay in active rectifiers without comparators. Since it doesn't have comparators to control power transistors, a delay unit is needed to provide accurate timing. The measured power efficiency is 82% at 400 Ω output loading and 41 mW output power.

The LDO provides a stable power supply for the system-on-chip (SoC). The SoC chip typically consists of analog front-end circuits, digital circuits, and SAR ADC with a reference voltage. It is found that a single LDO is difficult to satisfy the different performance requirements of analog, digital, and reference-voltage circuits. Moreover, the number of off-chip components such as capacitors and resistors should be restricted in IMDs. Thus, high performance fully-integrated LDOs with low power dissipation and small chip area are required.

In the IMD implanted into human brain for epilepsy detection and stimulation [3], the near-field ILPS is the best choice. In this paper, a CMOS ILPS is proposed and fabricated in 0.18 $\mu$m CMOS process technology to supply the voltage of the SoC in the above IMD [12]. The proposed ILPS is operated at the industrial, scientific, and medical (ISM) band (13.56 MHz) and capable of delivering 20 mA output current. An active VD with fully on-chip delay-compensated comparators and peaking current source is designed to avoid the use of external control signals. The peaking current source is used to decrease the supply voltage dependence of bias current [13]. The signal voltage received by the receiver coil is 1.192 V. The dropout voltage of active VD is 384 mV with the voltage conversion ratio of 1.67. The measured PCE of active VD is 85% at 40 mW output power on 100 Ω load.

In the proposed ILPS, the fully-integrated multiple LDOs are used to generate stable 1.8 V output voltage for analog (ALDO), digital (DLDO), and reference-voltage (RLDO) circuits. Therefore, the performance of individual LDO can be optimized and the output cross talk from DLDO can be isolated. The measured ripple voltages of active VD, ALDO, DLDO, and RLDO output are 10.4 mV, 5.9 mV, 72.4 mV, and 1.5 mV, respectively. The measured PCE of the power regulator is 74.8% under 20 mA output current.

This paper is organized as follows. In Section II, the system architecture and circuit design of the proposed ILPS are described. The experimental results are shown in Section III. Finally, the conclusion is given in Section IV.

## II. System Architecture and Circuit Design

### A. System Architecture

Fig. 1 shows the block diagram of the proposed ILPS which is composed of the coils for power transmission, active VD, and fully-integrated multiple LDOs. The active VD is used to obtain the required DC voltage with less AC voltage so that the inductive magnetic energy through body tissue can be reduced to avoid the risk of tissue damage. Finally, the LDO is used to regulate the unregulated DC voltage from the active VD into a stable voltage for the IMD.

To determine the specifications of ILPS, the maximum current loading of each sub-block of the SoC for epilepsy detection and stimulation must be considered. The sub-blocks of SoC include analog front-end amplifiers (AFEA), SAR ADC, biosignal processor (BSP), MedRadio-band transceiver, and stimulator [3]. Depending on the circuit operation, the sub-blocks are further divided into analog, digital (sample-data), and reference. Then their maximum transient loading currents of 0.56 mA, 17.2 mA, and 1 mA are obtained in analog, digital, and reference circuits, respectively. The total transient loading current is 18.76 mA. Therefore, the maximum driving current capability of the proposed ILPS is designed to be 20 mA. The maximum driving current capabilities of the proposed ALDO, DLDO, and RLDO are 5 mA, 20 mA, and 1.5 mA, respectively.

### B. Near-Field Coil Design

Since the coil structure affects quality (Q) factor, coupling coefficient (k), and inductance, it must been carefully chosen to suit the implanted devices [14]–[16]. For the seizure control IMD [3], spiral coils are chosen for inductive link. The implant size cannot exceed 2.5 cm in diameter and transmission distance is about 1 cm. The cylindrical ferrite cores are placed into the coil center to increase the Q factor. The use of ferrite core as a magnet has been used in cochlear implant device [1] and proved its feasibility.

Under these conditions, both Tx and Rx are designed. The design and simulation procedure is described below.

Firstly, the outer (inner) diameter of the implanted Rx coil is chosen as 2.2 cm (2 cm) with 2 turns of AWG 25 wires. Then the number of turns and the radius of Tx coil are determined through

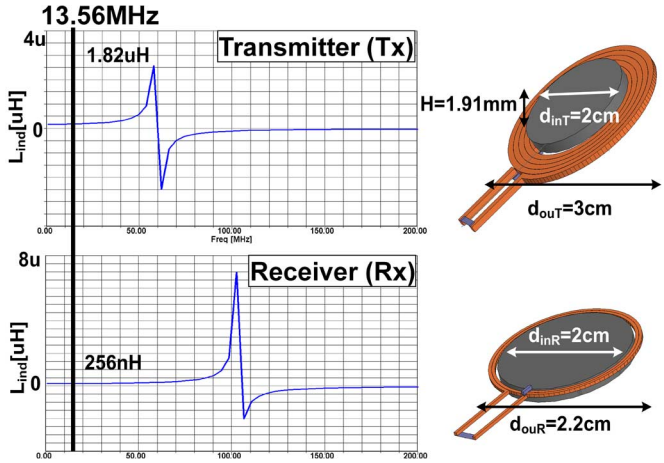



Fig. 2. HFSS simulation results on inductances of the Tx and Rx coils with ferrite cores. The coil sizes are also given, where H is height of ferrite core.

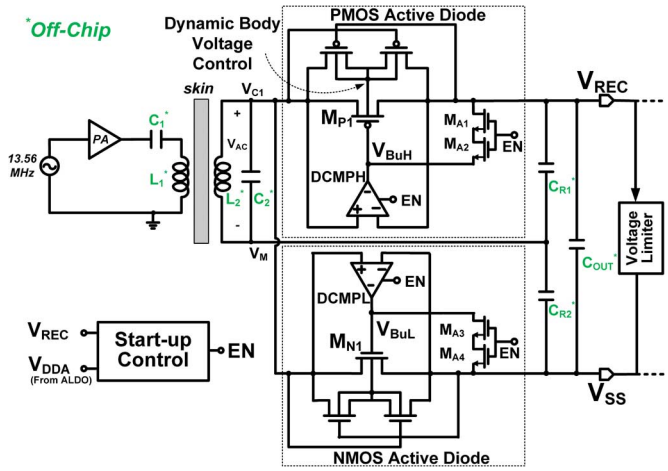



Fig. 3. The circuit structure of VD.

the HFSS simulation to achieve the maximum coupling coefficient and transmission efficiency. The outer (inner) diameter of Tx coil is determined as 3 cm (2 cm) with 5 turns of AWG 18 wires. Finally, the coil inductances are simulated.

Fig. 2 shows the HFSS simulation results on inductances of Tx and Rx coils with ferrite cores. Below the self-resonant frequency, the inductance of Rx coil is 256 nH at 13.56 MHz whereas that of Tx coil is 1.82 $\mu$H. The electric behavior of coil is like that of a capacitor showing negative inductance when the frequency is greater than self-resonant frequency.

### *C. Active Voltage Doubler Rectifier (VD)*

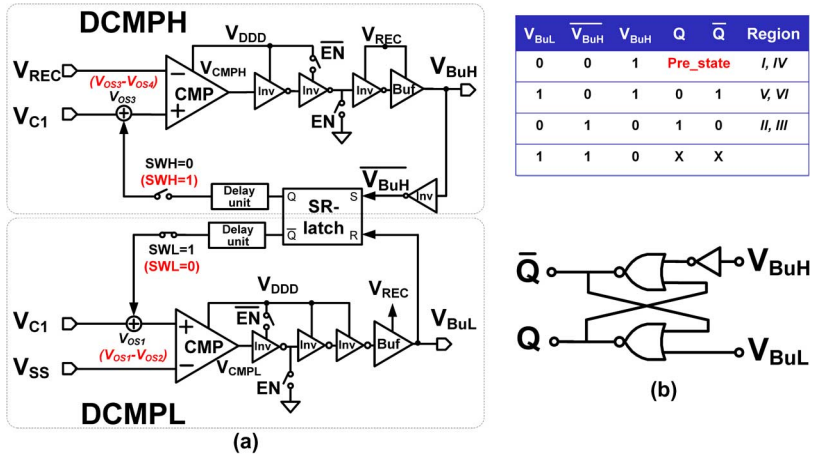
The circuit structure of the active VD is shown in Fig. 3, which consists of NMOS active diode, PMOS active diode, start-up control, two symmetrical delay-compensated comparators (DCMPH and DCMPL) with delay compensation control, dynamic body voltage control circuits, voltage limiter, and off-chip filtering capacitors $\mathrm{C_{R1}}$, $\mathrm{C_{R2}}$, and $\mathrm{C_{OUT}}$, which are 0.1 $\mu$F SMD capacitors. In Fig. 3, $\mathrm{C_1}$ (89 pF) and $\mathrm{C_2}$ (520 pF) are used to make the resonant frequency at 13.56 MHz. The voltage limiter limits the output voltage $\mathrm{V_{REC}}$ of active VD to a maximum value of 2.5 V (nominal value of 2 V) in case the input power of the active VD is too large. The dynamic body voltage control circuit with two auxiliary transistors is used to automatically connect the body of power MOS device to the suitable potential so that both body-effect and substrate leakage of power MOS device can be eliminated. For example, the p-type dynamic body voltage control circuit connects the body of power transistor $\mathrm{M_{P1}}$ to the highest voltage between the input and output voltages. Similarly, the body of power transistor $\mathrm{M_{N1}}$ can be connected to the lowest voltage dynamically by n-type dynamic body voltage control circuit.

Since the large power transistors $\mathrm{M_{P1}}$ and $\mathrm{M_{N1}}$ in Fig. 3 have larger parasitic capacitances, their turn-on delay and turn-off delay when driven by the output voltages $\mathrm{V_{BuH}}$ and $\mathrm{V_{BuL}}$ of the delay-compensated comparators DCMPH and DCMPL, reduce the conduction time and induce the reverse current. Thus the delays have to be compensated by DCMPH and DCMPL. The detailed structures of DCMPH and DCMPL are shown in Fig. 4(a). As can be seen from Fig. 4(a), the delay-compensated comparator DCMPH (DCMPL) consists of a delay compensation control path, a comparator CMP, three inverters, and a buffer to generate the output voltages $\mathrm{V_{BuH}}$ ($\mathrm{V_{BuL}}$). The output voltages $\mathrm{V_{BuH}}$ and $\mathrm{V_{BuL}}$ are connected to the delay compensation control path formed by a SR-latch and a delay unit to dynamically generate suitable offset voltages to compensate both turn-on and turn-off delay times. They are powered from DLDO output voltage ($\mathrm{V_{DDD}}$). The structure and the operation table of the SR-latch is shown in Fig. 4(b). The use of SR-latch can prevent from the error offset voltage switching due to the noise of input voltage in the comparators. Thus accurate delay compensation can be achieved. The delay unit is used to provide a suitable delay to accurately control the offset switching for exact delay compensation. In Fig. 4(a), when the switch $\mathrm{SWH} = 0$ ($\mathrm{SWL} = 1$), the positive offset voltage $\mathrm{V_{OS3}}$ ($\mathrm{V_{OS1}}$) is generated at the input of the comparator CMP in DCMPH (DCMPL). When the switch $\mathrm{SWH} = 1$ ($\mathrm{SWL} = 0$), the negative offset voltage $\mathrm{V_{OS3}} - \mathrm{V_{OS4}}$ ($\mathrm{V_{OS1}} - \mathrm{V_{OS2}}$), where $\mathrm{V_{OS3}} < \mathrm{V_{OS4}}$ ($\mathrm{V_{OS1}} < \mathrm{V_{OS2}}$), is generated at the input of the comparator in DCMPH (DCMPL). The generation of these offset voltages will be explained later with the comparator circuit.

In Fig. 5, the steady state operational waveforms of DCMPH and DCMPL in Figs. 3 and 4 is described in the following.

***Region I***: $\mathrm{V_{C1}} + \mathrm{V_{OS3}} < \mathrm{V_{REC}}$, $\mathrm{V_{C1}} + \mathrm{V_{OS1}} > \mathrm{V_{SS}}$. In this region, the output voltage $\mathrm{V_{BuH}}$ of DCMPH is at high level whereas $\mathrm{V_{BuL}}$ of DCMPL is at low level. As may be seen from Fig. 3, the power transistor $\mathrm{M_{P1}}$ and $\mathrm{M_{N1}}$ are turned off and $\mathrm{C_{R1}}$ and $\mathrm{C_{R2}}$ are not charged. The SR-latch in DCMPH (DCMPL) is in the previous state and $\mathrm{SWH} = 0$ ($\mathrm{SWL} = 1$) to maintain the positive input offset of the comparator CMP in DCMPH (DCMPL) at $\mathrm{V_{OS3}}$ ($\mathrm{V_{OS1}}$) as shown in Fig. 4.

***Region II***: $\mathrm{V_{C1}} + \mathrm{V_{OS3}} > \mathrm{V_{REC}}$, $\mathrm{V_{C1}} + \mathrm{V_{OS1}} > \mathrm{V_{SS}}$. $\mathrm{V_{BuH}}$ is pulled low and $\mathrm{M_{P1}}$ is turned on after the turn-on delay $\mathrm{T_{DHL}}$ to charge $\mathrm{C_{R1}}$ and keep $\mathrm{V_{C1}} \approx \mathrm{V_{REC}}$. $\mathrm{V_{BuL}}$ is still at low level, thus the output state of SR-latch Q ($\bar{\mathrm{Q}}$) is 1 (0). The SWH (SWL) is changed to 1 (0) after the delay $\mathrm{T_{Delay}}$ of the delay unit shown in Fig. 4. The offset voltage $\mathrm{V_{OS3}}$ ($\mathrm{V_{OS1}}$) is changed to the negative offset voltage




| $V_{BuL}$ | $\overline{V_{BuH}}$ | $V_{BuH}$ | Q | $\overline{Q}$ | Region |
|---|---|---|---|---|---|
| 0 | 0 | 1 | Pre_state | | *I, IV* |
| 1 | 0 | 1 | 0 | 1 | *V, VI* |
| 0 | 1 | 0 | 1 | 0 | *II, III* |
| 1 | 1 | 0 | X | X | |

Fig. 4. The circuit structures of (a) DCMPH, DCMPL, and (b) SR-latch.

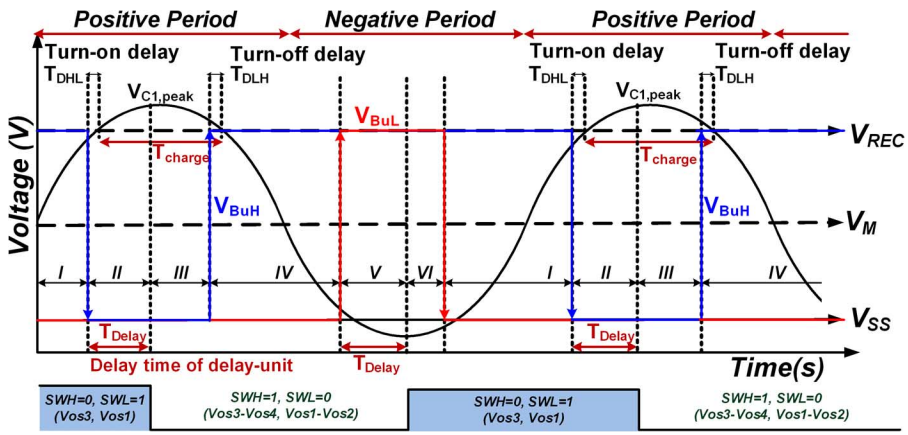



Fig. 5. Steady-state operational waveforms of DCMPH and DCMPL.

$V_{OS3} - V_{OS4}$ $(V_{OS1} - V_{OS2})$ where $V_{OS3} < V_{OS4}$ $(V_{OS1} < V_{OS2})$ as shown in Fig. 4.

***Region III***: $V_{C1} + (V_{OS3} - V_{OS4}) > V_{REC}$, $V_{C1} + (V_{OS1} - V_{OS2}) > V_{SS}$. $V_{BuH}$ is still low and $M_{P1}$ is on to charge $C_{R1}$.

***Region IV***: $V_{C1} + (V_{OS3} - V_{OS4}) < V_{REC}$, $V_{C1} + (V_{OS1} - V_{OS2}) > V_{SS}$. $V_{BuH}$ is pulled to a high level nearly equal to $V_{REC}$. In Fig. 3, $M_{P1}$ is turned off after the turn-off delay $T_{DLH}$ and no conduct current is generated to charge $C_{R1}$.

***Region V***: $V_{C1}+(V_{OS3}-V_{OS4}) < V_{REC}$, $V_{C1}+(V_{OS1}-V_{OS2}) < V_{SS}$. $V_{BuL}$ is pulled to high and $M_{N1}$ is turned on after the turn-on delay to charge $C_{R2}$ and keep $V_{C1} \approx V_{SS}$. After $T_{Delay}$, SWH (SWL) becomes 0 (1) and the offset voltage $V_{OS3} - V_{OS4}$ $(V_{OS1} - V_{OS2})$ is changed back to the offset voltage $V_{OS3}$ $(V_{OS1})$.

***Region VI***: $V_{C1} + V_{OS3} < V_{REC}$, $V_{C1} + V_{OS1} < V_{SS}$. After the power transistor $M_{N1}$ is turned off, the operational period is moved to ***Region I***.

As may be realized from Figs. 3 and 4, when $V_{BuH}$ is changed from high to low, the positive input offset voltage $V_{OS3}$ in the comparator CMP in DCMPH is changed to the negative offset voltage $V_{OS3} - V_{OS4}$ after the delay time $T_{Delay}$ of the delay unit. The delay time $T_{Delay}$ is designed to avoid the malfunction that $V_{BuH}$ might be switched back to high immediately to stop charging output capacitor and introduce voltage ripple if the offset voltage changes to negative instantly without delay to make $V_{C1}+(V_{OS3}-V_{OS4}) < V_{REC}$. Similarly, when $V_{BuL}$ is changed from low to high, the input offset voltage $V_{OS1}-V_{OS2}$ of DCMPL is changed to $V_{OS1}$ after $T_{Delay}$. This can avoid the malfunction that $V_{BuL}$ might be switched back to low immediately to turn off $M_{N1}$ and cause ripples.

The received voltage $V_{AC}$ $(= V_{C1} - V_M)$ of the near-field coil could generate a large ringing voltage $\Delta V_{ring}$ when the power transistor $M_{P1}$ is turned off in Region IV. If $V_{C1} + \Delta V_{ring} + V_{OS3} > V_{REC}$, the power transistor $M_{P1}$ would be turned on again. Thus to prevent the incorrect switching, the delay compensation control is designed to maintain the same offset voltage $V_{OS3} - V_{OS4}$ even after $V_{BuH}$ is switched from low to high. The offset voltages $V_{OS3}$ $(V_{OS1} - V_{OS2})$ and $V_{OS3} - V_{OS4}$ $(V_{OS1})$ make the turn-on and turn-off points exactly at $V_{C1} \geq V_{REC}$ $(V_{C1} \leq V_{SS})$ and $V_{C1} \leq V_{REC}$ $(V_{C1} \geq V_{SS})$, respectively. The control signals SWH and SWL can be generated from the SR-latch as shown in Fig. 4(b). Moreover, the delay compensation is performed fully on-chip without any off-chip control signals.

The CMOS circuit of the comparator CMP with inverters and buffer (driving stage) in DCMPH is shown in Fig. 6. Similar

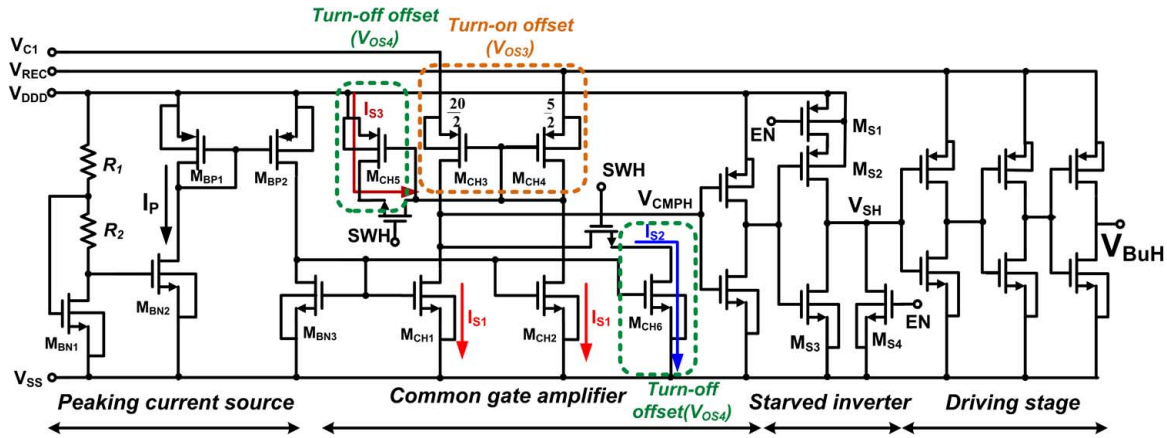



Fig. 6. The CMOS circuit of the comparator, inverters and buffer (driving stage) in the DCMPH.

circuit is also used in DCMPL. As seen in Fig. 6, the circuit consists of a common gate amplifier ($M_{CH1} - M_{CH4}$) where the source terminals of $M_{CH3}$ and $M_{CH4}$ are the input terminals of $V_{C1}$ and $V_{REC}$, three stages of inverters to drive the large gate capacitance of power transistor $M_{P1}$, and two offset control switches driven by SWH. The PMOS common-gate topology is adopted to achieve a high comparison speed because of the low input impedance.

In Fig. 6, $M_{CH3}$ and $M_{CH4}$ are designed with different sizes to produce the positive input offset voltage $V_{OS3}$ and compensate the turn-on delay. The simulated value of $V_{OS3}$ is 505 mV. To produce the negative input offset voltage $V_{OS3} - V_{OS4}$, the control signal SWH $= 1$ and the current of $M_{CH5}$ ($M_{CH6}$) is added to (subtracted from) that of $M_{CH4}$ ($M_{CH3}$). The simulated value of $V_{OS3} - V_{OS4}$ is $-184$ mV. In the DCMPL, the simulated value of $V_{OS1}$ ($V_{OS1} - V_{OS2}$) is 75 mV ($-394$ mV). These offset voltages are designed to generate the exact turn-on and turn-off points.

Since the supply voltage $V_{DDD}$ from DLDO is not kept constant before steady state, the peaking current source which is insensitive to $V_{DDD}$, is designed to provide stable bias currents $I_P$, $I_{S1}$, and $I_{S2}$ as shown in Fig. 6. According to the HSPICE simulation results, the variation of the current $I_P$ in the peaking current source in Fig. 6 is only 16% when $V_{DDD}$ changes from 1.3 V to 1.8 V. This leads to 15.6% maximum variation of the offset voltages $V_{OS1}$, $V_{OS2}$, $V_{OS3}$, and $V_{OS4}$ in both DCMPH and DCMPL.

Since the proposed ILPS is used in the implanted medical devices, the temperature variations are not large when implanted. Only process and supply voltage variations are considered. Under different process corners and variations, the variations of delay compensation are investigated through 5-corner and Monte Carlo HSPICE simulations. The results show that the relative errors on the turn-on (turn-off) delay compensation with respect to the total turn-on time of both power transistors are within $+3.7\%$ and $-0.6\%$ ($+12.1\%$ and $-16.1\%$). The simulated PCE is still greater than 86.1%. If only Monte Carlo variation is considered, the errors are smaller. Under 10% variations of the power supply $V_{DDD}$, the simulated errors on the turn-on (turn-off) delay compensation are within $+3.7\%$ and $-0.8\%$ ($+14.7\%$ and $-22.7\%$). The simulated PCE is slightly decreased to 85.5%.

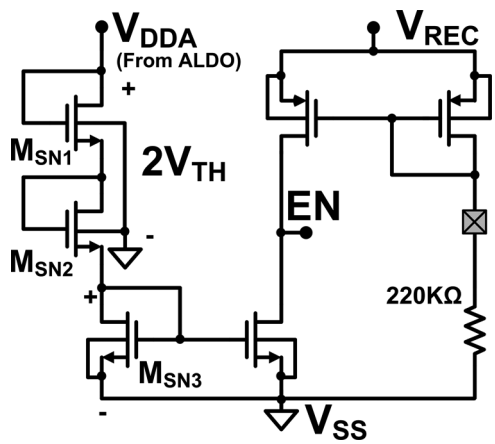



Fig. 7. The schematic of start-up control circuit.

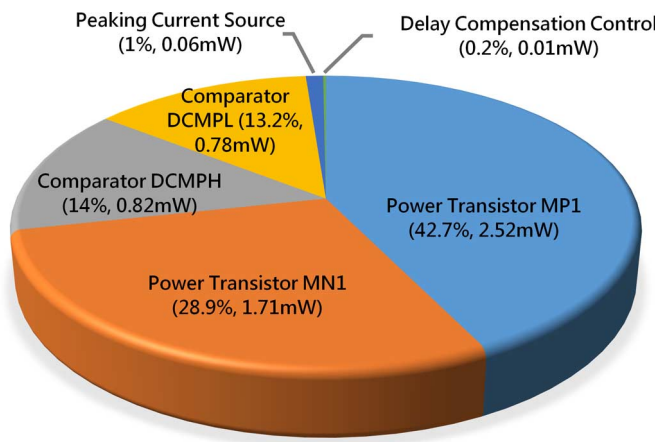



Fig. 8. The pie chart of power dissipation in the proposed active VD.

Under the same Monte Carlo simulation as above, the mean values of the simulated dropout voltage is 402.8 mV and the simulated variations on the dropout voltage are within 12.4% and $-10.1\%$. Under 10% $V_{DDD}$ variations, the variations

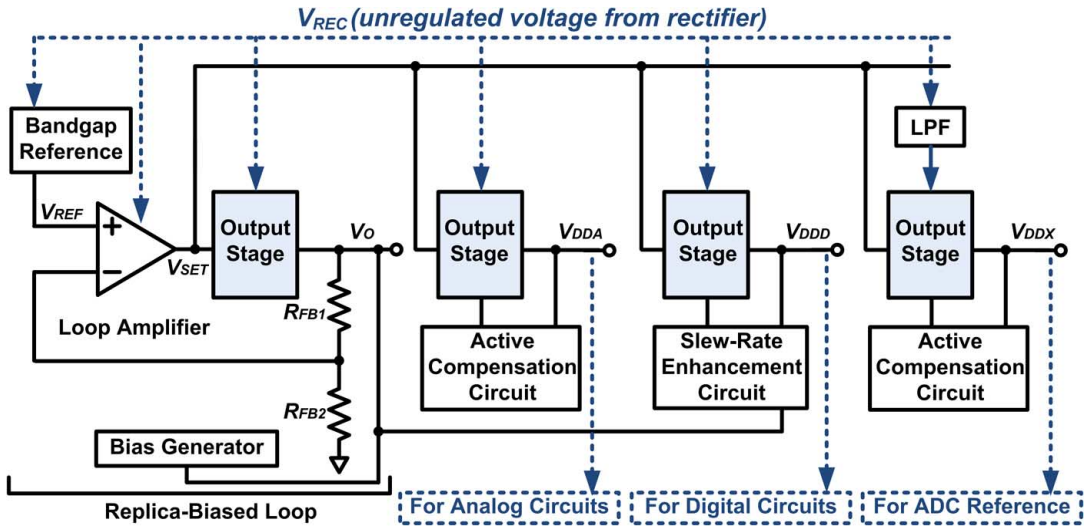



Fig. 9. The block diagram of the supply system with three LDOs.

are within 17.2% and −20.3%. Thus the PV variations of the dropout voltage are acceptable.

It is crucial to self-start the active VD because the comparators are powered by $V_{DDD}$ and $V_{REC} = V_{DDD} = 0$ V initially. To solve the start-up problem, a start-up control circuit shown in Fig. 7 is designed to sense both $V_{REC}$ and analog $V_{DDA}$ from ALDO and generate the voltage EN nearly equal to $V_{REC}$ when $V_{DDA}$ is low. With EN high, which is nearly equal to $V_{REC}$, the current starved inverter $M_{S1} - M_{S4}$ in Fig. 6 blocks the incorrect $V_{SH}$ and turns on the switches $M_{A1} - M_{A4}$ in Fig. 3. The $M_{A1} - M_{A4}$ are medium Vt ($V_{TH,m} \approx 0.27$ V) devices that can be turned on easily when $V_{REC}$ is in low voltage. Thus in the start-up period, both $M_{P1}$ and $M_{N1}$ are connected as MOS diodes to form a passive VD. Until $V_{DDA} > 2V_{TH} + V_{TH0}$ where $V_{TH0}$ is the threshold voltage of normal Vt ($V_{TH0} \approx 0.43$ V) devices under zero substrate bias and $V_{TH}$ is the threshold voltage with substrate bias, $M_{SN1} - M_{SN3}$ are operated in saturation region to pull the voltage level of EN equal to $V_{SS}$. Then the rectifier is operated in the normal active VD mode.

The total power consumption of the proposed active VD is 5.9 mW by simulation and its pie chart showing the power dissipations of each component is given in Fig. 8. When the output power of active VD is 40 mW, the power dissipations on the power transistors $M_{P1}$ and $M_{N1}$ are 2.52 mW (42.7%) and 1.71 mW (28.9%), respectively. The dissipations on DCMPH and DCMPL are 0.82 mW (14%) and 0.78 mW (13.2%), respectively. The dissipation on the peaking current source is 0.06 mW (1%) and that on the delay compensation control circuits is 0.01 mW (0.2%). The simulated PCE is 86.9%.

When the output power of the active VD is reduced to 4 mW, the power transistors dissipate 0.38 mW and the other circuits dissipate 1.6 mW in total. The simulated PCE is decreased to 63.3%. This sets a lower limit of the VD output power.

### *D. Low-Dropout Regulators (LDOs)*

The block diagram of the supply system with fully-integrated multiple LDOs is shown in Fig. 9 [3] where a replica-biased loop and three local regulation loops for analog, digital, and reference-voltage circuits. $V_{REC}$ is the unregulated input voltage from the rectifier. $V_O$, $V_{DDA}$, $V_{DDD}$, and $V_{DDX}$ are the output voltages of replica-biased loop, ALDO, DLDO, and RLDO, respectively. The replica-biased loop is used to generate stable bias voltage $V_{SET}$ for other regulation loops. The output stage is basically based on the flipped voltage follower (FVF) [17]. The main advantage of the FVF is the reduced output impedance by shunt feedback connection, which is the key for obtaining good regulation and achieving frequency compensation. In Fig. 10, $V_{REC}$ is the unregulated input voltage, $V_{OUT}$ is the regulated output such as $V_O$, $V_{DDA}$, $V_{DDD}$, and $V_{DDX}$, and $V_{BUP}$ and $V_{BDN}$ are bias voltages. When there is a variation at $V_{OUT}$ detected by the source of $M_{F2}$, the voltage difference between $V_{OUT}$ and control voltage $V_{SET}$ introduces an error signal. The error signal is then amplified by two cascaded common-gate amplifier by $M_{F1}$ and $M_{F2}$ in order to adjust the gate overdrive voltage of the pass transistor $M_{PA}$. Finally, the drain current of $M_{PA}$ alters to compensate the output voltage $V_{OUT}$. Since the FVF-based output stage has a low output resistance, the loop stability can be guaranteed.

In this design, the FVF-based output stage is adopted in each LDO. Therefore, the fast output voltage regulation is achieved by three local regulation loops. The ALDO, DLDO, and RLDO are responsible for driving analog circuits, digital circuits, and ADC reference,

With the separated ALDO, DLDO, and RLDO, the characteristic of each LDO can be optimized to supply the specified sub-block of an IMD. To power analog circuits, ALDO should generate an accurate DC voltage supply which has good line and load regulation. Besides, a high bandwidth in the power-supply rejection (PSR) is also required to protect the noise-sensitive blocks like VCOs and pre-amplifiers from the coupled input supply noise. Moreover, the output transient current should be minimized to reduce the disturbance on the power-line of the ALDO.

To power digital circuits such as DSP, fast transient response in DLDO is essentially important. Meanwhile, the DLDO must

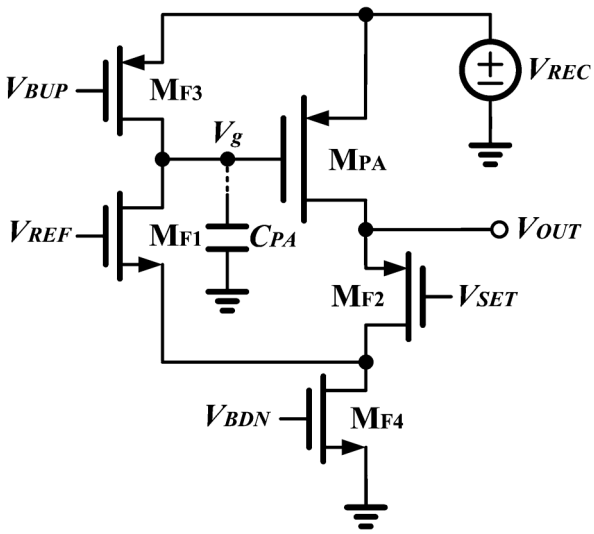



Fig. 10. The schematic of the output stage based on FVF.

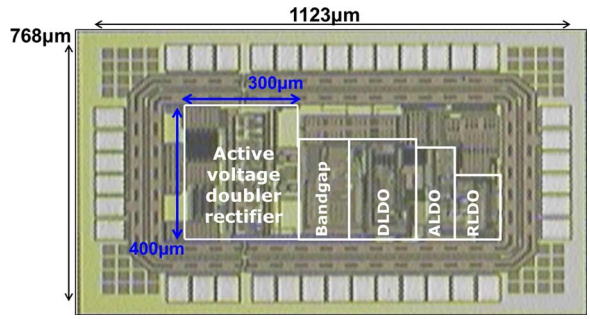



Fig. 11. The chip micrograph.

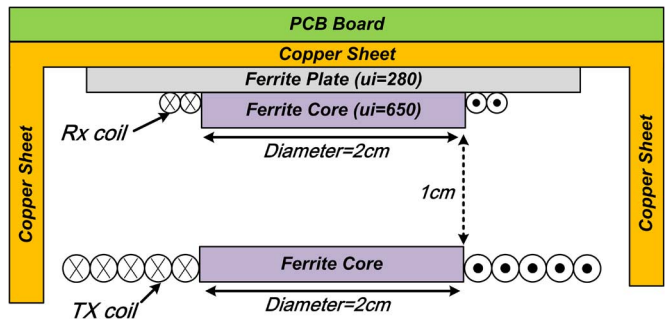



Fig. 12. The experimental setup for the measurement of the fabricated ILPS.

be able to handle a large and steep supply current change. Nevertheless, the digital circuitry is assumed to have greater tolerance to supply variations. Consequently, $\pm 10\%$ of line voltage variations and load variations is acceptable. Generally, the slew-rate (SR) limit is the dominant factor in the transient performance of capacitor-free LDOs. Thus, the slew-rate enhancement (SRE) circuit is essentially required for the DLDO.

The RLDO is specially designed to generate a stable reference voltage for a 10-bit SAR ADC. A good isolation of RLDO is mandatory. Since any disturbance on the reference voltage directly degrades the ADC resolution, the disturbance should be smaller than 1/2 LSB (about 0.88 mVp-p). Moreover, the fixed load current is assumed to be negligible. Therefore, a passive low-pass filter (LPF) can be added to further reduce the supply noises.

The output stage of each LDO is exactly the same but with different aspect ratios according to their requirements in driving capabilities. Through the topology, each regulation loop can be optimized individually to satisfy different requirement and avoid cross-interferences especially from DLDO. The multiple LDOs have 2 V to 1.8 V output voltages and maximum DC output currents are 5 mA, 20 mA, and 1.5 mA in ALDO, DLDO, and RLDO, respectively.

## III. Experimental Results

The proposed ILPS was successfully fabricated in TSMC 1P6M 0.18 $\mu$m CMOS process. The whole chip photograph including the proposed active VD, multiple LDOs, and bandgap reference is shown in Fig. 11. The chip area is $1123\ \mu\mathrm{m} \times 768\ \mu\mathrm{m}$, including the pads. The Rx coil should be close to the chip to reduce the parasitic line inductance. The input power of Tx coil is measured and the measured transmission efficiency of coils is used to estimate the PCE of active VD.

The fabricated chip is directly bonded on printed circuit board (PCB), since the chip-on-board method can have smaller parasitic inductance and resistance. It should be noted that larger parasitic inductances on bond wires could seriously increase the output ripples and degrade the rectifier performance or cause malfunction.

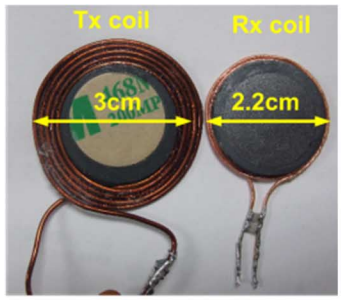
Since the ILPS transfers the power at 13.56 MHz, the larger magnetic field could influence the sensitive components on the PCB to generate larger output voltage ripples on the LDOs. Several simple and effective techniques of magnetic field shielding is proposed [18], [19].

The experimental setup is show in Fig. 12 where the environment is shielded by the copper metal planes. The ferrite plane is placed between Rx coil and PCB board so that the electromagnetic (EM) flux does not leak through the metal plate and better EM shielding can be achieved. At the ferrite-copper boundary, the H-field is nearly tangential and confined inside in the ferrite plate. The normal component of the H-field emitted into the copper is very small, so is the eddy current loss due to the H-field.

### A. Ferrite Core Spiral Coils

Table I is the measurement result of the near-field coils. With the ferrite cores, the inductances, quality factors, and maximum transmission efficiency of the coils are significantly increased. The inductances of coils are measured by impedance analyzer. The relative permeability $(\mathrm{u_r})$ of ferrite cores at 13.56 MHz is shown in the data sheet from the manufacturer. The diameter of the Tx coil is 3 cm and that of the Rx coil is 2.2 cm. The near-field coils with ferrite cores have the measured transmission efficiency of 76.3% which is slightly higher the calculation one (74.3%) and better than the previous work (22% [16], 29.9% [20]).

TABLE I
THE PERFORMANCE OF THE NEAR-FIELD COILS




**Approximate formulae[21]:**

$$P_{eff} = \frac{k^2 Q_1 Q_L}{1+k^2 Q_1 Q_L} \times \frac{Q_2}{Q_2+Q_L} = 74.3\%$$

*Where*
*k : Coupling coefficient (0<k<1)*
*$Q_1$: Unloaded primary quality factor*
*$Q_2$: Unloaded secondary quality factor*
*$Q_L$: Loaded secondary quality factor*

| | | | |
|---|---|---|---|
| **Tx coil L1 (uH)** | *Simulated* | | *Measured* |
| | Without ferrite core | With ferrite core | With ferrite core |
| | 0.97 | 1.82 | 1.58 |
| **Rx coil L2 (nH)** | *Simulated* | | *Measured* |
| | Without ferrite core | With ferrite core | With ferrite core |
| | 174 | 256 | 265 |
| **Relative permeability ($u_r$)** | 200 (@13.56-MHz) | | |
| **Coupling coefficient(k)** | 0.105 | | |
| **Qmax(L1/L2)** | 245/163 | | |
| **L1 dimension** | Diameter=3cm , Thickness=1.91mm | | |
| **L2 dimension** | Diameter=2.2cm, Thickness=1.91mm | | |
| **Transmission efficiency($P_{eff}$)** | 76.3% (Measured) | | |

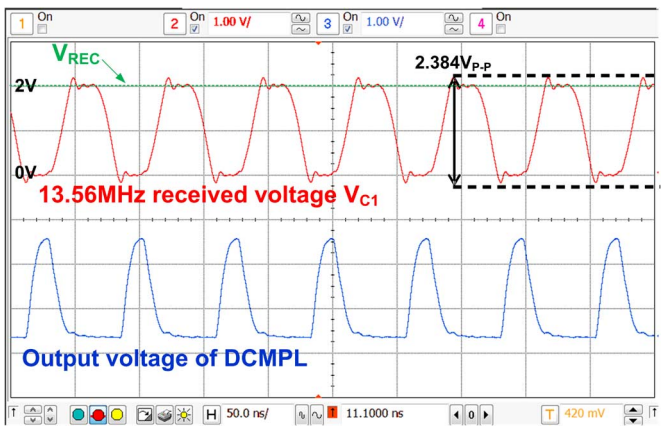



Fig. 13. The input waveform of active VD and the output voltage of DCMPL.

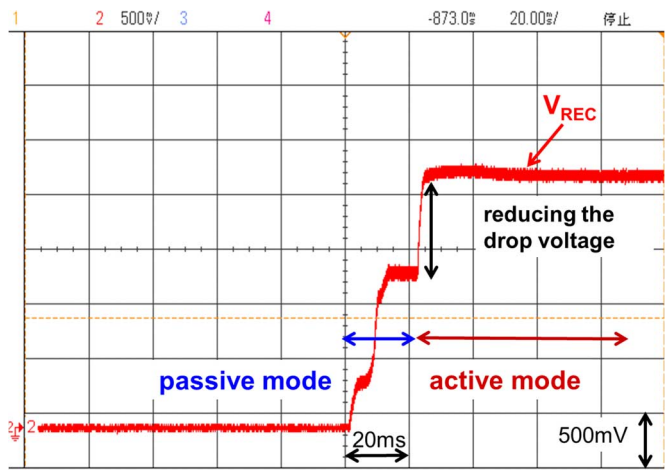



Fig. 14. The waveform of the start-up mechanism.

## B. Active Voltage Doubler Rectifier (VD)

The proposed active VD can output 2 V DC voltage and have a low dropout voltage ($|V_{DS,MP1}|+V_{DS,MN1}$) of 384 mV. Thus the required voltage amplitude of $V_{C1}$ is 2.384 V as shown in Fig. 13. The lower dropout voltage is obtained by delay compensation control and peaking current source. The turn-on and turn-off delay compensations reduce charging current obviously and cause lower dropout voltage. Furthermore, the peaking current source stabilizes bias current so that the comparators have fixed turn-on and turn-off offset voltages without external control. This also improves dropout voltage.

The measured start-up characteristic of the active VD is shown in Fig. 14 where $V_{REC}$ rises from 0 V to 2.3 V during 20 ms. After the start-up period, the active VD changes from passive mode to active mode.

The measured Tx power with 20 mA loading and $R_L = 100\ \Omega$ at power regulator is 61.69 mW. The PCE is derived as 40 mW/(61.69 mW × 76.3%) = 85%, where 76.3% is the measured transmission efficiency of the near-field coils. The variations of measured PCE and VCR ($V_{REC}/V_{AC}$) versus output loading currents from 25 mA to 4 mA are shown in Fig. 15 where different $R_L$ are indicated. As can be seen from Fig. 15, if the current loading is reduced to 4 mA (8 mW) with $V_{REC} = 2$ V, the VCR is slightly reduced to 1.55 and the PCE is decreased to 72.5%. If the current loading is increased to 25 mA (50 mW), the VCR is slightly reduced to 1.61 and the PCE to 82.4%. In Fig. 16, the measured PCE and VCR versus $V_{AC}$ from 1.15 V to 1.35 V with $R_L = 100\ \Omega$ and the loading currents of 20 mA and 4 mA are plotted. As can be seen from Fig. 16, both PCE and VCR have small variations.

The measured voltage output ripple of the fabricated active VD is shown in Fig. 17. Since the near-field coils are close to the active VD in the experimental setup, the additional 13.56 MHz noise is coupled into the output node $V_{REC}$ of active VD. The measured active VD output peak-to-peak ripple is 10.4 mV under 20 mA output current. Since the DLDO output voltage ($V_{DDD}$) is the supply the comparator in the active VD, under

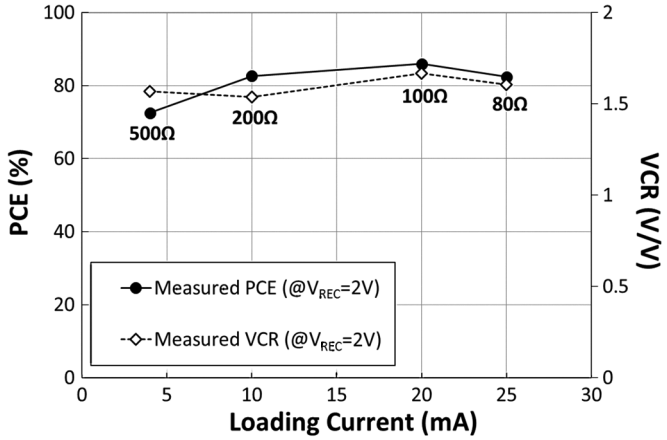



Fig. 15. The variations of measured PCE and VCR ($\mathrm{V_{REC}}/\mathrm{V_{AC}}$) versus output loading currents with different $\mathrm{R_L}$.

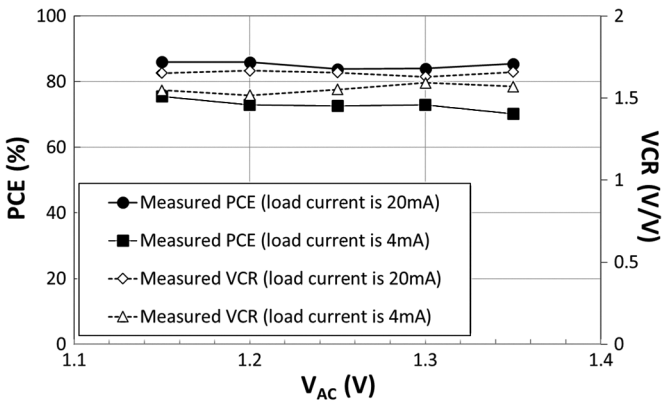



Fig. 16. The measured PCE and VCR versus $\mathrm{V_{AC}}$ with $\mathrm{R_L} = 100\ \Omega$.

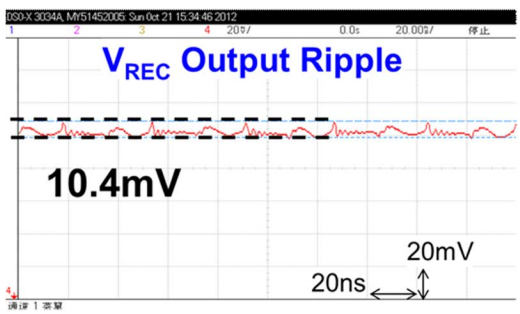



Fig. 17. The voltage output ripple of proposed active VD.

the maximum transient current of 3 mA in DLDO, the voltage ripple of VD is slightly increased.

The main contributing factors to a low ripple at $\mathrm{V_{REC}}$ are exact delay compensation, chip-on-board method with low parasitic bonding-wire inductances, and the shielding of Rx coil.

### C. Low-Dropout Regulators (LDOs)

Fig. 18 shows the measurement results of transient load regulation of DLDO. When the loading current of DLDO changed from light load of 0.4 mA to heavy load of 20 mA, the corresponding ripple voltage is 150 mV. With the same loading current variance of the DLDO, the output voltage variations

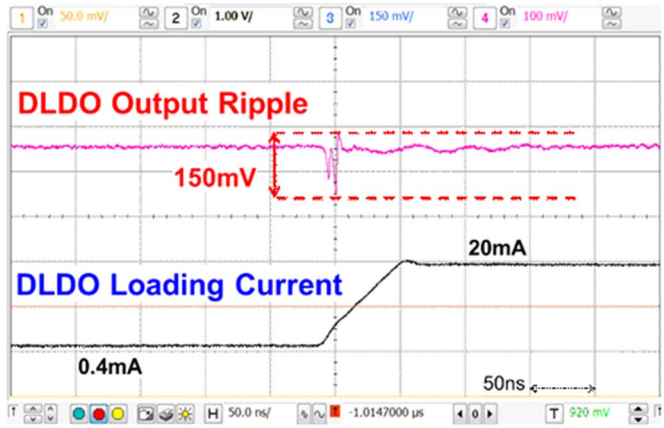



Fig. 18. The measurement result of transient load regulation of DLDO.

are only 3.973 mV and 2.79 mV for ALDO and RLDO, respectively, are shown in Fig. 19. Both ALDO and RLDO have low crosstalk noise from DLDO. The measured PSR of ALDO, DLDO, and RLDO in 10 kHz (27 MHz) are $-74$ dB, $-52$ dB, and $-66$ dB ($-7$ dB, $-1$ dB, and $-31$ dB), respectively. The multiple LDOs have current efficiencies of 95.93%, 98.75% and 91.95% in ALDO, LDO and RLDO, respectively. The PCE of multiple LDOs can be calculated as

$$\begin{aligned}\mathrm{PCE} &= \frac{I_{\mathrm{Load}} \times V_{\mathrm{DDD}}}{(I_{\mathrm{Load}} + I_Q) \times V_{\mathrm{IN}}} \\ &= \text{average current efficiency} \times \frac{1.8}{2} \qquad (1) \\ &= \frac{5 \times 95.93\% + 20 \times 98.75\% + 1.5 \times 91.95\%}{5 + 20 + 1.5} \\ &\quad \times \frac{1.8}{2} = 88\%. \qquad (2)\end{aligned}$$

The performance comparison with other reported CMOS delay-compensated 13.56 MHz active rectifiers is given in Table II. As compared with [8]–[10], where both turn-on delay and turn-off delay are compensated by using off-chip control signals, the proposed VD delivers 20 mA output current while maintaining the lower dropout voltage of 384 mV which is smaller than those in the previous works (700 mV [8], 1.3 V [9], 520 mV [10]). The PCE of 85% is higher than others. It also provides a lower output peak-to-peak ripple (10.4 mV) than those in the previous works ($\approx$ 80 mV [8], $\approx$ 50 mV [9], $\approx$ 22 mV [10]).

The main reasons of lower ripple in the designed LDOs are the lower ripples in VD as well as the separated LDOs to reduce the cross-talk effect.

## IV. Conclusion

An ILPS circuit for IMD with hand winding coils, integrated rectifier, and multiple LDOs has been proposed and fabricated in TSMC 0.18 $\mu$m CMOS technology. To enhance quality factor and magnetic flux, the near-field coils with ferrite cores is designed. The spiral coils with ferrite core have the measured transmission efficiency of 76.3%. The active VD with on-chip delay compensated comparators is designed to avoid the use of external control signals.


Fig. 19. The measurement results of (a) ALDO and (b) RLDO output isolation.

TABLE II
COMPARISON OF MEASURED PERFORMANCE OF CMOS ACTIVE RECTIFIERS

| Parameters | 2011 T-CAS I[8] | 2012 ISSCC[9] | 2013 TBCAS[10] | This work |
|---|---|---|---|---|
| Technology | 0.5-μm CMOS | 0.5-μm CMOS | 0.5-μm CMOS | 0.18-μm CMOS |
| Structure | Active rectifier | Active voltage doubler rectifier | Active voltage doubler rectifier | Active voltage doubler rectifier |
| Delay compensation | On delay& Off delay | On delay& Off delay | On delay& Off delay | On delay& Off delay |
| Chip area (Without PAD) | 0.18mm$^2$ | 0.585mm$^2$ | 0.144mm$^2$ | 0.12mm$^2$ |
| Input amplitude $V_{AC}$ | 3.8V | 2.2V | 1.46V | 1.192V |
| Output voltage $V_{REC}$ | 3.12V @$R_L$=500Ω | 3.1V @$R_L$=500Ω. | 2.4V @$R_L$=1KΩ | 2V @$R_L$=100Ω |
| Maximum output current | 6.24mA | 6.2mA | 2.4mA | 20mA |
| Rectifier output power | ~20mW | ~20mW | ~5.8mW | 40mW |
| Operating frequency | 13.56MHz | 13.56MHz | 13.56MHz | 13.56MHz |
| Dropout voltage | 700mV | ~1.3V | ~520mV | 384mV |
| Rectifier output voltage ripple | 80mV | ~50mV | ~22mV | 10.4mV |
| Average $V_{REC}/V_{AC}$ | 0.82 | 1.41 | 1.64 | 1.67 |
| Power conversion efficiency(PCE) | **80.2% @$R_L$=500Ω (70% @$R_L$=150Ω)** | **70% @$R_L$=500Ω** | **79% @$R_L$=1KΩ (68% @$R_L$=150Ω)** | **85% @$R_L$=100Ω** |

For further PCE improvement, the multiple LDOs is adopted to fit different power needs in different circuits of IMDs. The measured PCE of VD is 85% at 40 mW output power on 100 Ω load. The measured ripple voltages of rectifier, ALDO, DLDO, and RLDO output are 10.4 mV, 5.9 mV, 72.4 mV, 1.5 mV, respectively. The 74.8% whole chip PCE is achieved, that is the multiplication of PCEs of active VD and multiple LDOs.

The exact delay compensation, chip-on-board method with low parasitic bonding-wire inductances, and the shielding of Rx coil leads to low ripple voltages in rectifier whereas the low ripple of rectifier and the separated LDOs with less cross-talk makes low ripple voltages in the three LDOs.

The proposed ILPS has been integrated with the epilepsy control SoC and successfully tested in rats.

## ACKNOWLEDGMENT

The authors would like to thank National Chip Implementation Center (CIC) for technical support and chip fabrication.

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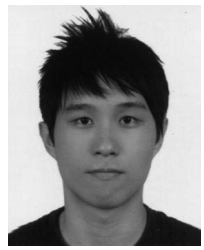

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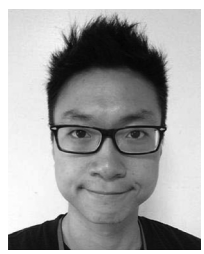

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