High-Performance GAA Sidewall-Damascened Sub-10-nm *In Situ* n^+-Doped Poly-Si NWs Channels Junctionless FETs

Po-Yi Kuo, *Member, IEEE*, Yi-Hsien Lu, and Tien-Sheng Chao

***Abstract*— The gate-all-around sidewall-damascened sub-10-nm *in situ* n^+-doped poly-Si nanowires channels junctionless FETs (GAA SWDNW-JLFETs) with one NW of sub-50-nm^2 cross-sectional area have been successfully fabricated and demonstrated in the category of poly-Si NWs JL transistors for the first time. Some key properties are explored: 1) novel SWDNW processes; 2) dependence of threshold voltage (V_{TH}) and subthreshold swing (S.S.) on dimension of *in situ* n^+-doped poly-Si NWs in GAA SWDNW-JLFETs; and 3) thermal stability of main electrical characteristics under high operating temperature. The high-performance GAA SWDNW-JLFETs show good electrical characteristics: 1) steep S.S. ~ 75 mV/decade; 2) low gate supply voltage (V_G) = 1.5 V; 3) high ON/OFF currents ratio (I_{ON}/I_{OFF}) ~ 8 x 10^7 and significantly high-thermal stability without implantation processes and hydrogen-related plasma treatments for future 3-D integrated circuits, system-on-panel, and system-on-chip applications.**

***Index Terms*— Gate-all-around (GAA), junctionless (JL), sidewall-damascened nanowires (SWDNWs).**

I. Introduction

GATE-ALL-AROUND (GAA) silicon nanowire (NW) transistors are promising candidates for future CMOS devices and applications due to their reduced short-channel effects [1], [2]. The sub-10-nm undoped poly-Si NWs-based devices are also very promising for construction of 3-D integrated circuits (3-D ICs) in our previous works [3], [4]. Recently, the junctionless (JL) transistors have been proposed and demonstrated [5]–[10]. The absence of a doping concentration gradient completely eliminates diffusion of impurities and problem of sharp doping profile formation, since the doping concentration in the JL transistor is high, uniform, and homogenous across the source (S), channel, and drain (D) [5]. The current transport is concentrated in center of a uniform doping channel, which decreases the influences of Si/gate oxide interfaces [10]. However, there are negative V_{TH} and gradual subthreshold swing (S.S.) tendencies in GAA large dimension n^+-doped poly-Si NWs and non-GAA n^+-doped poly-Si thin-film channel JL transistors compared with conventional junction devices [7], [8]. Using thermal dry oxidation method at high temperature to thin thickness of n^+ implanted poly-Si thin films is not compatible for 3-D ICs applications and not easy to control the thickness of wide poly-Si thin films with grain boundaries [10]. In this paper, for the first time, the novel GAA sidewall-damascened sub-10-nm *in situ* n^+-doped poly-Si NWs channels JL FETs (GAA SWDNW-JLFETs) with one NW of sub-50-nm^2 cross-sectional area are successfully fabricated and demonstrated in the category of poly-Si NWs JL FETs, through the use of novel SWDNWs fabrication processes.

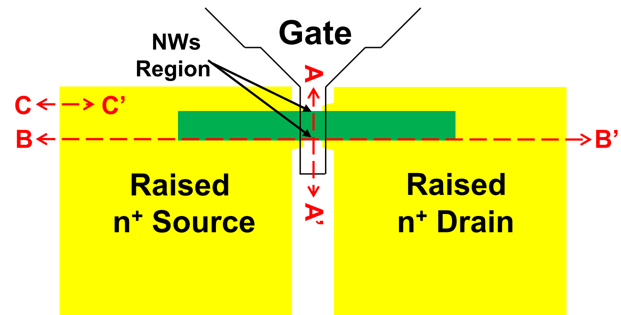

Fig. 1. New layout masks of GAA SWDNW-JLFETs.

The proposed device simultaneously possesses sub-10-nm scaled *in situ* n^+-doped poly-Si NWs channels and 100-nm raised n^+-doped S/D pads without the use of advanced lithographic tools and implantation process. The characteristics and thermal stability of GAA SWDNW-JLFETs are superior and do not require hydrogen-related plasma treatments. High-performance GAA SWDNW-JLFETs with low gate supply voltage (V_G), steep S.S., and high ON/OFF currents ratio (I_{ON}/I_{OFF}) can be obtained. These advantages hold a great promise for the realization of 3-D ICs, system-on-panel (SOP), and system-on-chip (SoC).

II. Devices Design and Experiments

The details of the sidewall-damascened sub-10-nm undoped poly-Si NWs channels processing steps were reported in our previous works [3], [4]. In order to decrease the gate-induced drain leakages (GIDL) and parasitic gate to S/D capacitances, the new layout masks of GAA SWDNW-JLFETs are designed in Fig. 1. In Fig. 1, we have decreased the mask overlapped areas of gate to raised n^+ S/D pads.

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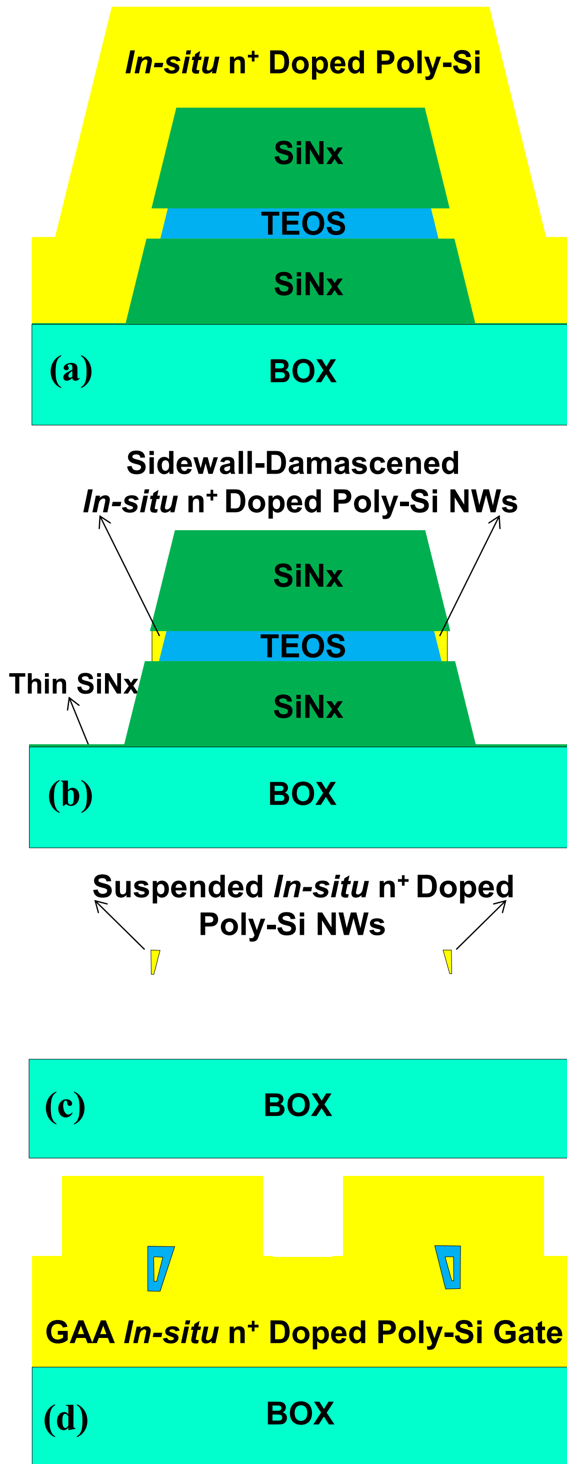


Fig. 2. Key process steps of GAA SWDNW-JLFETs shown by the schematic view of cross-sectional structures along the *A–A*'. (a) Deposition of 100-nm-thick *in-situ* n^+ doped poly-Si layer. (b) Formation of raised n^+ S/D pads and sidewall-damascened *in-situ* n^+ doped poly-Si NWs channels. (c) Suspension of *in-situ* n^+ doped poly-Si NWs channels after removing the dummy N/O/N sandwich structures. (d) GAA TEOS gate oxide and *in-situ* n^+ doped poly-Si gate.

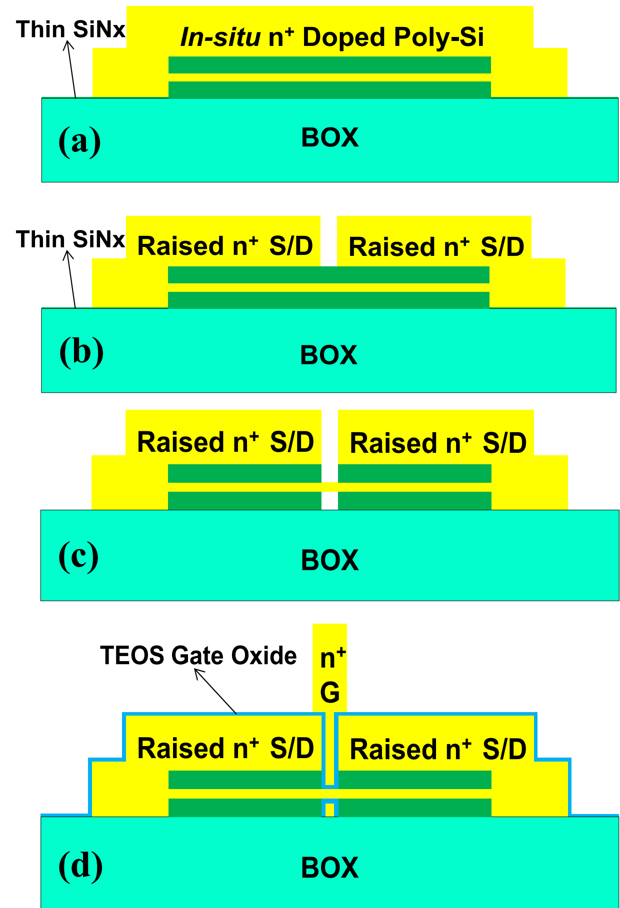


Fig. 3. Key process steps of GAA SWDNW-JLFETs shown by the schematic view of cross-sectional structures along the *B–B*'. (a) Deposition of 100-nm-thick *in-situ* n^+ doped poly-Si layer. (b) Formation of raised n^+ S/D pads and sidewall-damascened *in-situ* n^+ doped poly-Si NWs channels. (c) Suspension of *in-situ* n^+ doped poly-Si NWs channels after removing the dummy N/O/N sandwich structures. (d) GAA TEOS gate oxide and *in-situ* n^+ doped poly-Si gate.

This corked-gate structure in Fig. 1 has many advantages: 1) reducing parasitic *S*/*D* resistance; 2) self-alignment of gate to n^+ NW channels; 3) protection of NW channels during gate etching; and 4) shorter NW channel length between raised n^+ *S*/*D* pads. The NW channel length is equal to the distance between raised n^+ source and drain pads. When the suspended NW is longer, it is broken more easily during processes. In order to understand the novel sidewall-damascened sub-10-nm *in situ* n^+-doped poly-Si NWs processes, we also exhibit the cross-sectional structures along the *A–A*', *B–B*', and *C–C*' in Fig. 1.

The key process steps of GAA SWDNW-JLFETs viewed from different directions are shown in Figs. 2 and 3. Figs. 2 and 3 display the schematic view of cross-sectional structures along the *A–A*' and *B–B*', respectively. In Figs. 2(a) and 3(a), a 100-nm-thick *in situ* n^+-doped poly-Si layer was deposited on trapezoid-shaped SiN_x/tetraethoxysilane (TEOS)/SiN_x (N/O/N) dummy sandwich structures and remnant thin SiN_x films by low-pressure chemical vapor deposition (LPCVD) at 550 °C.

Next, the raised n^+ *S*/*D* pads and sidewall-damascened nanoscaled *in situ* n^+-doped poly-Si NWs channels in the lateral cavities were simultaneously formed by an anisotropic selective dry etching step in Figs. 2(b) and 3(b). The suspended *in situ* n^+-doped poly-Si NWs channels were then selectively formed by removing the dummy N/O/N sandwich

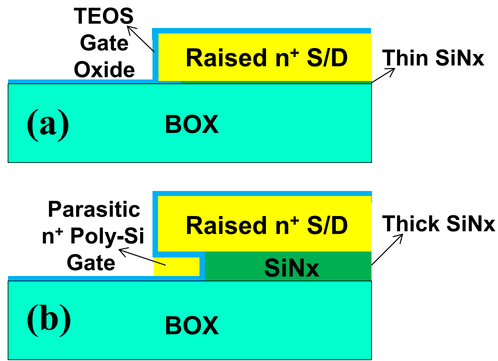


Fig. 4. Schematic view of cross-sectional structures along the *C–C'* after patterning GAA poly-Si gate by dry etching with different thickness of remnant SiN_x films. (a) Raised n^+ S/D pads were deposited on remnant thin SiN_x in our works. (b) Raised n^+ S/D pads were deposited on remnant thick SiN_x in unwanted cases.

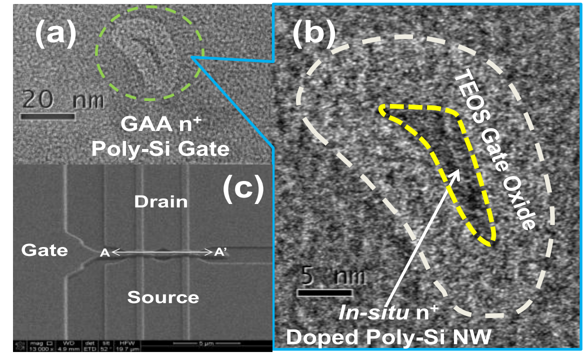


Fig. 5. (a) and (b) Cross-sectional TEM along the *A–A'*. (c) Top view SEM images of SWDNW-JLFETs. The D_{NW} is <10 nm and the A_{NW} is ~45 nm^2.

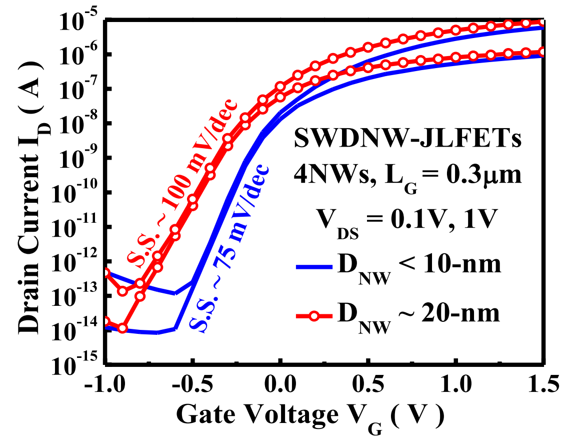


Fig. 6. Measured I_D–V_G of SWDNW-JLFETs with different D_{NW}.

structures using hot phosphoric acid and dilute HF solutions in Figs. 2(c) and 3(c). We experimentally discovered that the etched rate of *in situ* n^+-doped poly-Si was slightly higher than that of undoped poly-Si by hot phosphoric acid process during the removal of the dummy N/O/N sandwich structures. In this paper, the NW dimension (D_{NW}) of *in situ* n^+-doped poly-Si NWs can be scaled down through the tilted sidewall of trapezoid-shaped N/O/N dummy sandwich structures and controlling the etched time by hot phosphoric acid at low temperature. In Figs. 2(d) and 3(d), a 7-nm-thick LPCVD TEOS gate oxide was deposited, and a 200-nm-thick *in situ* n^+-doped poly-Si gate was deposited and then gate patterned. The raised n^+ S/D pads and sidewall-damascened *in situ* n^+-doped poly-Si NWs channels were conveniently activated after deposition of TEOS gate oxide by LPCVD at 700 °C for 2 h. The measured sheet resistance (Rs) of a 100-nm-thick *in situ* n^+-doped raised S/D is ~100 Ω/□. Thus, the resistivity of *in situ* n^+-doped raised S/D is $\sim 1 \times 10^{-3}$ Ω-cm and the doping concentration is $\sim 7 \times 10^{19}$ cm^{-3}. The conventional n^+-i-n^+ junction top-gate planar thin-film transistors (TFTs) with a 50-nm-thick poly-Si channel and 15-nm-thick TEOS gate oxide/200-nm-thick n^+-doped poly-Si gate were also fabricated to serve as controls. The channel width (W)/gate length (L_G) of control devices is 0.35/0.35 μm. After passivation and metallic processes, all devices were fabricated without hydrogen-related plasma treatments.

In our novel sidewall-damascened NWs fabrication processes, a designed thin SiN_x film was remained on BOX after dry etching dummy N/O/N sandwich structures. Fig. 4 exhibits the schematic view of cross-sectional structures along the *C–C'* after patterning GAA poly-Si gate by dry etching. In our works [Fig. 4(a)], the raised n^+ S/D pads were deposited on the remnant thin SiN_x film without parasitic n^+ poly-Si gates under the edges of raised n^+ S/D pads. In the unwanted case [Fig. 4(b)], the raised n^+ S/D pads were deposited on the remnant thick SiN_x film. The parasitic n^+ poly-Si gates were also damascened under the edges of raised n^+ S/D pads resulted from the sidewall-undercut cavities in the remnant thick SiN_x film after removing dummy N/O/N sandwich structures by hot phosphoric acid solutions. The unwanted parasitic n^+poly-Si gates will increase the overlapped areas of poly-Si gate to raised n^+ S/D pads, which leads to abnormal GIDL and poor OFF-state currents [11].

III. Results and Discussion

Fig. 5 shows the cross-sectional transmission electron microscope (TEM) along the *A–A'* and top view scanning electron microscope (SEM) images of GAA SWDNW-JLFETs. In Fig. 5(b), the average D_{NW} of one *in situ* n^+-doped poly-Si NW is <10 nm and the NW cross-sectional area (A_{NW}) of one *in situ* n^+-doped poly-Si NW is ~45 nm^2. The D_{NW} is defined by two conditions: 1) NW average width and 2) NW cross-sectional area (A_{NW}). In Fig. 5(b), the NW average width can be defined as (5 + 12 nm)/2 = 8.5 nm (<10 nm). The real A_{NW} is ~45 nm^2 (smaller than 10 nm ×10 nm = 100 nm^2). Thus, D_{NW} is <10 nm. The final triangle-shaped *in situ* n^+-doped poly-Si NWs with small A_{NW} are due to the tilted sidewall of trapezoid-shaped N/O/N dummy sandwich structures and shrinking again by controlling the etched time by hot phosphoric acid at low temperature.

Fig. 6 shows the measured I_D–V_G of GAA SWDNW-JLFETs with different D_{NW} and the measured I_D–V_D of GAA SWDNW-JLFETs with different D_{NW} is shown in Fig. 7. All characteristics of GAA SWDNW-JLFETs

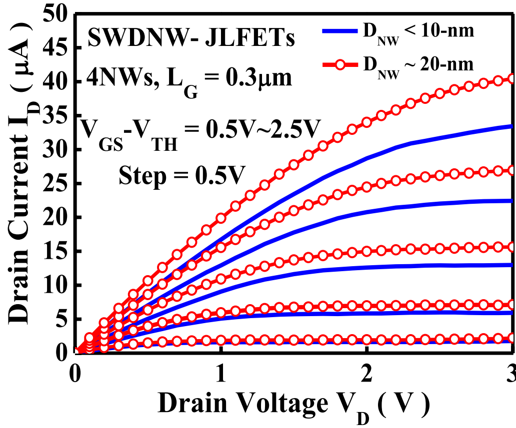


Fig. 7. Measured I_D–V_D of SWDNW-JLFETs with different D_{NW}.

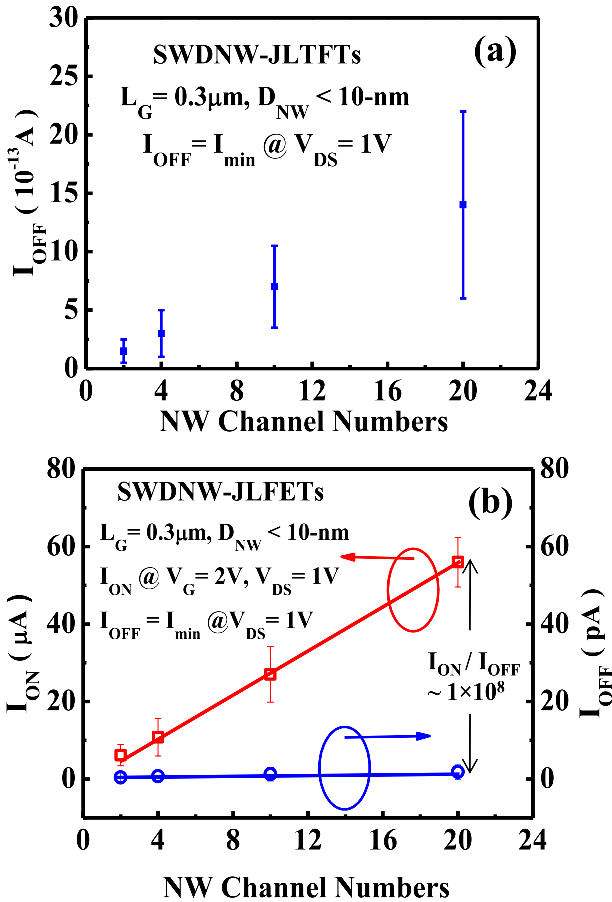
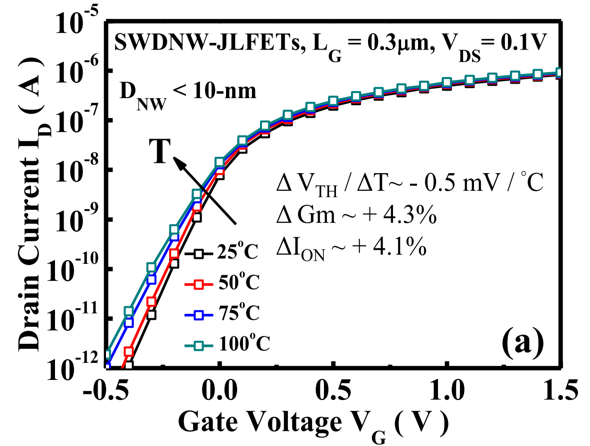
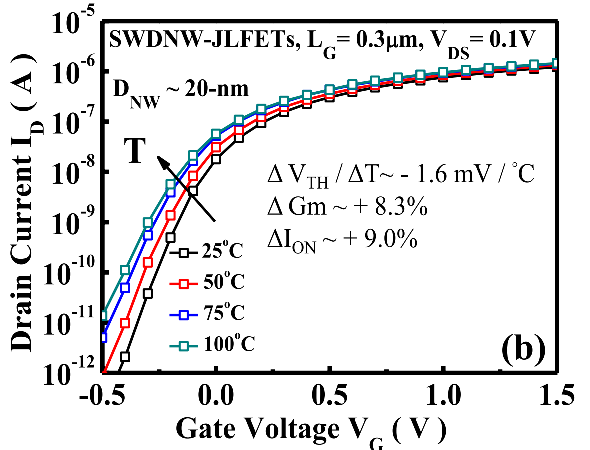


Fig. 8. (a) Measured detailed I_{OFF} of SWDNW-JLFETs with D_{NW} < 10 nm with different NW channel numbers. (b) Measured I_{ON} and I_{OFF} of SWDNW-JLFETs with D_{NW} < 10 nm with different NW channel numbers.





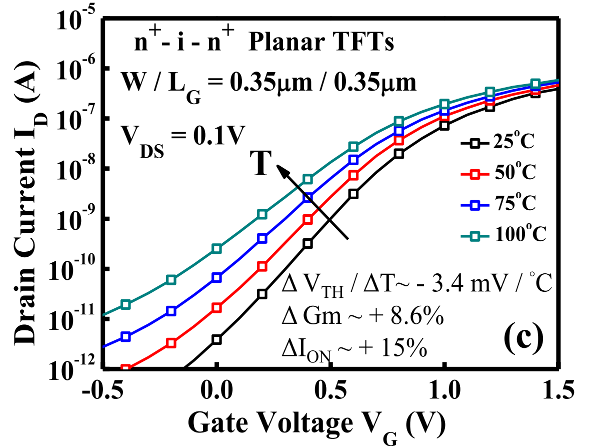


Fig. 9. Temperature dependence on I_D–V_G of (a) GAA SWDNW-JLFETs with D_{NW} < 10 nm, (b) GAA SWDNW-JLFETs with D_{NW} ~ 20 nm, and (c) conventional n$^+$-i-n$^+$ top-gate planar-TFTs from 25 °C to 100 °C.

with D_{NW} < 10 nm are superior to those of GAA SWDNW-JLFETs with D_{NW} ~ 20 nm except lower I_{ON}. The GAA SWDNW-JLFETs with D_{NW} < 10 nm exhibits a more positive V_{TH} compared with the GAA SWDNW-JLFETs with D_{NW} ~ 20 nm. In our GAA SWDNW-JLFETs, the adjustment of V_{TH} can be achieved through not only gate work function, but also D_{NW} and channel doping concentration [12]. The GAA SWDNW-JLFETs with D_{NW} < 10 nm also displays the steepest S.S. (~75 mV/decade) due to its smallest *in situ* n$^+$-doped poly-Si NWs dimension and better gate controllability [3]. Although the sub-10-nm *in situ* n$^+$-doped poly-Si NWs are not single crystalline for all channels, the characteristics of GAA SWDNW-JLFETs with D_{NW} < 10 nm without hydrogen-related plasma treatments are close to those of single-crystalline MOSFETs. It is believed that the electrical characteristics of GAA SWDNW-JLFETs with D_{NW} < 10 nm can be improved due to significant reduction of number of grain boundaries in the sub-10-nm *in situ* n$^+$-doped poly-Si NWs channels [3], [4]. In JLFETs, the S.S. is affected

TABLE I
COMPARISON OF IMPORTANT PARAMETERS FROM THE GAA SWDNW-JLFETs AND OUR PREVIOUS WORKS [4]

	GAA SWDNW-JLFETs with D_{NW} < 10-nm	GAA SWDNW-JLFETs with D_{NW} ~ 20-nm	Ref .[4]
D_{NW} (nm)	< 10	~ 20	~ 10
Junction Type	Junctionless (*In-situ* n^+ Doped)	Junctionless (*In-situ* n^+ Doped)	n^+-i- n^+ Junction (Implantation)
V_{TH} (V)	-0.03	- 0.19	+ 0.23
EOT (nm)	7	7	7
S.S. (mV/dec.)	~ 75	~ 100	~ 99
I_{ON} / I_{OFF} (I_{ON}: V_G = 2V, V_{DS} = 1V) (I_{OFF} = Imin, V_{DS} = 1V)	$\sim 8 \times 10^7$	$\sim 9 \times 10^7$	$\sim 1.5 \times 10^7$
NH_3 Plasma	w/o	w/o	w/o

by D_{NW}, gate oxide thickness, and number of grain boundaries in poly-Si NW channels [13]. We used a 7-nm-thick gate oxide in this paper. The number of grain boundaries in poly-Si NW channels can be decreased by shrinking D_{NW} and scaling NW channel length (L_{CH}). Therefore, we think that S.S. ~60 mV/decade can be achieved by reducing gate oxide thickness, scaling NW channel length < 100 nm, and shrinking D_{NW} < 5 nm.

In particular, the GAA SWDNW-JLFETs have lower I_{OFF} and improved GIDL compared with the previous works [3], [4] in the OFF-state. Since we fabricated the GAA SWDNW-JLFETs by the novel SWDNWs fabrication processes without implantation processes, the damages induced by implantation can be eliminated and total overlapped areas of poly-Si gate to raised n^+ S/D pads can be reduced. Fig. 8 shows the measured I_{ON} and I_{OFF} of SWDNW-JLFETs with D_{NW} < 10 nm with different NW channel numbers. The SWDNW-JLFETs with D_{NW} < 10 nm with multiple channels have similar low I_{OFF} characteristics, where the I_{ON} is nearly proportional to the number of channels. The best $I_{ON}/I_{OFF} \sim 1 \times 10^8$ can be achieved in NW channel numbers of 20 in Fig. 8(b).

One of the big challenges facing 3-D ICs is how to remove the heat dissipated on the upper layers to keep a high-performance chip temperature, especially in applications that require stacking of multiple processor and memory chips [14]. It is important that devices have a good thermal stability of electrical characteristics under elevated high operating temperature for 3-D ICs applications. Fig. 9 details the temperature dependence on electrical characteristics of GAA SWDNW-JLFETs with D_{NW} < 10 nm, GAA SWDNW-JLFETs with D_{NW} ~ 20 nm, and conventional n^+-i-n^+ top-gate planar-TFTs from 25 °C to 100 °C. In this paper, the number of grain boundaries can be significantly diminished in sub-10-nm *in situ* n^+-doped poly-Si NWs channels. The GAA SWDNW-JLFETs with D_{NW} < 10 nm are insensitive to temperature variations due to the smallest poly-Si NWs [4]. This good thermal stability of main electrical characteristics under high operating temperature has been demonstrated in the category of poly-Si NWs JL transistors for the first time.

The comparison of important parameters from the GAA SWDNW-JLFETs and our previous works [4] is shown in Table I. The GAA SWDNW-JLFETs with D_{NW} < 10 nm with the smallest D_{NW} exhibit the steeper S.S., and higher I_{ON}/I_{OFF} compared with previous works [4] due to implantation free processes, better gate controllability, and less number of grains and grain boundaries in the NWs channels region [13].

IV. CONCLUSION

The GAA SWDNW-JLFETs with sub-10-nm *in situ* n^+-doped poly-Si NWs have been successfully fabricated and demonstrated. The GAA SWDNW-JLFETs without complex ultrashallow n^+ S/D junction processes and extra S/D activation after implantation significantly simplify fabrication and reduce thermal budgets. The V_{TH} of GAA SWDNW-JLFETs can be modified more positively by shrinking the D_{NW}, resulting in better gate controllability, smaller DIBL, steeper S.S, and higher thermal stability. The high-performance GAA SWDNW-JLFETs combined with GAA gate-stacked structure, raised S/D, and sub-10-nm *in situ* n^+-doped poly-Si NWs channels appear great potential for future 3-D ICs, SOP, and SoC applications.

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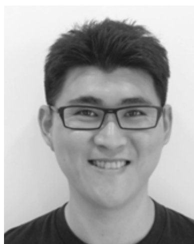

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