Fabrication of High-Performance Poly-Si Thin-Film Transistors With Sub-Lithographic Channel Dimensions

Ko-Hui Lee, Horng-Chih Lin, *Senior Member, IEEE*, and Tiao-Yuan Huang, *Fellow, IEEE*

***Abstract*—A method for fabrication of tri-gate polycrystalline silicon (poly-Si) transistors with short channel length and width is proposed and demonstrated without employing costly lithographic tools. Specifically, the method employs a spacer formation technique to extend source and drain regions so as to scale down the channel length below sub-lithographic dimension. Concurrently, the channel width is scaled down below sub-lithographic dimension by using a photoresist (PR) trimming technique. Our results show that the reduction in the planar channel width is essential for suppressing the short-channel effects. Finally, devices with channel length of 120 nm and planar channel width of 110 nm are demonstrated with superior electrical characteristics in terms of small subthreshold swing (146 mV/dec) and low drain-induced-barrier-lowing value (100 mV/V).**

***Index Terms*—Lithography, poly-Si, thin-film transistor (TFT), tri-gate, trimming.**

I. Introduction

POLY-Si thin-film transistors (TFTs) have been implemented in the manufacturing of active-matrix liquid-crystal displays [1], [2]. The technology also exhibits great potential for system-on-panel (SOP) [1] and 3D stackable devices/circuits on bulk CMOS circuits [3], [4]. The downscaling of TFT devices is essential for improving the performance and reducing the power consumption by lowering the operation voltage. Normally the channel length scaling is done with a refined lithographic solution at the expense of rising cost. Moreover, the device miniaturization has inevitably accompanied by problems such as short-channel effects (SCEs) and the increase in off-state leakage [5], [6]. These concerns must be carefully addressed as the channel length is significantly shortened. In line with this, the multiple-gate configurations have been proposed as a promising solution to solve the above issues [7]–[9] by their extraordinary gate controllability over the channel potential, thereby effectively suppressing the SCEs and the off-state leakage current. It should be noted that, in order to capitalize the above capability, the planar width of the channel in the multiple-gated configurations need to be shrunk as well [7].

Previously, we've presented several approaches to define the poly-Si nanowire channels using conventional G-line or I-line based lithography [10]–[12]. However, the minimum channel length is around 400 nm as imposed by the limitation of I-line lithography. To reduce the channel length or width to 100 nm, a high-resolution lithography such as deep UV stepper or e-beam writer is usually employed [9], [13], at the expense of high cost and/or reduced throughput. In this work, we propose a novel method that simply combines photoresist (PR) trimming and sidewall spacer techniques to fabricate tri-gate poly-Si TETs with greatly shrunk channel dimensions. With only I-line based photolithography, devices of channel length of 120 nm with superior performance are demonstrated.

II. Device Fabrication

Fig. 1 shows the schematic device structures achieved in the main steps for the fabrication of the poly-Si TFTs. The fabrication was carried out on a 6-inch Si wafer capped with a thick thermal oxide to simulate the glass substrate. A 180-nm thick n^+ poly-Si was deposited on the wafer surface by low-pressure chemical vapor deposition (LPCVD), as shown in Fig. 1(a). The layer was then patterned to form two isolated n^+ poly-Si studs using an i-line-based photolithography and subsequent plasma etching, as shown in Fig. 1(b). The minimal distance between the two n^+ poly-Si studs is 0.4 μm. Next, a 150-nm-thick n^+ poly-Si layer was deposited as shown in Fig. 1(c), followed by an anisotropic etching to form the spacer on the sidewall of the poly-Si studs, as shown in Fig. 1(d). This step helps shorten the channel length between the source and drain. The anisotropic etching steps used to pattern the n^+ poly-Si studs and spacers were done in an inductively coupled plasma (ICP) reactor with Cl_2 chemistry. The pressure of the Cl_2 plasma during etching is 10 mtorr.

After the raised S/D regions were formed, a 32 nm-thick amorphous silicon (α-Si) layer was deposited and then treated with a solid-phase crystallization (SPC) process at 600 °C in N_2 ambient for 24 hours to transform the α-Si into poly-Si. Note that this layer serves as the device channel after definition. As shown in Fig. 1(e), a 10-nm-thick oxide layer was next deposited on the wafer to protect the surface of the poly-Si

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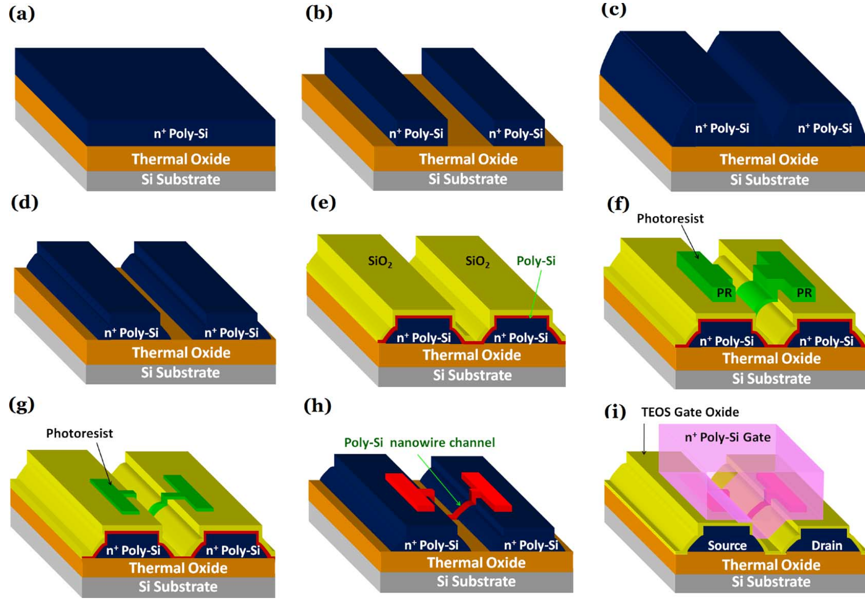


Fig. 1. Schematic device structures achieved in the main fabrication steps of the proposed method. (a) Deposition of an n^+ poly-Si on a Si wafer capped with a thermal oxide. (b) Definition of two isolated n^+ poly-Si studs to serve as the S/D pads. (c) Deposition of the second n^+ poly-Si layer. (d) Formation of the n^+ poly-Si spacers to shorten the distance between source and drain pads. (e) Deposition of the poly-Si channel layer and oxide capping layer. (f) Generation of a dogbone PR pattern connecting between the source and drain pads. (g) Trimming of the PR to narrow down the planar width. (h) Definition of the poly-Si channel and subsequent removal of the capping oxide and PR. (i) Formation of the gate oxide and gate electrode.

layer during a later plasma trimming process. Afterwards, a dog-bone-shaped PR pattern connecting the source and drain pads is generated using an I-line stepper, as shown in Fig. 1(f). In this work, an over exposure condition is intentionally the executed to preliminarily shrink the planar width of the exposed PR patterns. After the development process of photolithography, the PR was then trimmed in a Cl_2/O_2 plasma ambient [Fig. 1(g)]. It should be noted that the planar width of device could be scaled down to around 110 nm with the PR trimming. The poly-Si channel was subsequently defined using an anisotropic dry etching. After removing the remaining PR and the capping oxide, the poly-Si channel was exposed, as shown in Fig. 1(h). Then, a 10 nm-thick gate oxide and a 150 nm-thick n^+ poly-Si layer were deposited. The poly-Si was sequentially patterned to serve as the gate electrode [Fig. 1(i)], and a standard metallization was next performed to complete the device fabrication. For the purpose of comparison, devices of various channel length and width were fabricated.

Fig. 2(a) shows the top view of scanning electron microscopy (SEM) image of a device taken after the poly-Si spacer etching. The measured channel length (the distance between the two adjacent poly-Si spacers) is around 120 nm. Fig. 2(b) is the image after the dogbone-shaped channel formation. Owing to the implementation of the trimming process, the planar portion of the channel is reduced to around 110 nm.

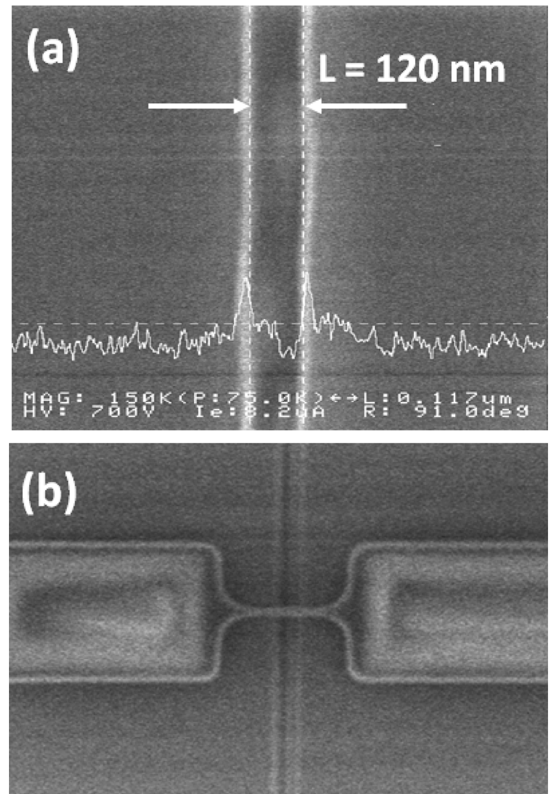


Fig. 2. (a) A SEM picture of a fabricated device taken after the formation of the n^+ poly-Si spacers shows that L as small as 120 nm is achieved. (b) A SEM picture of a fabricated device taken after the formation of the poly-Si channel. The planar width of the device is around 110 nm.

III. Results and Discussion

Transfer characteristics of a fabricated device measured at V_d of 0.1 and 1 V are shown in Fig. 3. Channel length (L) of the device is 120 nm and the planar width is around 110 nm. The effective width, W_{eff}, ($= 2 \times \text{film thickness} + \text{planar width}$) is 174 nm. The threshold voltage (V_{th}), defined as the gate voltage when the drain current reaches $(W/L) \times 10$ nA at $V_d = 0.1$ V, is -0.1 V. Good device performance with high $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio ($2 \times 10^6 @ V_d = 1$ V), low subthreshold swing (SS) (146 mV/dec) and low drain induced barrier lowing (DIBL) (100 mV/V) is exhibited in the figure. The steep SS and small

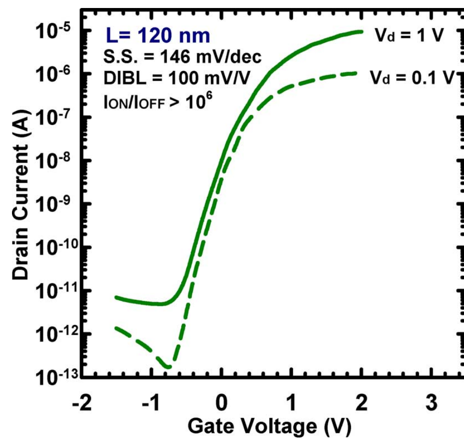


Fig. 3. Transfer characteristics of a fabricated device with L of 120 nm and channel width of 112 nm measured at $V_g = 0.1$ and 1 V.

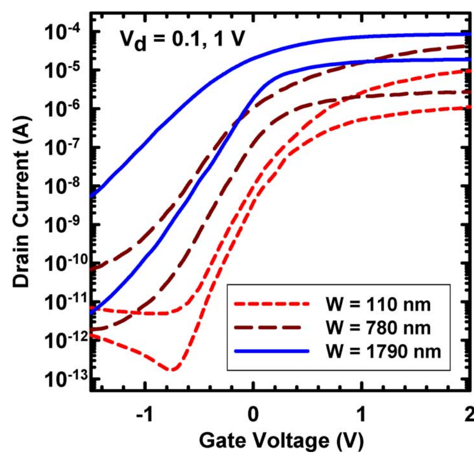


Fig. 4. Transfer characteristics of devices with L of 120 nm and various planar width measured at $V_d = 0.1$ and 1 V.

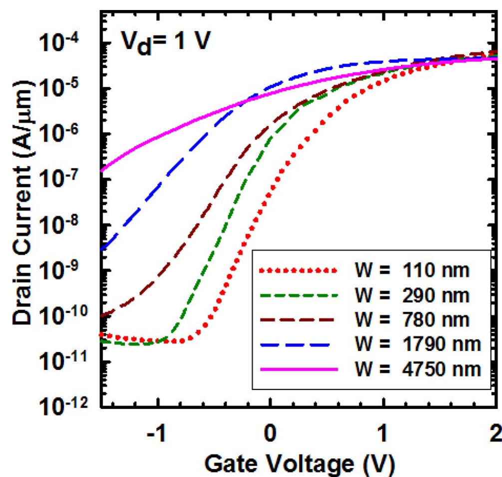
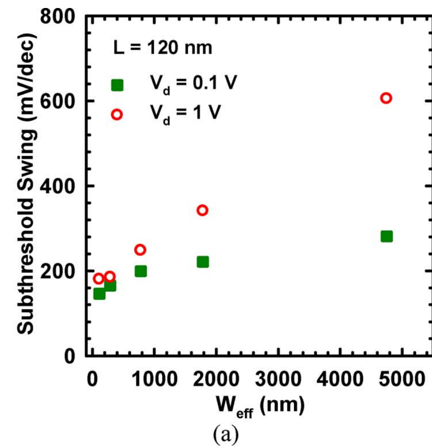
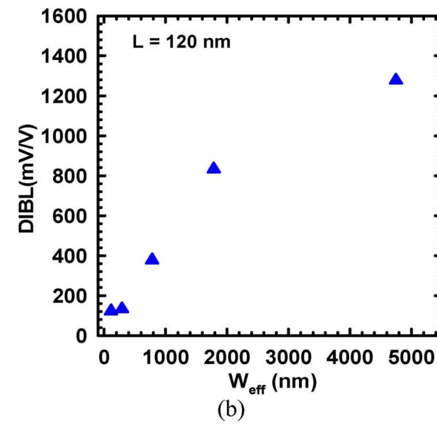


Fig. 5. Transfer characteristics of devices L of 120 nm and various planar width measured at $V_d = 1$ V. The drain current is normalized to W_{eff}.

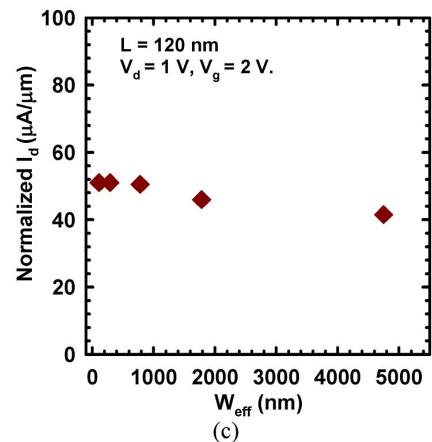
DIBL value could be ascribed to the tri-gated configuration and the reduced channel's cross-section. To illustrate this point, we further compare the device characteristics of devices with same L (120 nm) but various W_{eff} (110, 780, and 1790 nm) in Fig. 4. As can be seen in the figure, reducing the planar channel



(a)



(b)



(c)

Fig. 6. (a) SS, (b) DIBL, and (c) normalized drain current as a function of W_{eff}.

width is very effective in suppressing the SCEs in terms of improved SS and reduced DIBL. To further confirm this point and get more insights into the impacts of channel trimming, we compare the transfer characteristics of five devices with various planar channel widths measured at 1 V, as shown in Fig. 5. Note that in the right figure the drain current has been normalized to W_{eff}. The extracted SS, DIBL and on current (measured at gate voltage of 2 V) are shown as a function of W_{eff} in Fig. 6(a)–(c), respectively. In Fig. 6(a) and (b), it is seen that SS and DIBL are both significantly improved as W_{eff} is decreased. This is ascribed to the suppression of leakage conduction through the film body as the planar channel width is narrowed [7]. In Fig. 6(a) the improvement becomes even

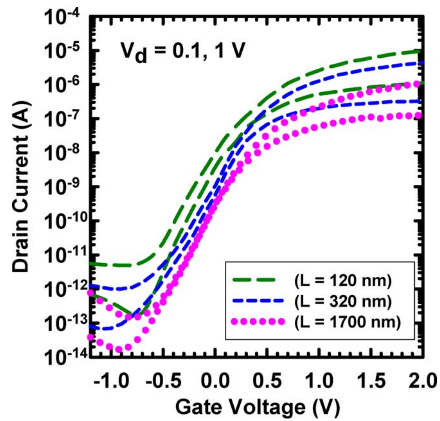


Fig. 7. Transfer characteristics of devices with W_{eff} of 174 nm and various L measured at $V_d = 0.1$ and 1 V.

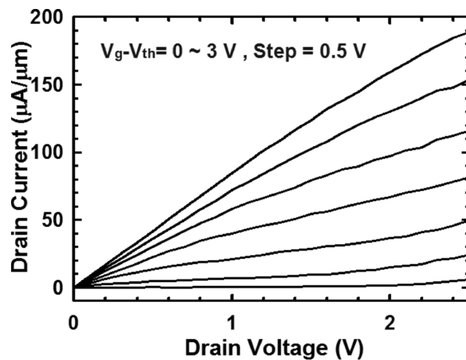


Fig. 8. Output characteristics of devices with W_{eff} of 174 nm and L of 120 nm.

more striking as the drain voltage is increased. This is reasonable since the aforementioned leakage conduction is enhanced with increasing drain bias. On the other hand, in Fig. 6(c) we can see that the normalized drain current (measured at gate $\text{voltage} = 2$ V in Fig. 5) becomes larger as W_{eff} is decreased. Such finding is attributed to the channel corner effect [14], [15]. As the device is turned on, the electric field at the corners of the channel is greatly enhanced owing to the large curvature. As a consequence, the induced carrier concentration is higher therein, so does the local conduction current density. The corner effect becomes significant as the planar width is reduced, the origin for the trend observed in Fig. 6(c).

Transfer characteristics of devices with various L are shown in Fig. 7. Note that the devices are with same W_{eff} of 174 nm. Although a larger DIBL effect occurs to the device with shorter channel length, the devices exhibit comparable SS, indicating that the SCEs are effectively suppressed. The off current increases with reduced channel length. The device characteristics are expected to improve by additional plasma treatment [16]. Fig. 8 shows the output characteristics of the device with L of 120 nm and W_{eff} of 174 nm. The driving current at $V_g - V_{\mathrm{th}} = 2$ V and $V_d = 1$ V reaches 60 μA/μm.

IV. Conclusion

We have proposed and demonstrated a novel method for the fabrication of tri-gate poly-Si TFTs with channel dimensions exceeding the resolution capability of the employed lithographic system. This scheme adopts the sidewall-spacer etching technique to shorten the channel length and the PR trimming technique to shrink the channel width, both below the lithographic limits. With the I-line-based lithography, both channel width and length down to around 110 nm are achieved in this work. Moreover, the fabricated devices exhibit improved performance and suppressed SCEs, thanks to the reduced channel width and the use of tri-gate configuration.

References

[1] S. Uchikoga, "Low-temperature polycrystalline silicon thin-film transistor technologies for system-on-glass displays," *MRS Bull.*, vol. 27, pp. 881–886, Nov. 2002.

[2] W. G. Hawkins, "Polycrystalline-silicon device technology for large-area electronics," *IEEE Trans. Electron Devices*, vol. ED-33, no. 4, pp. 477–481, Apr. 1986.

[3] T. H. Hsu, H. T. Lue, C. C. Hsieh, E. K. Lai, C. P. Lu, S. P. Hong, M. T. Wu, F. Hsu, N. Lien, J. Y. Hsieh, L. W. Yang, T. Yang, K. C. Chen, K. Y. Hsieh, R. Liu, and C. Y. Lu, "Study of sub-30 nm thin film transistor (TFT) charge-trapping (CT) devices for 3D NAND Flash application," in *IEDM Tech. Dig.*, 2009, pp. 629–632.

[4] E. K. Lai, H. T. Lue, Y. H. Hsiao, J. Y. Hsieh, C. P. Lu, S. Y. Wang, L. W. Yang, T. Yang, K. C. Chen, J. Gong, K. Y. Hsieh, R. Liu, and C. Y. Lu, "A multilayer stackable thin-film transistor (TFT) NAND-type flash memory," in *IEDM Tech. Dig.*, 2006, pp. 41–44.

[5] V. Subramanian, "Multiple gate field-effect transistors for future CMOS technologies," *IETE Tech. Rev.*, vol. 27, pp. 446–454, 2010.

[6] M. Masahara, Y. Liu, S. Hosokawa, T. Matsukawa, K. Ishii, H. Tanoue, K. Sakamoto, T. Sekigawa, H. Yamauchi, S. Kanemaru, and E. Suzuki, "Ultrathin channel vertical DG MOSFET fabricated by using ion-bombardment-retarded etching," *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2078–2085, Dec. 2004.

[7] J. T. Park and J. P. Colinge, "Multiple-gate SOI MOSFETs: Device design guidelines," *IEEE Trans. Electron Devices*, vol. 49, no. 12, pp. 2222–2229, Dec. 2002.

[8] B. Doyle, B. Boyanov, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, R. Rios, and R. Chau, "Tri-gate fully-depleted CMOS transistors: Fabrication, design and layout," in *VLSI Symp. Tech. Dig.*, 2003, pp. 133–134.

[9] S. D. Suk, M. Li, Y. Y. Yeoh, K. H. Yeo, J. K. Ha, H. Lim, H. W. Park, D. W. Kim, T. Y. Chung, K. S. Oh, and W. S. Lee, "Characteristics of sub 5 nm tri-Gate nanowire MOSFETs with single and poly-Si channels in SOI structure," in *VLSI Symp. Tech. Dig.*, 2009, pp. 142–143.

[10] W. C. Chen, H. C. Lin, Y. C. Chang, and T. Y. Huang, "Effects of independent double-gated configuration on polycrystalline-Si nonvolatile memory devices," *Appl. Phys. Lett.*, vol. 95, pp. 133502-1–133502-3, 2009.

[11] H. C. Lin and C. J. Su, "High-performance poly-Si nanowire NMOS transistors," *IEEE Trans. Nanotechnol.*, vol. 6, no. 2, pp. 206–212, Mar. 2007.

[12] H. C. Lin, W. C. Chen, C. D. Lin, and T. Y. Huang, "Performance enhancement in double-gated poly-Si nanowire transistors with reduced nanowire channel thickness," *IEEE Trans. Electron Devices*, vol. 30, no. 6, pp. 644–646, Jun. 2009.

[13] C. M. Lee and B. Y. Tsui, "High-performance poly-Si nanowire thin-film transistors using the HfO_2 gate dielectric," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 327–329, Apr. 2011.

[14] H. H. Hsu, H. C. Lin, C. W. Luo, C. J. Sue, and T. Y. Huang, "Impact of multiple-gated configuration on the characteristics of poly-Si nanowire SONOS devices," *IEEE Trans. Electron Devices*, vol. 58, no. 3, pp. 641–649, Mar. 2011.

[15] S. Sato, Y. Lee, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, K. Yamad, and H. Iwai, "Gate semi-around Si nanowire FET fabricated by conventional CMOS process with very high drivability," in *Proc. 40th ESSDERC*, 2010, pp. 14–16.

[16] C. M. Lee and B. Y. Tsui, "A high-performance 30-nm gate-all-around poly-Si nanowire thin-film transistor with NH_3 plasma treatment," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 683–685, Jul. 2010.

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