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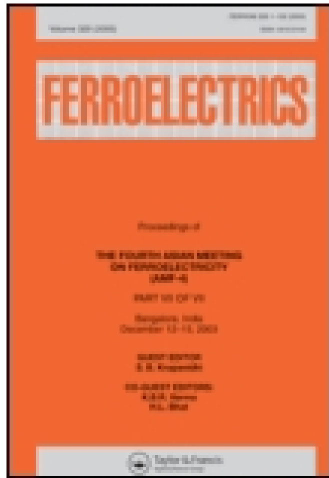

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Perovskite Oxides as Resistive Switching Memories: A Review

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Perovskite Oxides as Resistive Switching Memories: A Review

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Numerous metal-insulator-metal systems demonstrate electrically induced resistive switching effects and have therefore been proposed as the basis for future nonvolatile memories. They combine the advantages of flash memories and dynamic random access memories while avoiding their drawbacks, such as operation speed, power consumption and device integration and scalable issues. The RRAM devices primarily operate at different resistance values to store the digital data and can keep the resistance state without any power supply. Recent advances in the understanding of the resistive switching mechanism are explained by a thermal or electrochemical redox reaction near the interface between the oxide and the top active metal electrode. Here we review the ongoing research and development activities on the perovskite based resistive switching memory devices. The possible switching mechanisms for the resistive switching are described. The effects of crystal structure, dopants, doping concentrations, annealing temperature, device structures and thickness of the active oxide layer on the resistive switching characteristics and consequently the memory performances are also discussed. From this insight, we take a brief look into different effect on the switching of the perovskite material systems.

Keywords Perovskite oxides; resistive switching memory (RRAM); nonvolatile memory; metal-insulator-metal; current-voltage

1. Introduction

Novel memory technologies with scaled transistors, switching speed, low power consumption, flexible and nonvolatile nature are desirable for electronic systems. Nonvolatile memory that permanently stores data is requisite for computers and portable gadgets. Various kinds of nonvolatile memory (NVM) devices have emerged over the last few decades, although each has some technical limits, such as switching power, retentivity, scalability and reliability aspects [1–25]. To overcome such constraints, resistive switching memory device [7–40], is one of the promising candidates for future nanoscale memories. Such class of switching devices are conductive bridge RAM (CBRAM) [21] and resistive random access memory (RRAM) [23–47], might be replace flash RAM in USB drives and other portable gadgets in near future. The memristor was first proposed as a fourth fundamental component on the electronic circuit by L. Chua at 1970 [7] like capacitor, resistance and

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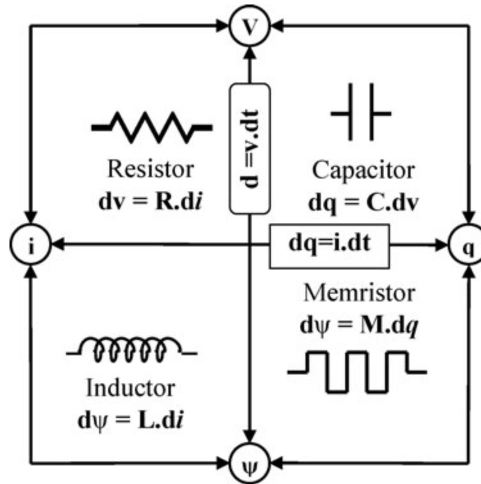

Figure 1. The four basic circuit elements and their properties [after ref. 43].

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inductor, as shown in Fig. 1. Chua described a generalized flux ‘Ψ’ as the time integral of voltage ‘V(t)’ and related this to the charge ‘q’ as time integral of current ‘I(t)’. If the resistance representing the ratio V/I depends on the charge ‘q(t)’ passed through the device, it becomes a memristance ‘M(q(t))’ according to V(t) = Mq(t)/t. In this case, the RRAM or resistive switching memory shows hysteretic behavior which can be exploited as nonvolatile RRAM cells. The interesting link between the theoretical concept of Chua and the body of literature on resistive switching memory cells was first pointed out by Stanley Williams group of HP laboratory [8].

RRAM provides a combination of longer lifetime, lower power, and higher memory density. In contrast to flash, RRAM writes with relatively low power and at high speed. Additionally, the writing process is ‘almost infinitely reversible’ [48], making such devices much more universally applicable than flash. Resistive switching memory, in theory, can scale to sizes much smaller than flash, as small as a few ion widths wide. Metal ions or filaments are about a fraction of angstroms, so the line widths of the order of nanometers seem possible. It was reported that the RRAM exhibits lower programming currents than phase change RAM (PRAM) or magnetic RAM (MRAM) without sacrificing programming performance, retention or endurance [41–50]. RRAM device has the expected advantages of nonvolatility, fast programming, small bit cell size and low power consumption. RRAM is a realistic and prospective alternative because of its simple memory cell structure, low fabrication-process temperature, and appropriate scalability due to filamentary conductive path mechanism in the oxide film. Compared to the flash and racetrack memory, a lower voltage is sufficient and hence RRAM can be used in low power applications. Chen et al. has recently shown that RRAM is scalable below 30 nm [38]. The motion of oxygen vacancy or oxygen ion is a key phenomenon for oxide-based resistive switching memory. Cen et al. [39] reported that the oxygen motion may takes place in regions as small as 2 nm. It is believed that if a filament is responsible, it would not exhibit direct scaling with cell size [51]. Instead, the current compliance limit (set by an outside resistor, for example) could describe the current-carrying capacity of the filament.

Based on the circuit necessities of the today’s high-density NVM such as flash and by taking the predictions about technology scaling of the next 15 years into account [10–50], one can bring together a number of requirements for RRAM cells [10–50]:

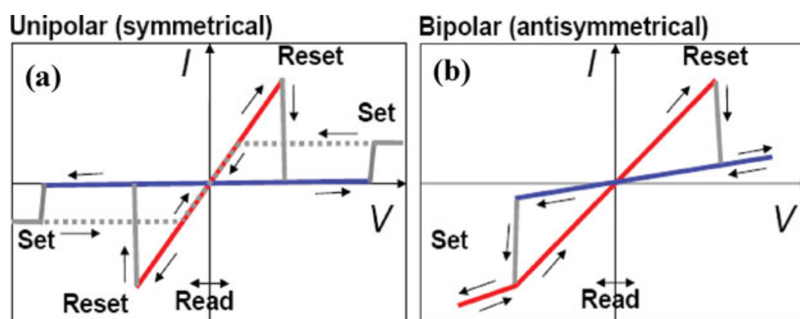

Figure 2. Two basic I–V operation of the resistive switching memory cell (a) unipolar and (b) bipolar switching [after ref. 48, 51, 52].

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Write operation: Write voltages (V_{wr}) should be in the range of a few hundred mV to be compatible with scaled CMOS to a few V, to provide an advantage over flash, which suffers from the high programming voltages. The length of V_{wr} pulses is desired to be $<$100 ns in order to contend with DRAM specifications and to outperform flash (with time programming speed 10 ms) or even $<$10 ns to compete with high-performance SRAM.

Read operation: Read voltages (V_{rd}) need to be significantly smaller than write voltages in order to prevent a change of the resistance during the read operation. Because of the constraints of circuit design, V_{rd} cannot be less than approximately one tenth of V_{wr}. An additional requirement originates from the minimum read current I_{rd}. In the ON-state, I_{rd} should not be less than approximately 1mA to allow for a fast detection of the state by reasonably small sense amplifiers. The read time t_{rd} must be in the order of t_{wr} or preferably shorter.

Resistance ratio: Although an R_{OFF} /R_{ON} ratio of only 1.2 to 1.3 can be utilized by in the circuit design as shown in MRAM, R_{OFF} /R_{ON} ratios $>$10 are required to allow for small and highly efficient sense amplifiers and, hence, RRAM devices are cost competitive with flash.

Endurance: Contemporary flash shows a maximum number of write cycles between 10^3 and 10^7, depending on the type. RRAM should provide at least the same endurance, preferably a better one.

Retention: A data retention time t_{ret} of $>$10 years is required for the universal NVM. This retention time must be kept at thermal stress up to 85°C and small electrical stress such as a constant stream of read voltage pulses.

1.1. Resistive Switching Model

Figure 2 shows the typical current-voltage (I–V) characteristics of a RRAM device. There exist two types of switching memory associated with the electrical polarity requisite for the switching properties. When the resistance change does not depend on the polarity of the applied voltage or current and the device can be switched between the two resistance states i.e. high resistance state (HRS) and low resistance state (LRS) within the same polarity, such polarity independent switching behaviour is called unipolar switching. The second scheme is called bipolar switching because, opposite polarity of the applied voltage is needed to switch between the HRS and LRS.

Figure 3(a), (b), (c) and (d) describes the schematic diagrams of the possible state of the memory during the positive half-cycle when $V_m < V_T^{ON}$, $V_m > V_T^{ON}$ and their corresponding

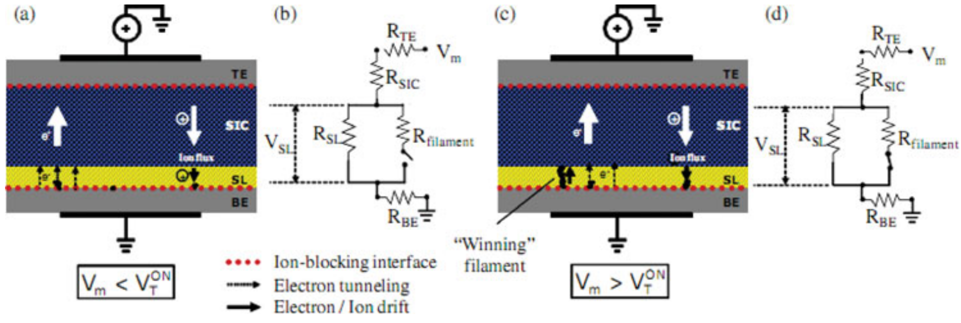

Figure 3. Schematic diagrams of the possible state of the memory during the positive half-cycle when (a) $V_m < V_T^{ON}$, (b) $V_m > V_T^{ON}$. (c) & (d) are circuit representations showing the memory in the OFF and ON states respectively. The size of the filament has been exaggerated by orders of magnitude; the sizes are also not to scale [after ref. 52].

circuit representations showing the memory in the OFF and ON states, respectively. To explain the external I–V characteristics of a RRAM, we refer to Figs. 3(b) and 3(d), where the electrical resistances of the various layers contributing to the total resistance of the memory structure are represented in the simple electrical equivalent circuit form. During either ON or OFF state, the resistances of the top electrode (R_{TE}), bottom electrode (R_{BE}), and the solid ionic conductor (R_{SIC}) remain constant. The resistance switching phenomena in the memory are therefore limited to the switching layer itself.

On the other hand, the total resistance of the switching layer can be written as the sum of two parallel resistances [48], can be written as,

$$R_{Tot}^{SL} = \frac{1}{\frac{1}{R_{SL}} + \frac{1}{R_{Fil}}} \tag{1}$$

R_{SL} is the Ohmic resistance of the switching layer (SL) which depends on its physical geometry and the intrinsic resistivity and R_{Fil} is the total resistance of the complete filaments connected between two electrodes. The switching mechanisms are predicted to depend on the filamentary conduction. In the OFF state, since there are no complete filaments bridging formed on the SL, $R_{Fil} >> R_{SL}$. Therefore, the total resistance of the memory device at OFF state can be approximated as $R_{Tot,\ OFF\ state}^{SL} = R_{SL} = R_{OFF}$; In the ON state, when one or more complete filament(s) bridge the SL, the filament resistance plays a crucial role because $R_{Fil} << R_{SL}$. Therefore, the total resistance of the switching layer in the ON state can be written as $R_{Tot,\ ON\ state}^{SL} = R_{Fil} = R_{ON}$. Furthermore, since $R_{Fil} << R_{SL}$ in general, $R_{OFF} >> R_{ON}$ and hence the two states are defined as the HRS and LRS state, respectively [48].

1.2. *Switching Mechanisms*

A large variety of physical phenomena are known, which can, in principle, lead to non-volatile resistive switching memory effects (Fig. 4). The actual physical driving force for the resistance switching is quite different, although in all cases electrically induced. In the nano-mechanical memory effects, mechanical forces can be utilized. A change in the molecular configuration may lead to a resistive memory behaviour of a single molecule for the molecular switching effect [52]. Electrostatic and electronic effects are also possible

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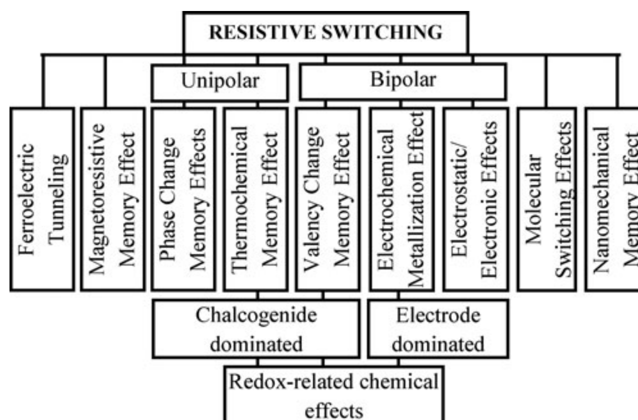

Figure 4. Classifications of different resistive switching effects considered for the nonvolatile memory applications.

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origins of resistive switching. The direction of a ferroelectric or a ferromagnetic domain polarization may lead to different tunnel currents [53, 54]. The temperature induced change between a crystalline phase (ON-state) and an amorphous phase (OFF-state) in dedicated tellurides and selenides is exploited in phase change memories (PCM) [11]. There are three other classes which involve chemical effects, i.e., effects which relate to redox processes in the MIM cell either triggered by a temperature or electrical voltage or both. Firstly, the bipolar electrochemical metallization mechanism (ECM) relies on an electrochemically active electrode metal such as Ag, the drift of the highly mobile Ag^+ cations in the ion conducting 'I' layer, their discharge at the (inert) counter electrode leading to the growth of Ag dendrites, which form a highly conductive filament in the ON state of the cell [48]. Upon reversal of the polarity of the applied voltage, an electrochemical dissolution of these filaments takes place, resetting the system into the OFF state. Secondly, the valence change mechanism (VCM) occurs in the specific transition metal oxides (TMO) which is triggered by a migration of anions, such as oxygen anions (which are typically described by the motion of the corresponding vacancies, i.e., oxygen vacancies) [48–58]. A subsequent change of the stoichiometry leads to a redox reaction expressed by a valence change of the cation sublattice and a change in the electronic conductivity. This bipolar memory switching is induced by voltage pulses, where the polarity of the pulse determines the direction of the change, i.e., reduction or oxidation. A third class relies on a thermo-chemical mechanism (TCM) which leads to a change of stoichiometry due to a current-induced increase of the temperature [10, 48].

The switching mechanisms in the high-k oxide, such as, ZrO_2, devices have been proposed schematically in Fig. 5. During forming process, the conducting filaments are formed using oxygen vacancies instead of metal ions and the device is switched to LRS. The local electric field enhancement provides to easily form localized path at on state, as shown in Fig. 5(a) [12]. The device switch to HRS by applying a negative bias on the top electrode due to that the O^{2-} ion drifts from the interfacial layer between the top electrode and resistive switching material (ZrO_2), as shown in Fig. 5(b). The films re-oxidize the region beneath the interfacial layer at the top electrode side by the assistance of the local Joule heating. An external defects were created due to the local electric field enhancement and line up to form the conducting filaments again, during negative bias set process, as

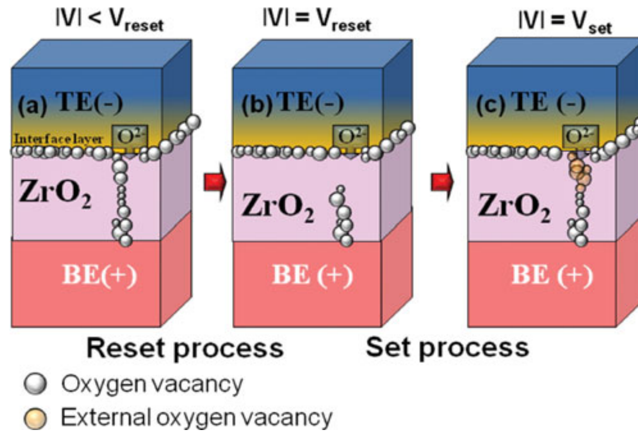

Figure 5. Schematic structure for the resistive switching mechanism in high-k ZrO_2 film.

shown in Fig. 5(c). It was reported that the switching mechanism on perovskite materials are also similar like high-k oxides.

1.3. Resistive Switching Materials

Before realizing rapidly growing interest RRAM device in the future NVM practical applications, there are still several issues including reliability, performance, and device yield need to be solved. Resistive switching characteristics have been demonstrated in a variety of materials including binary metal oxides such as TiO_2, ZnO, ZrO_2, Ta_2O_5, CuO, NiO and WO_x; chalcogenide materials such as Ag doped GeSe, Ag doped AgS etc.; and perovskite oxides such as $SrZrO_3$ (SZO), $Pr_{0.7}Ca_{0.3}MnO_3$, STO etc. [8–82]. Current-voltage (I–V) characteristics of MIM structures using above materials exhibit a huge resistance change between high resistance state (HRS) and low resistance state (LRS), appropriate for binary logic devices. Among the varieties of materials, the perovskite oxides proved enormous attention for this application in the last decade. Lee *et al.* demonstrated that the oxides with dopants had higher device yield than the non-stoichiometric oxides, such as Nb_2O_{5-x}, ZrO_x, and $SrTiO_x$ (STO) [73]. Reproducible resistive switching behaviors have been observed in doped perovskite oxide films, such as Cr-doped $SrZrO_3$ (Cr:SZO) [72, 74–76], Cr-doped $SrTiO_3$ (Cr:STO) [77], Nb-doped $SrTiO_3$ (Nb:STO) [78–79], and V-doped $SrZrO_3$ (V:SZO) films [64, 68–71, 80].

It is reported that the resistive switching (RS) behaviors could be associated with the metallic defects [82–84], oxygen vacancies [82–89], and dislocations [90, 91] in the oxide based resistive thin films. As a result, controlling the distribution and content of these defects plays a crucial role in solving current issues such as the dispersion of RS parameters, device yield, and reliability in forward-moving research of RRAM. Several techniques including active top electrode (TE) [92–94], metal doping into oxides [82, 84, 95–99], Zr^+ implantation [72], IrO_2 buffer layer [85], and embedded metal technology [83, 87], have been employed in the fabrication of the resistive switching memory devices.

Perovskite material is studied by several groups for its versatile applications in DRAM and also RRAM [100–120]. $SrZrO_3$ (SZO) based perovskite oxides thin films have been studied for several years because of the interest for its versatile properties such as, high-temperature protonic conductivity [100, 101], promising use in MHD generators [102],

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suitable for high-voltage and high-reliability capacitor applications, used as high-*K* gate dielectrics [100, 103]. Another alternative and important application of SZO thin films is for the nonvolatile memory application as a resistive switching memory. A previous study proved that $SrZrO_3$ (SZO) based RRAM exhibited lower forming voltage and lower set voltage than those of the vanadium-doped SZO thin films, however, the large dispersion of RS parameters and the low device yield in SZO thin films limit their development in realizing the practical NVM application. $SrTiO_3$ (SRO) and $SrTiO_3$ (STO) thin films can also be used for RRAM applications [104–105].

Perovskite manganites $ReAMnO_3$ (Re = rare earth ions, A = alkaline ions), have attracted immense intention, due to their unusual electronic and magnetic properties, such as colossal magnetoresistance (CMR) and colossal electroresistance (CER) effects. Among the various CMR manganites, $Pr_{1-x}Ca_xMnO_3$ (PCMO) attracts considerable attention because PCMO films show an electric-pulse-induced resistance (EPIR) changes effect under electric field pulse without any applied magnetic field at room temperature [83]. The EPIR effect is pulse polarity dependent and reversible, which is essential for its easy fabrication, fast switching speed ($<$100 ns), high density, and low power application [85].

Several groups have studied the resistive switching properties of PCMO films [106–110], using different bottom electrode (BE) and top electrode (TE). Liu et al. prepared $Pr_{0.7}Ca_{0.3}MnO_3$ film by pulsed laser deposition (PLD) on $LaAlO_3$ substrates and observed a new EPIR change effect in the CMR oxide at room temperature and under zero magnetic field [83]. It was found that the resistance of PCMO film (thickness $\sim$600 nm) could either be decreased or increased (more than 1700%) according to the pulse polarity (above a threshold voltage $\sim$5 Volt). Several groups studied the EPIR and CMR effect in PCMO films using different electrodes. PCMO films were mostly deposited by pulse laser deposition (PLD) to maintain the near stoichiometric of the complex oxide films [86]. Rather than PLD, sputtering has also used to study the resistive switching properties of the PCMO based resistive switching structures [87].

1.4. Factors That Are Influences on Resistance Switching Properties

The different factors are influences on the resistive switching properties of perovskite oxide based memory structures. The mostly reportable factors are (1) crystal structure, (2) deposition techniques, (3) different dopants, (4) doping concentrations, and (5) device structures. Here we will discuss briefly about the role of those factors on resistive switching properties of perovskite oxide based RRAM structures.

In this article we reviewed the process and electrical characteristics of some promising perovskite oxides materials such as doped strontium zirconates $SrZrO_3$ (SZO), doped strontium titanates $SrTiO_3$ (STO) and $Pr_{1-x}Ca_xMnO_3$ manganites (PCMO) etc. for RRAM applications. The influences on resistive switching properties of those perovskite oxides films from the some important published papers are reviewed.

2. Resistive Switching of $SrZrO_3$ Film

2.1. Crystal Structures

The resistive switching properties of perovskite structures are strongly affected on the crystal structures of the films. Liu *et al.* [68], reported about the effect of crystal structure on resistive switching properties of vanadium doped SZO films by using $LaNiO_3$ (LNO)

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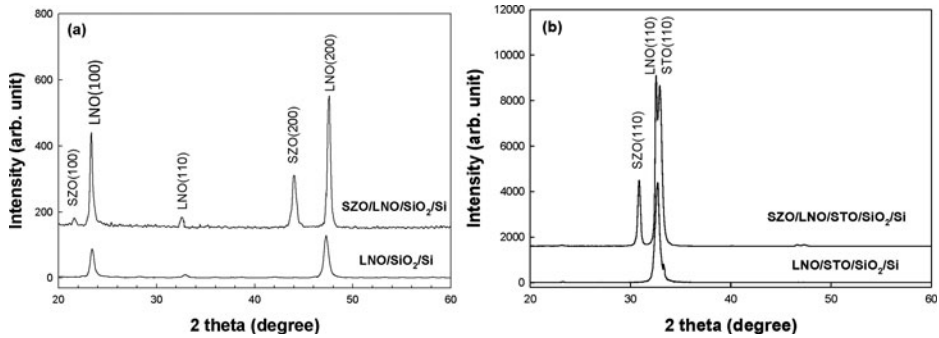

Figure 6. XRD patterns of (a) LNO/SiO_2/Si and SZO/LNO/SiO_2/Si structure, (b) LNO/STO/SiO_2/Si and SZO/LNO/STO/SiO_2/Si structure [after ref. 69].

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bottom electrode and Al top electrode respectively. To vary the crystal structure of the V doped SZO films, the different oriented LNO bottom electrodes had been used by introducing $SrTiO_3$ (STO) buffer layer. Prior to LNO deposition, a thin STO layer was sputtered on the SiO_2/Si substrate to form a [110] orientated LNO bottom electrode. [200] oriented LNO films were obtained by sputtering on simple SiO_2/Si substrate. The rf sputtered V:SZO films was deposited on [110] and [200] oriented LNO bottom electrodes were used as a active element.

Figure 6(a) depicts the XRD patterns of the V-doped SZO films having thickness of 90 nm on two different textured LNO bottom electrodes. Fig. 6(a) shows the LNO film on SiO_2/Si and SZO film on this LNO/SiO_2/Si substrate had [200] preferred orientation. However, it is difficult to deposit a [110] orientated LNO film directly on a SiO_2/Si substrate by sputtering. So, prior to LNO deposition, a [110] orientated STO film was grown on the SiO_2/Si substrate at 550°C as a template layer. As can be seen from the Fig. 6(b), both the LNO and SZO films are [110] orientated.

The electrical current-voltage characteristics of the [200] and [110] orientated V-doped SZO films (thickness 90 nm) are shown in Fig. 7(a). As can seen from the figure, [200] orientated device have the lowest leakage current density at original state (shown in Fig. 7(d)). The switching voltage should be related to the crystallinity of the resistive film. The polarity direction of the resistive transition is an intrinsic property for the device. The device is set, by switching from low leakage-state to high leakage-state by applying an appropriate negative voltage (-13 Volt). By applying appropriate positive voltage (8 Volt) the device is reset and switched to the low leakage-state. The entire devices are shows bipolar switching properties. The resistance ratio between the two leakage-states decreases with increasing the bias voltage in the both directions (inset of Fig. 7(a)), due to the different conduction mechanisms of the two leakage-states [69, 72]. The resistance ratio is more than 3 orders of magnitude under low voltage and about 10^2 times at 5 Volt. The asymmetric switching voltage is observed due to the asymmetric interfaces of SZO film with top and bottom electrodes. Resistance switching behavior of the [200] orientated device is similar with the [110] orientated device having higher resistance ratio and stable than the former one. Fig. 7(b) depicts the I–V characteristics of the V:SZO based MIM device (thickness 45 nm) on (100) $LaNiO_3$ bottom electrodes. The devices switch ON or set at -13 Volt and turn OFF at $\sim$12.6 Volt after passing a negative differential resistance (NDR) transition region. Ratio of the two resistance states is more than 10^3 times at low voltage, having resistances of H-state and L-state are 10 kΩ and 100 MΩ at -1 Volt,

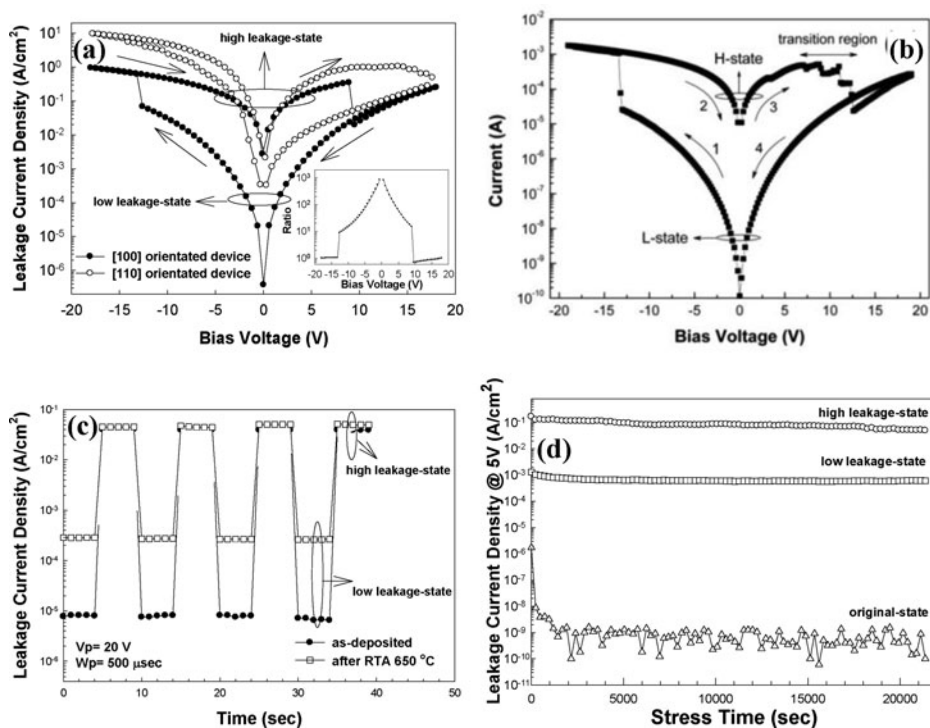

Figure 7. Plots of leakage current density versus bias voltage of the (a) [200] orientated device and the [110] orientated device having V-doped SZO film having 90 nm thickness [After ref.69], (b) [200] orientated device V:SZO device having thickness 45 nm [After ref. 68], (c) The influence of thermal treatment on the resistance switching property of the [200] orientated devices and (d) plots of leakage current density versus stress time at different leakage-states [After ref. 69]. Inset of (a) is the plot of resistance ratio versus bias voltage of the [200] orientated device [after ref. 69].

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respectively. The polarity direction of the resistive switching of SZO oxide is an intrinsic property. This resistive switching cycle can be traced and reproduced more than 10^2 times. During the set process, the biased electrons formed conduction paths consisted of probable point defects, such as oxygen vacancies ($V_O^{\bullet}$, $V_O^{\bullet\bullet}$) and ionic and electronic defects associated with Zr replacing by V ($V_{Zr}^{\bullet}$, e^-). Concurrently the electrons hopped passing through the V:SZO film and the current is dramatically increased in those paths. As a result, the resistive switching mechanism during set process was considered as the formation of current paths [68, 75]. At later sections we will discuss more details about the switching mechanisms.

Figure 7(c) shows the change of leakage current density with time for the [200] orientated device having thickness 90 nm. The devices were read at 1.2 Volt as varied with different voltage pulses. The annealed samples (RTA at 650°C in O_2, for 1 min) shows lowest resistance ratio than the as-deposited one. The leakage current density of high leakage-state was changed to the low leakage-state after applying a +20 Volt, 500 μs voltage pulse and it is changed to the high leakage-state again by applying −20 Volt, 500 μs pulse width. The resistance ratio of the two leakage states is more than 3 orders of magnitude for the as-deposited samples. The write-read-erase-read sequence can be repeated and the leakage-state would not be altered by read bias voltages. The resistance ratio is decreases

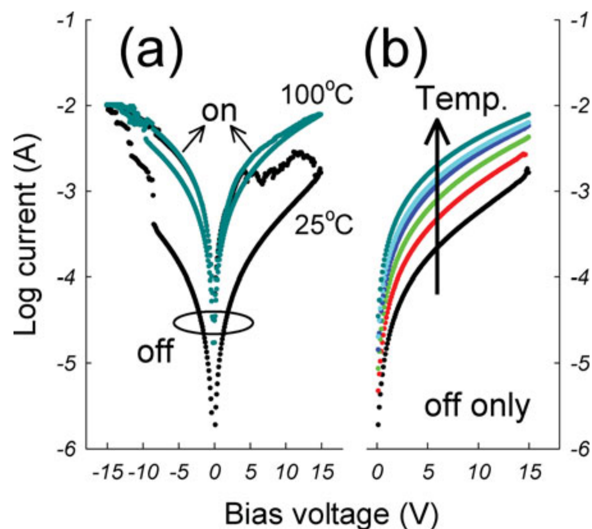

Figure 8. (a) Typical *I–V* for V:SZO, only those at 25°C and 100°C shown to clearly reveal the temperature immunity of on-state conduction, (b) the dependence of off-state current at positive bias on temperature from 25°C∼100°C [after ref. 60].

after annealing, though the static I–V characteristics are almost same with the as-deposited samples except the leakage current densities of two leakage-states increased a little. This can be explained by the unusual conduction mechanisms of the two resistance states. The leakage current density at high leakage-state obeyed Ohmic conduction mechanisms and whereas the P-F emission mechanisms followed at low leakage-state [68, 75]. For pulse operation, the leakage current densities are very sensitive to pulse width [68, 122]. Fig. 7(d) shows the plot of current density at different states (stressed at 5 Volt) versus stress time, which indicates that the leakage current densities of all leakage-states are almost constant. A higher current density of the original-state observes in beginning, then after a short time its decreases to reach equilibrium current density, due to relaxation behaviour.

Lai *et al.* [60], reported the effect of annealing temperature on resistive switching properties of the sputtered 0.2 at% V-doped SZO [200] device having thickness 50 nm. LNO an Al were used as a bottom and top electrode respectively. Fig. 8(a) shows a pronounced hysteretic *I–V* characteristic with two different conduction states measured at 25°C and 100°C. The main variations of currents at different temperatures founds in the off-state currents, though the on-state currents are almost fixed with enhanced immunity to thermal disturbance, as shown in Fig. 8(a). To stress the prevailing effect at the off-state conduction on the switching ratio, this is highlighted in the temperature dependence I–V curve at OFF states, as shown in Fig. 8(b). Speculatively the carrier transport in off-state is dominated by some kind of charge trap in the bulk. The frequently observed *I–V* jiggle during positive sweep ON to OFF transition at 25°C also implies the more stable conduction nature in ON state. Rohde et al. reported that the required power is a most dominant parameter to obtained good switching [60, 123]. It was estimated from the current levels at OFF and ON states near the switching voltage in Fig. 8(a) and with the same pulse amplitude V_p, it has lower power $P = i \times V_p$ and therefore the significantly less energy $E = P \times \Delta t$ required for the OFF to ON state transition compared with that for ON to OFF state transition. The relative stability between two states was also found in other RRAM structures. Sawa *et al.*

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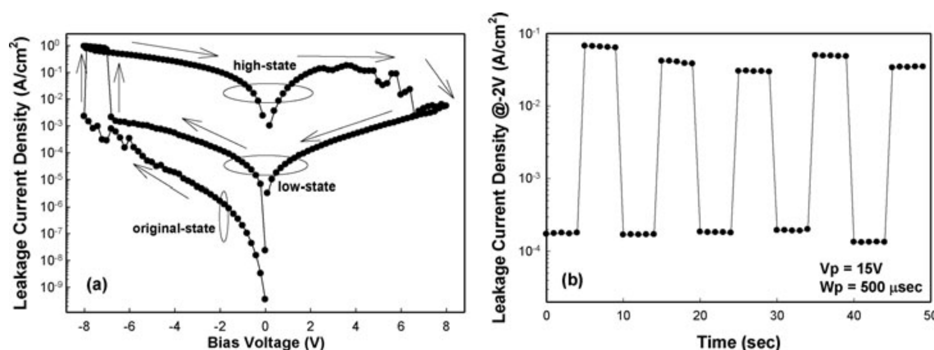

Figure 9. Plot of leakage current density of the 400°C annealed sol-gel derived V:SZO film (a) with the bias voltage and (b) as a function of time operated by the voltage pulse [after ref. 71].

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[60, 90] reported that the OFF state is much more stable than the ON state for the device having PCMO as an active layer.

2.2. Effect of Deposition Techniques

The dependence of the oxide films are strongly influences the resistive switching properties of the perovskite oxide films. Radio frequency (rf) magnetron sputtering, and sol-gel techniques are mostly used to synthesize SZO films for switching memory fabrications. In the previous sections we had studied the resistive switching properties of the sputtered deposited V doped SZO films.

Liu et al., reported about the resistance switching mechanisms of perovskite structured $SrZrO_3$ (SZO) film fabricated by sol-gel route. 100 nm thick sputtered $LaNiO_3$ (LNO) film on SiO_2/Si substrate was used as a bottom electrode [66, 69]. The 0.1 M SZO precursor solution with 0.2 mol% vanadium (V) dopant was spin-coated on the $LaNiO_3/SiO_2$/Si substrates to obtain the ~50 nm thick active oxide films [66, 69, 71]. Aluminum top electrode (area 2.86×10^{-4} cm^2) was evaporated on it to form the metal/ insulator/ metal (MIM) structure.

Figure 9(a) shows the plot of leakage current density with respect to bias voltage of the 400°C annealed vanadium doped SZO based MIM device [71] prepared by sol-gel method. The first switching is known as forming process, which needs larger switching voltage than the set voltage. Prior to forming process, the resistance switching property will be destroyed by adding a large positive voltage on the device. Before any change in resistance state, the leakage current density increases with the increasing of bias voltage, which is defined as virgin state. When negative voltage is higher than −8 Volt (forming voltage), leakage current density increases abruptly from its virgin state to the high current state (high-state). The positive bias of more than +6 Volt is applied to reset the device to low current state (low-state). However, leakage current density at low-state is larger than that of the original-state. While the higher negative voltage of ~ −7 Volt is applied, the leakage current density is changed from the low-state to the high-state again. The sequence of resistance switching would be reversibly changed between high current state and low-state, but never back to the original-state with high resistance ratio is about 3 orders of magnitude. The device switched between two states by applying ±15 Volt, 500 μs voltage pulse respectively as shown in Fig. 9(b). The polarity of resistance change is same as like bias voltage sweeping with almost same switching ratio. Fig. 10(a) shows the plots of leakage current density

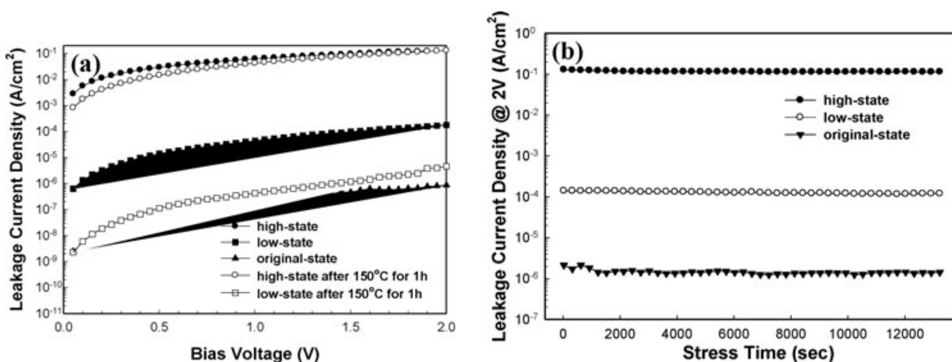

Figure 10. (a) Plots of leakage current density with the applied bias voltage of original-state, low-state, and high-state at room temperature and after heating at 150°C for 1 h during measurement and (b) plots of leakage current density with time after 2 Volt applied stress [after ref. 71].

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with the applied bias at different states and those after thermal acceleration testing. After thermal acceleration, the leakage current density of high-state was decreased a little and still very close to the previous one. Whereas the leakage current density at low-state after thermal acceleration was decreased largely and close to the leakage current density of original-state. The phenomenon of retention behavior of this device is not similar to the ferroelectric materials, as shown in Fig. 10(b). A 2 V voltage bias for more than 3 h was applied to the device before test. The leakage current density of different states does not change, indicating that, voltage stress would not disturb the memory state and the device has non-destructive readout property.

2.3. *Effect of Different Dopants*

In this section we will discuss about the effect of different metal doping in the SZO films. Dopants are of critical importance in semiconductor devices. Small amounts of dopants that act as donors or acceptors are introduced into the semiconductor crystal lattice to effect a considerable change at electronic properties of semiconductor. In the previous sections we studied about the resistive switching properties of the V doped SZO films. The different dopants can significantly affect on the oxygen vacancies and defect levels in the switching perovskite layers. As a result the switching properties are affected. The set and reset voltage for the 0.2 mol% V-doped SZO film is found to be −7 Volt and 6 Volt respectively.

2.3.1. Effect of V and Tm co-doping on sol-gel derived $SrZrO_3$ film. Liu *et al.* [66], reported about the resistance switching mechanisms of vanadium (V) and thulium (Tm) co-doped $SrZrO_3$ (SZO) film fabricated by sol-gel technique using [200] oriented LNO bottom electrode and Al top electrode, as used before. Fig. 11(a) show the plot of leakage current density with voltage for this sol gel derived V and Tm doped SZO (V:Tm:SZO) based MIM capacitors. Initially, the leakage current density increases with increasing bias voltage, which is defined as the original state. While the negative bias voltage is higher than −12 Volt applied on TE, the leakage current density increases abruptly to higher value, which is defined as the high leakage-state (H-state). After the forming process, while the positive bias voltage is higher than 10 Volt applied at the TE, the leakage current density drops abruptly to low leakage-state (L-state). After that, while the voltage is higher than

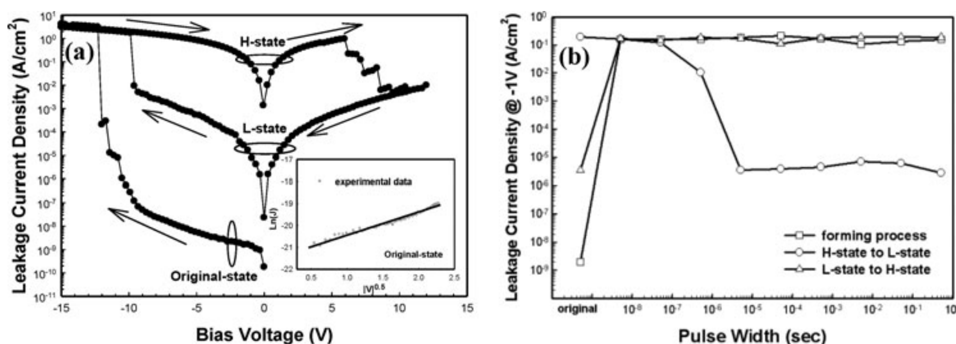

Figure 11. (a) Current voltage characteristics of the Al/(V:Tm:SZO)/LNO structure. Inset shows the comparison between Schottky emission model and experimental data of original-state under the negative bias voltages and (b) the plot of leakage current density with pulse width [after ref. 66].

-10 Volt, the leakage current density increases abruptly to that of H-state again. Resistance of the device is switched between H-state and L-state and is never switched back to the original-state during the electrical operation. The leakage-states are not changed without power supply and the resistance ratio between two states is $\sim 10^4$. The process from change of two resistance states is believed to cause the formation and ruptures of the conducting paths or conducting filaments [55–81]. In the region from 6 Volt to 10 Volt, the process from H-state to L-state occur the uneven switching property. The conducting paths are randomly broken while the positive bias is applied, which leads to the leakage current decreased. In the region from 6 Volt to 10 Volt, the conducting paths are randomly ruptured and some new filaments are formed temporarily. While the applied voltage is larger than 10 volt, all conducting paths are ruptured and the leakage-state is return to the stable L-state. Therefore, the uneven switching property observes during H-state to L-state transition [68]. The forming voltage as well as set/ reset voltages are quite larger compare to the only V-doped SZO film, as stated in the previous section. Inset of Fig. 11(a) shows the plot of $Ln(J)$ versus $V^{1/2}$, solid line shows the fitted experimental data, which corresponds to the Schottky emission mode responsible for original state [19]. The conduction mechanisms of H-state and L-state were reported to be Ohmic conduction and Poole-Frenkel (PF) emission, respectively [72]. The mechanism of resistance switching is not clear. The reproducible resistance switching observed due to the formation of conducting filament which consists of metallic elements. After adding an appropriate negative bias on the device, the metallic elements would form conducting filaments as the conducting paths and the leakage-state was changed to H-state. The conducting paths were ruptured and the leakage-state was changed to L-state again, after applying an appropriate positive bias on the device. So, it is observed that after V and TM doping the operational voltage of this doped SZO structured are increased.

Figure 11(b) depicts the effect of the pulse width with 15 Volt pulse amplitude on the resistance switching. When a -15 Volt with 5 ns voltage pulse is added, the device is changed from original-state to H-state, indicating that the forming process is completed within 5 ns. Before measuring the switching times form H- to L-state or vice versa, the leakage-states were set to H- and L-state by applying negative and positive dc voltages, respectively. The H-state is changed to L-state after applying a 15 Volt, 5 μs voltage pulse, representing that the switching time is between 500 ns and 5 μs. However, prior to the abrupt resistance switching, the current density of H-state gradually decreases with increasing

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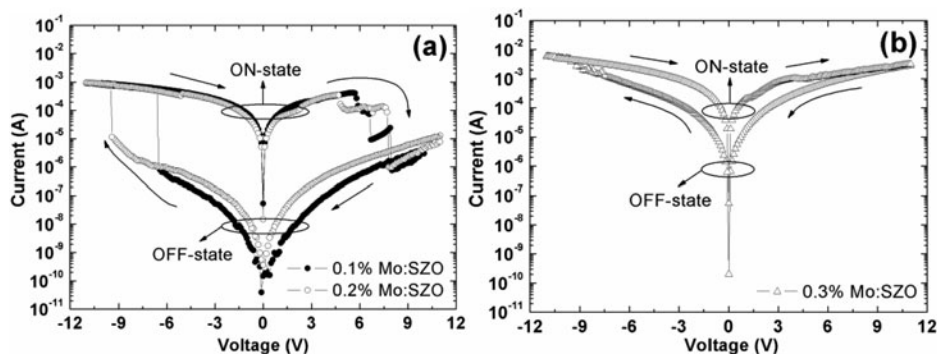

Figure 12. I–V curves of various 0.1, 0.2, 0.3% Mo doping SZO-based memory devices [after ref. 66].

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the pulse width. On the other hand, the L-state is changed to H-state while a −15 Volt, 5 ns voltage pulse is added. Switching time from H-state to L-state is much larger than that of L-state to H-state. Change of leakage current with stress time at different pulse width also studied by Liu *et al.* [66]. Decay of the leakage current increases with decreasing the pulse width, once the leakage-state is switched from L-state to H-state by a voltage pulse. After switching by a −12 Volt, 50 μs voltage pulse, the leakage current keeps almost the same after stressing 1200 sec at 3 Volt. However, after switching to H-state by a −12 Volt, 5 ns voltage pulse, the leakage current is about 80% decayed from its initial value, due to several wobbly conducting paths formed at smaller pulse width. After voltage stressing, the wobbly conducting paths are broken and lead to the decay of leakage current. Therefore, the resistance switching by smaller pulse width has larger decay of the leakage current. The normalized leakage current vs. stress time at different stress voltages also reported [66]. After switching to H-state by a −12 Volt, 5 ns voltage pulse, the decay under 3 Volt voltage stress is much larger than that under −3 Volt stress. In other words, the significant decay occurs while the direction of the voltage stress is different from that of the voltage pulse.

2.3.2. Effect of Mo doping on sol-gel derived $SrZrO_3$ film. Lin *et al.* [65] reported about the resistive switching characteristics of the different Mo doped SZO thin films prepared by sol-gel process. SZO thin films with various Mo-doping concentrations of 0.1, 0.2, and 0.3 mol percent, were deposited on LNO bottom electrode by sol-gel method using strontium acetate, zirconium n-propoxide, and molybdenum acetate powder precursors and acetic acid and acetylacetone as a solvent. Prepared solution was spin-coated having 20 to 50 nm thickness on LNO/SiO_2/Si substrates to form the active switching layer. Evaporated Al was used as a top electrode.

I–V switching characteristics of 0.1, 0.2, and 0.3% Mo-doped SZO thin films are shown in Fig. 12. While negative voltage is swept on the top electrode to −11 Volt, the current rapidly increases and device is switched from the low conductive state (OFF-state) to high conductive state (ON-state). The state holds on ON-state after sweeping the bias voltage from −11 to 0 Volt. Subsequently, the bias voltage sweeps to positive and changes the device from ON-state to OFF-state after passing a transition region, showing the negative differential resistance (NDR), and the OFF-state is hold as sweeping back to 0 Volt. The resistance ratio between two states is over 10^3 when the doping concentrations

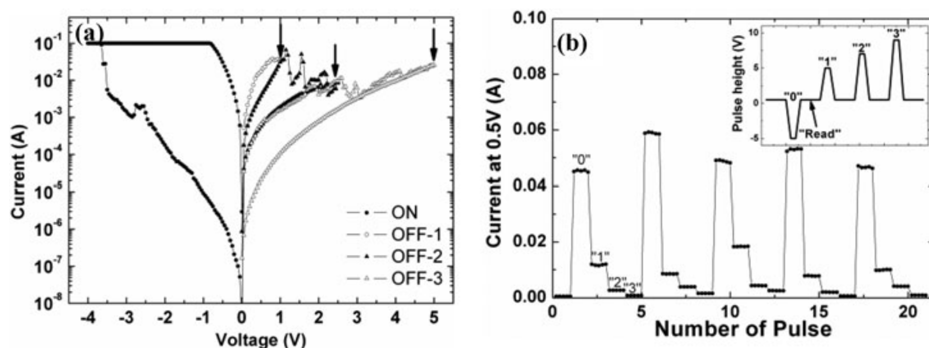

Figure 13. (a) Hysteretic I–V characteristics of the Al/0.2%-Mo:SZO/LNO device measured with different spans of voltage scan for OFF-process [after ref. 65] and (b) multi-bit storage test performed by different OFF-pulses with fixed ON-pulse [after ref. 65].

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of Mo are 0.1 and 0.2%. Moreover, resistive switching behavior of the 0.2% Mo doping SZO shows more reliable than that with 0.1% Mo doping. The resistive switching behavior becomes worse for the 0.3% Mo doped SZO film as shown in Fig. 12(b). Resistive switching behavior in this Al/0.2%-Mo:SZO/LNO device is due to the formation and rupture of conducting paths, where composed of various kinds of defects. Appropriate dopant species and concentrations are used to control the defects within the SZO thin films [124, 125]. As we realized the set and reset voltage is smaller for the V doped film having same thickness and concentrations. Besides, the interface reaction between electrodes and SZO thin films might also influence the resistive switching characteristics [125]. However, the detailed resistive switching mechanism is still unclear, and further study is needed for elucidating the origin of the resistive switching mechanism and doping effects. The 0.2 mol% Mo doped SZO based memory device showed excellent resistive switching properties and device can be operated more than 300 times during successive operation. Both high and low conductive states were stable over 10^4 s. The electrical-pulse-induced resistance change (EPIR) property was studied by applying a −2 Volt, 10 ns voltage pulse to switch the state into ON-state, and back into OFF-state again by 5 Volt, 10 ns voltage pulse. The endurance cycle was operated more than 1000 times.

For the negative differential resistance (NDR) during OFF process, the hysteretic I–V characteristics of the Al/0.2%-Mo:SZO/LNO device were investigated with the different spans of voltage scan. Bias voltage was swept as 0 Volt → −4 Volt (current compliance: 0.1 Amp.) → 0 Volt → 1 Volt (V_{OFF-1}) → 0 Volt → 2.5 Volt (V_{OFF-2}) → 0 Volt → 5 Volt (V_{OFF-3}) → 0 Volt. As the V_{OFF} increased, the higher resistance value of OFF-state increased which demonstrating the possibility for multi-bit storage application as shown in Fig. 13(a). To further investigate this electrical property, different positive voltages of 5 Volt, 7 Volt, and 9 Volt were applied to switch the device into different OFF-states. While switching the device the ON-state was fixed at −5 Volt as shown in the inset of Fig. 13(b). All the pulse widths used here were 10 ns. The multi-bit storage was well demonstrated by various positive voltage pulses as shown in Fig. 13(b).

(a) Effect of active layer thickness. As the thickness of the SZO film increased, forming voltage increases as reported by Lin *et al.* [65]. When the thickness of SZO film exceeds 30 nm, the forming voltage becomes so high (∼15 Volt) that damages memory device. Therefore, there is no bistable switching phenomenon observed after forming process.

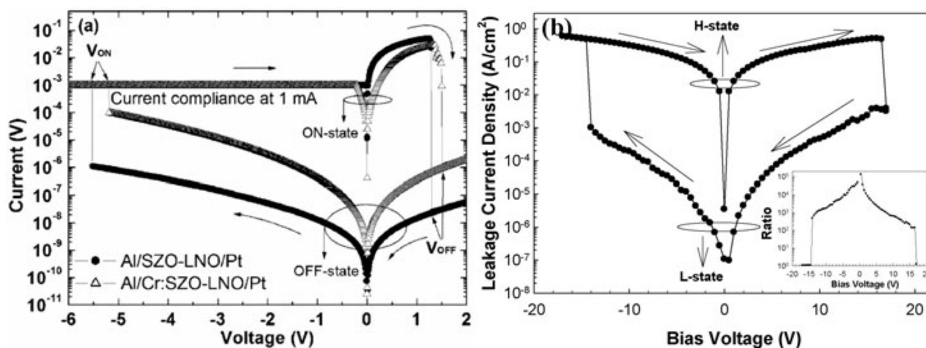

Figure 14. Leakage current density as a function of bias voltage for Cr-doped $SrZrO_3$-based MIM device. The inset shows the variation of the resistance ratio with the bias voltage. (a) I–V characteristics of both Al/SZO-LNO/Pt and Al/Cr:SZO-LNO/Pt devices, the arrows are indicate the voltage sweeping direction [after ref. 72].

On the contrary, both 20-nm and 30-nm Mo doped SZO memory films possess the resistive switching properties, and the resistive switching properties of 20-nm thick film are better than those of 30-nm Mo doped SZO based device.

2.3.3. Cr-doping effect on sputtered $SrZrO_3$ film. The resistive switching properties of the sputtered deposited V:SZO films was discussed in section 2.1. It is well known that the conductivity of the bottom electrode also takes a crucial role on switching properties. In this subsection we will discuss about the effect of Cr doping on resistive switching properties by using highly conducting bottom electrode. It has been reported that the conductivity of BE is improved by inserting Pt BE below the LNO layer [37]. Liu *et al.* [72] and Lin *et al.* [70], reported about the resistive switching characteristics of sputter deposited 90 nm thick polycrystalline 0.2% Cr-doped SZO film using LNO-Pt bottom electrode and evaporated Al top electrode (area 4.9×10^{-4} cm^2).

The bipolar I–V switching characteristics of the both Al/SZO-LNO/Pt and Al/Cr:SZO-LNO/Pt devices are shown in Fig. 14(a), where the resistance ratios between two states in these two type memory devices are over three orders of magnitude. A high voltage forming process of about -10 Volt is necessary to activate the Al/SZO-LNO/Pt device. But, the Al/Cr:SZO-LNO/Pt pristine device shows lower resistance value, which is the same as R_{OFF}, and therefore, the applied voltage for forming process is the same as that for on process (not shown here) [70]. Device with Cr doped SZO films shows higher switching ratio than the V doped SZO film having same thickness and dopant concentration. Fig. 14(b) shows the leakage current density vs. bias voltage for the 0.2% Cr doped SZO-based MIM device on LNO/$SrTiO_3$ substrate. Reproducible sequence of leakage current density can be traced from an increase of leakage current density for the high leakage (H-state) state with increasing bias voltage in the positive direction. At 15 Volt, the leakage current density rapidly decreased from high current (H-state) to low leakage (L-state) state. The leakage current density of the L-state increased with increasing bias voltage in the negative direction and rapidly increased from L-state to H-state at -15 Volt. Switching voltage of the resistive memory structures should be related to the crystallinity of the oxide film. Inset of Fig. 14(b) shows the resistance ratio decreased with increasing voltage in both the directions (10^5 at a low voltage and 10^3 at ± 10 Volt) at two leakage states. The large resistance ratio is observed for this device, which can provide enough margins to separate the different memory states.

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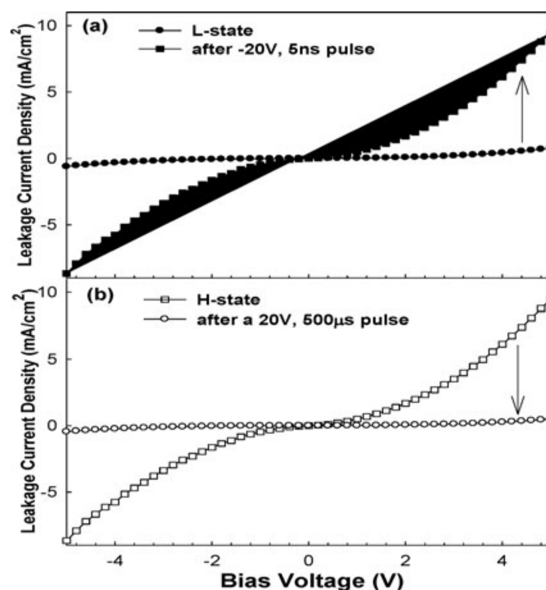

Figure 15. Change of leakage current density with the bias voltage after adding indicated voltage pulse at (a) low leakage-state and (b) high leakage-state [after ref. 72].

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The effects of different dopant concentrations in SZO material have also reported [37]. When the dopant concentration was twice larger or less than the 0.2% Cr concentration, resistive switching properties were poorer or disappeared. The same trend in the resistance ratio in both the directions indicates the identical influence of resistive transition. We will discuss in details about the effect of dopant concentration on switching properties in later section.

Figure 15(a) shows the variation of current density as a function of bias voltage of the Cr doped SZO MIM capacitor (deposited on LNO/$SrTiO_3$ substrate) and response of the device after applying a −20 Volt, 5 ns pulse on TE. By applying a negative voltage pulse, the device changed from L-state to H-state. On the other hand, Fig. 15(b) shows the switching of the H-state to L-state after applying 20 Volt, 500 μs pulse. Resistance change driven by voltage pulses had the same polarity direction with that driven by the bias voltages. It is indicated that the conduction mechanism at L-state is dominated by P-F emission as discussed before. In addition, it was observed that the conduction mechanism of H-state is governed by the P-F emission at low voltage while at higher bias voltage, the conduction mechanism of H-state is still followed by the Ohmic mechanism. This is due to the pulse operation has smaller transition time than dc voltage sweep. Switching transition time of the H-state to L-state was five orders of magnitude longer than that of the L-state to H-state, indicates the transition from L-state to H-state was easier than that of the H-state to L-state. Therefore, transition from H-state to L-state is limited part for the reversible switching by voltage pulse operation.

2.4. Thickness and Doping Concentration Effect on Vanadium Doped SZO Film

In section 2.1 we observed that the 0.2 mol% V doped SZO film shows bipolar switching effect. All other films with higher thickness of about 30–100 nm thick also shows bipolar

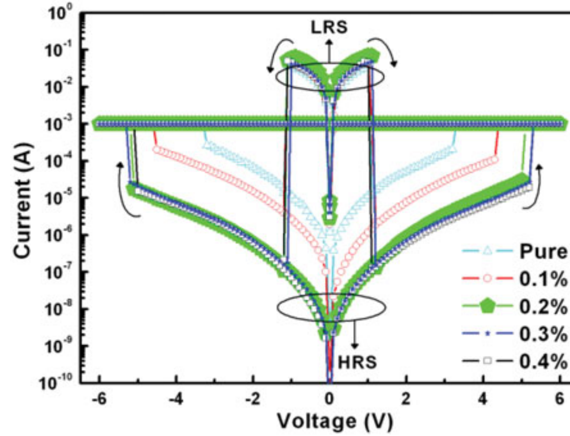

Figure 16. Typical I–V characteristics of SZO-based memory devices at different vanadium doping in semilogarithmic scale [after ref. 37].

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switching. As the film thickness decreases to 20 nm, the bipolar switching changes to the unipolar switching. On the other hand, in section 2.3.2 we also observed the significant effect of the dopant concentration on solgel derived Mo doped SZO films. Lin et al. [37] reported about the change of resistive switching of the SZO film having different vanadium concentration. A 20-nm thick with different vanadium doped, such as 0.1, 0.2, 0.3, and 0.4 mol%, SZO (V:SZO) thin films were deposited on LNO/Pt/Ti/SiO_2/Si layer by reactive RF sputtering (gas ratio Ar : $O_2 = 24 : 16$).

Figure 16 shows unipolar resistive switching characteristics of the Al/V:SZO/LNO/Pt memory structure. In the both positive and negative voltage directions, the device can switch from LRS to HRS state and vice-versa. Fig. 17(a) shows the forming voltages are increases with the increase of vanadium doping concentration up to 0.2 mol%, but it's almost fixed upto 0.4 mol% vanadium doping. The correlation between vanadium doping concentration and set/ reset voltage is illustrated in Fig. 17(b). Turn-on voltage increases with increasing vanadium up to 0.2 mol%, but it is almost fixed (~ -5 Volt) for 0.2 to 0.4 mol% V doping, this trend is similar to the trend of forming voltage with the doping concentration. It's clear that the memory device based on pure SZO shows the lower forming voltage and turn-on voltage than the doped one, which is appropriate for the low-voltage NVM application. On the contrary, turn-off voltage (-1 Volt) is almost independent of vanadium doping. As shown in Fig. 17(c), the change of HRS resistance is similar with the trend of forming voltage and set voltage with the increase of doping concentration. By contrast, LRS resistance remains constant of about 30 Ω for all the doped and undoped memory devices. The broad dispersions of turn-on voltage and HRS resistance is due to the randomly ruptured of conducting filaments by Joule heating effect [127]. Therefore, the LRS current is increased up to 0.1 Amp compared with the Al/SZO/LNO/Ti/SiO_2/Si devices ($\sim 10^{-3}$ Amp). Moreover, when this high current ($\sim$0.1 Amp) flows (locally high power density$\sim 10^{12}$ W/cm^3 [30]) through the filaments, the turn-off process is dominated by the Joule heating effect, which is dependent on thermal energy and independent of voltage polarity. As a result, the memory state of Al/SZO/LNO/Pt devices can be switched from LRS to HRS by applying both the positive and negative bias, which leads to nonpolar RS characteristics.

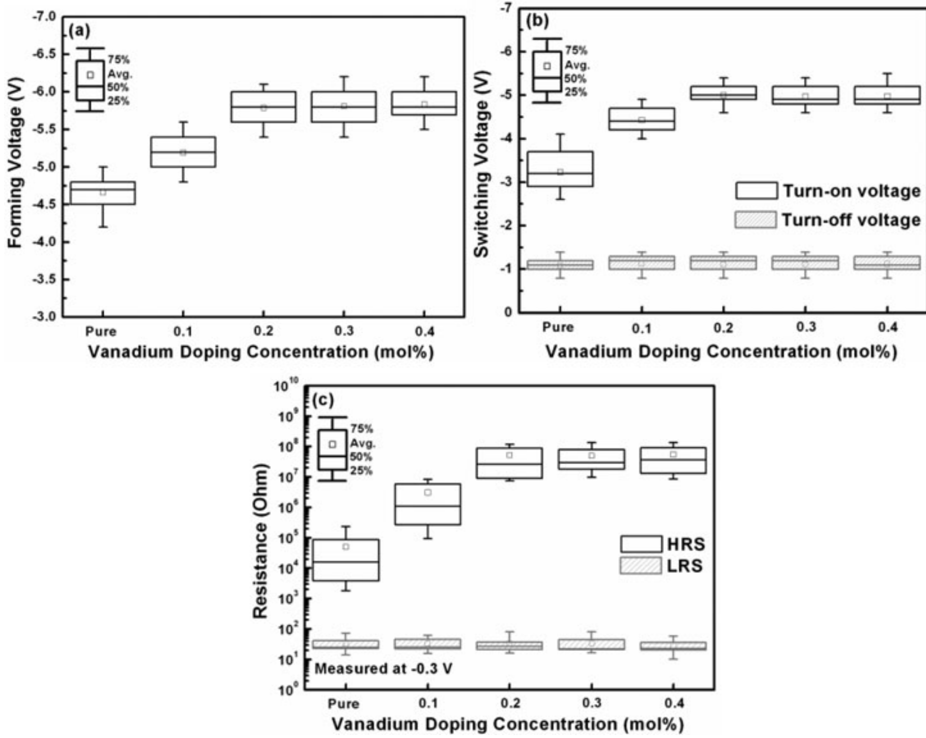

Figure 17. Statistic relationship between the vanadium doping concentration and RS parameters; (a) forming voltage, (b) switching voltage, and (c) HRS and LRS resistance [after ref. 37].

To understand the conduction mechanisms at HRS state of the SZO-based devices P-F emission mechanism is fitted. The P-F emission is expressed as [19]:

$$J \sim E \exp\left(\frac{-q\left(\phi_{B,eff} - \sqrt{qE/\pi\varepsilon_i}\right)}{kT}\right) \tag{2}$$

Where ε_i is the dynamic dielectric constant, q the elementary charge, $\phi_{B,eff}$ the effective barrier height which the conduction electrons are thermally emitted from the trapping levels to conduction band under applied electric field, k is the Boltzmann constant, and T is the absolute temperature. Fig. 18(a) shows the plots of Ln ($|J/E|$) as a function of $|E|^{1/2}$ of the HRS currents of the devices, indicating that the carrier conduction in the films is dominated by P-F emission. The calculated dielectric constant was decreased from 60 to 20 with the increasing of the vanadium doping concentration up to 0.2 mol%, but it has same value upto 0.4 mol% V doping, as shown in inset of Fig. 18(a), The temperature dependence of the HRS currents of the devices is shown in Fig. 18(b), which indicate the carrier conduction is also obeys P-F emission mechanism in the temperature ranges 300 K to 500 K.

Ohmic conduction mechanism is well fitted for LRS current of this RRAM devices, which is expressed as [19]:

$$J \sim V \exp(-E_a/kT) \tag{3}$$

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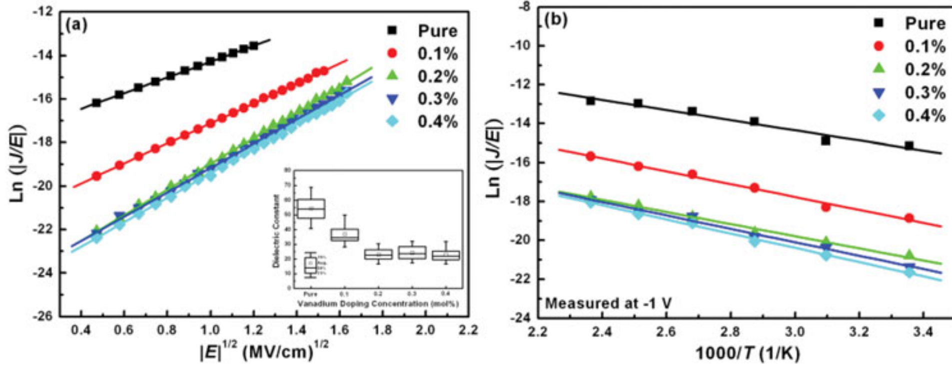

Figure 18. (a) The curve fitting plot of F-P emission for HRS currents, inset is the plot of dielectric constant versus vanadium doping concentration and (b) temperature dependence of the HRS current at −1 Volt for SZO based thin films [after ref. 37].

where E_a is the activation energy of conduction carriers in the insulating thin films. Fig. 19(a) presents the plot of Ln ($|J|$) versus Ln ($|V|$) of the LRS currents of the devices. The slopes are close to unity, indicates carrier conduction at LRS is followed by Ohmic conduction mechanism. However, based on the plot of Ln ($|J|$) versus 1000/T in Fig. 19(b) shows that the LRS current is increased with increasing the temperature; it should not be metallic conductivity. The hopping conduction would be responsible for the LRS current. Activation energies are calculated from the slopes of the Arrhenius plot, which are in the range of 0.10∼0.13 eV.

Figure 20 depicts the extraction of $\phi_{B,eff}$ of P-F defects in doped SZO RRAM structures. By extrapolation of above measurement data at zero electric field, $\phi_{B,eff}$ the P-F defects, such as oxygen vacancies or other electronic defects, distributed in the bandgap of SZO-based films can be obtained. P-F defects for the various doping concentrations are shown in the inset of Fig. 20. With increasing vanadium doping concentration up to 0.2%, $\phi_{B,eff}$ also increases from 0.44 to 0.63 eV, but it is almost same for the 0.2 to 0.4 mol% V:SZO films. This tendency is analogous to forming voltage, turn-on voltage, HRS resistance, and dielectric constant, indicating the vanadium doping plays an imperative role in

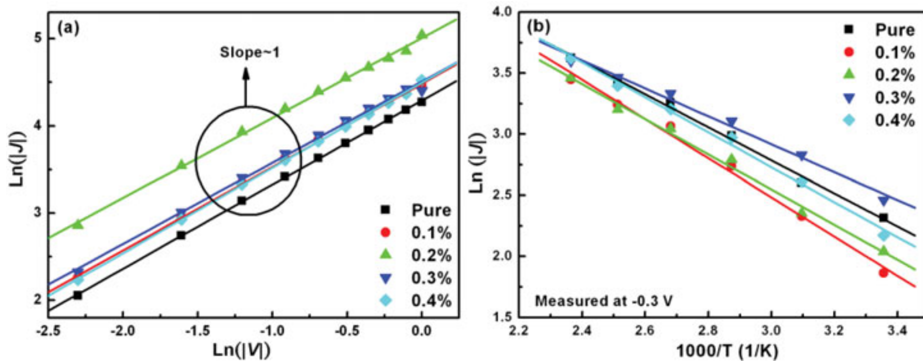

Figure 19. (a) Curve fitting plot of Ohmic conduction for LRS current in SZO-based memory devices and (b) temperature dependence of the LRS current at −0.3 Volt [after ref. 37].

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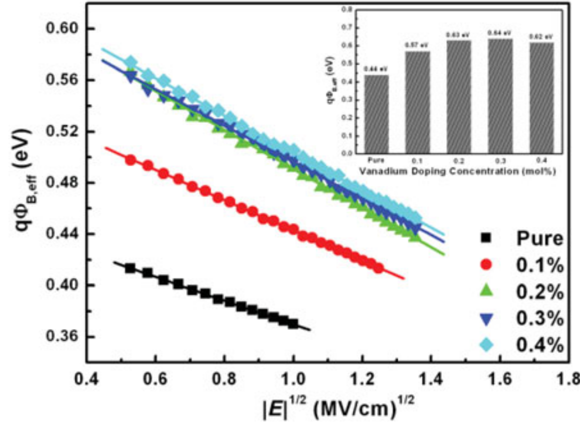
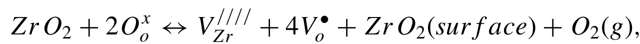


Figure 20. Extraction of $\phi_{B,eff}$ of F-P defects in SZO-based thin films, inset is $\phi_{B,eff}$ at different doping concentrations [after ref. 37].

the electrical properties of SZO thin films, within the solid solubility limit. In addition, activation energy calculated from the slope of Arrhenius plot is much smaller than the extracted $\phi_{B,eff}$. The conduction mechanism at LRS is quite different from HRS due to the different energy levels of defects.

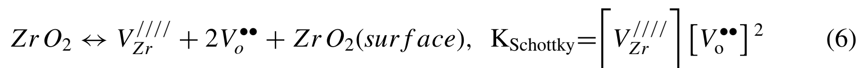
Vanadium doping into SZO films might lead Zr^{4+} sites to be substituted by V^{5+}, resulting in the change of $\phi_{B,eff}$ of P-F defects. So far, the essential of the P-F defects is still unclear. Lin *et al.* reported that Ti top electrode modified the distribution of oxygen content, oxygen vacancies, oxygen ions, and oxygen-related defects at the ZrO_2 films, which causes the transition from unipolar to bipolar switching behaviors [127, 128]. It is also noticed that the oxygen content and oxygen-related defects had enormous influences on RS properties [129–130]. RS characteristics on SZO-based memory devices should be interrelated with the oxygen vacancies in bulk films [68, 131]. Furthermore, oxygen vacancies also play a crucial role in the electrical characteristics in various kinds of electro-ceramic thin films such as $BaTiO_3$, $SrTiO_3$ (STO), $(Ba_{1-x}Sr_x)TiO_3$, and MgO [124, 132]. We believed that the P-F defects might relate to the oxygen vacancies at the SZO films. It is significant that the role of V doping plays a significant role on the physical and electrical properties of SZO films. Taking the site, mass, and charge balances into account, the possible defect equations at Zr site of the films substituted by the high valence cation (V^{5+}) can be expressed as the followings:

$$2V_2O_5 \xleftrightarrow{5ZrO_2} 4V_{Zr}^{\bullet} + 10O_o^x + V_{Zr}^{////} \quad (4)$$

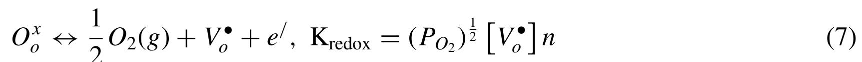


$$ZrO_2 + 2O_o^x \leftrightarrow V_{Zr}^{////} + 4V_o^{\bullet} + ZrO_2(surface) + O_2(g),$$

$$\mathrm{K_{Schottky}} = \left[V_{Zr}^{////}\right]\left[V_o^{\bullet}\right]^4 P_{O_2} \quad (5)$$



$$ZrO_2 \leftrightarrow V_{Zr}^{////} + 2V_o^{\bullet\bullet} + ZrO_2(surface), \quad \mathrm{K_{Schottky}} = \left[V_{Zr}^{////}\right]\left[V_o^{\bullet\bullet}\right]^2 \quad (6)$$



$$O_o^x \leftrightarrow \frac{1}{2}O_2(g) + V_o^{\bullet} + e^{/}, \quad \mathrm{K_{redox}} = (P_{O_2})^{\frac{1}{2}}\left[V_o^{\bullet}\right]n \quad (7)$$

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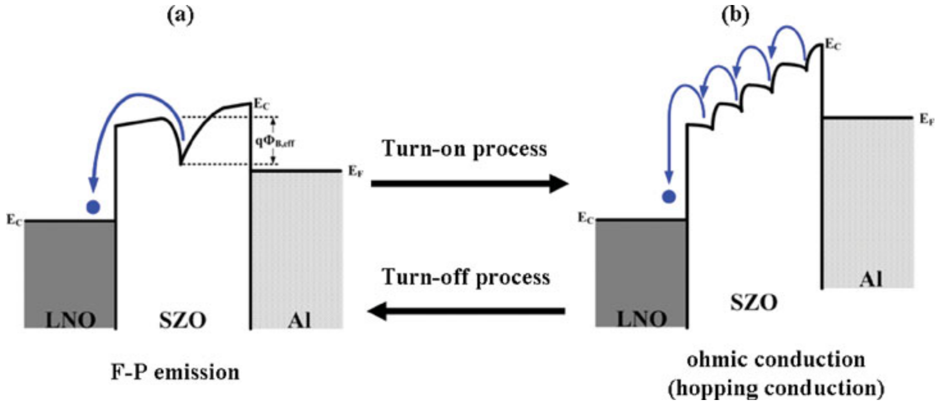
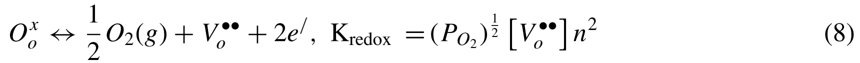


Figure 21. Schematic structure of the RS mechanisms of SZO-based thin films (a) HRS is dominated by F-P emission, showing the conduction electron hopping through the deep oxygen vacancies with $\phi_{B,eff}$ (i.e., rupture of conducting filaments), and (b) LRS is dominated by the Ohmic conduction (hopping conduction) showing the biased electron hopping through the shallow oxygen vacancies with $\phi_{B,eff}$ (i.e., formation of conducting filaments) [after ref. 37].



$$O_o^x \leftrightarrow \frac{1}{2}O_2(g) + V_o^{\bullet\bullet} + 2e^{/},\ \ \mathrm{K_{redox}} = (P_{O_2})^{\frac{1}{2}}\left[V_o^{\bullet\bullet}\right]n^2 \quad (8)$$

where $V_{Zr}^{\bullet}$ denotes vanadium ion with singly positive charge in Zr site, $V_o^{\bullet}$ and $V_o^{\bullet\bullet}$ are oxygen vacancies with singly and doubly positive charge, respectively, O_o^x indicates neutral oxygen ion in lattice site, $V_{Zr}^{////}$ is zirconium vacancy with quadruple negative charge, and $e^{/}$ denotes electron with singly negative charge for the charge compensation. Here, SrO is assumed that not to influence in the defect formation [37].

According to above equations, at particular temperature vanadium doping not only increases electron concentration but also reduces the oxygen vacancy concentration. Furthermore, the increased electrons must be depleted to the LNO buffer layer (for its higher work function than Al [133]) so that the HRS resistance could be increased. The introduction of donor, vanadium ion, can suppress the generation of oxygen vacancies in $SrBi_4Ti_4O_{15}$ thin films [134]. In addition, the introduction of low valence cation (Cr^{3+}) on Ti^{4+} site in the single-crystal STO thin films induced the oxygen vacancies into crystal lattice. These oxygen vacancies determined the path of electrical conduction in Cr-doped STO thin films, thus leading to bistable RS phenomenon [135]. $\phi_{B,eff}$ of $V_O^{\bullet}$ (0.5 eV) is obviously much lower than that of $V_O^{\bullet\bullet}$ (2.0 eV), as a result, it could be more difficult for the conduction electrons to overcome from $V_O^{\bullet\bullet}$ to conduction band than $V_O^{\bullet}$ under applied electric field. Indeed, $V_O^{\bullet}$ and $V_O^{\bullet\bullet}$ in SZO-based thin films would both be suppressed by vanadium doping. It may be noted that, decrease of static dielectric constants of SZO-based thin films with increasing vanadium doping, induced the reduction of oxygen vacancy concentrations.

From the curve fitting at HRS currents (Fig. 18(a)), the conduction mechanism below set voltage is dominated by P-F emission mechanism, indicating the conduction electrons hopping through the small amount of deep oxygen vacancies (~0.44 to 0.63 eV) in SZO-based thin films as shown in Fig. 21(a). The suppression of oxygen vacancies may increased the difficulty of biased electron hopping through the oxygen vacancies from cathode to anode. As a result, the HRS resistance is increased with increasing vanadium doping concentration up to 0.2 mol%. When increasing the applied voltage to set voltage

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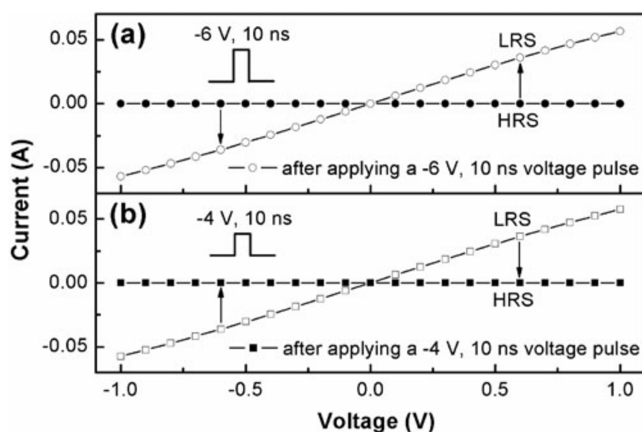

Figure 22. Resistive switching speed of the Al/V:SZO-LNO/Pt device, switching after applying indicated voltage pulse from (a) HRS to LRS and (b) LRS to HRS [after ref. 63].

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($\phi_{B,eff} = 0.10$ eV to 0.13 eV) shallow oxygen vacancies are aligned to make conducting filaments connecting between the TE and BE, leading to the transition from P-F emission to Ohmic conduction, as shown in Fig. 21(b).

The switching speed of the Al/V:SZO/LNO/Pt RRAM (45-nm thick 0.3 mol% V-doped) device is shown in Fig. 22. Fig. 22(a) shows the I–V curves switches from HRS to LRS states after applying a −6 Volt, 10 ns voltage pulse. This device is switched back to HRS state again after applying a −4 Volt, 10 ns voltage pulse, as shown in Fig. 22(b). Switching speed of set and reset processes is 10 ns. Liu et al., reported that the device with Al/Cr-doped SZO (Cr:SZO)/LNO structure can be turned on and turned off by applying −20 Volt, 5 ns and +20 Volt, 500 μs voltage pulses, respectively [63, 72]. The five orders of switching speed difference between turn on and turn off processes can be explained by the LNO compliance effect. In the turn off process, electrons are injected from BE to resistive layer, so the conductivity of BE will determine the switching speed of the device. Therefore, the SZO-based memory device using Pt BE can significantly improve the switching speed.

2.5. *Effect of Annealing on Resistive Switching Properties*

The annealing conditions also play a significant effect on the resistive switching parameters. Lin *et al.* studied the annealing effect on resistive switching memory for their 20 nm thin V:SZO[200] films on LNO/Pt substrate [68]. RTA process (600, 700, and 800°C in O_2 ambient for 1 min, respectively) was used to improve the quality of the SZO thin films. Other films (same thickness and conditions) were also RTA annealed at N_2 and Ar ambient for 600°C, 1 min. After RTA process the average lattice constants of the as-deposited, N_2-600, Ar-600, O_2-600, O_2-700, and O_2-800 SZO thin films are calculated to be 4.142, 4.142, 4.142, 4.127, 4.118, and 4.111 Å, respectively, from the XRD spectra, indicating that the lattice constant of the films is influenced by O_2 annealing. As the lattice constant changes after annealing, it is also affected on the switching parameters. Fig. 23(a) shows the statistical chart of the forming voltage variation of SZO (undoped) memory devices at different annealing conditions. Forming voltage are increases with the increasing of RTA temperature from 600 to 800°C, but it is almost same for the as-deposited, 600°C nitrogen and 600°C argon annealed devices, indicating that the insulating property of the

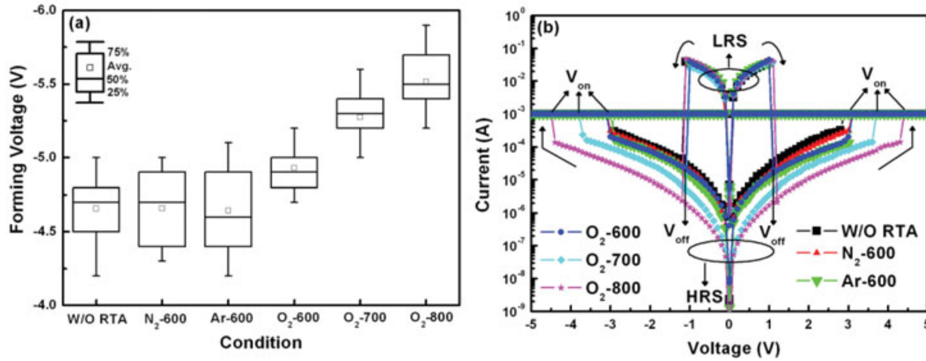

Figure 23. (a) Statistical chart of the forming voltage at different annealing conditions and (b) typical *I–V* curves of SZO-based memory devices [after ref. 55].

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as-prepared SZO films could be improved by oxygen annealing. Fig. 23(b) show the typical current-voltage (*I–V*) curves of the SZO memory devices at various annealing conditions. Devices show the nonpolar resistive switching properties. From the figure it is observed that both HRS resistance and set voltage are increased with the increase of annealing temperature (oxygen annealed), indicating that these RS parameters might be significantly associated with the oxygen content in SZO films. When the annealing ambient is changed, HRS resistance and set voltage is almost unaltered. It may be noted that, reset voltage and resistance at LRS is almost independent with annealing temperature and annealing ambient.

2.6. *Effect of Device Structure on $SrZrO_3$ Based Memory Devices*

Till now, we have discussed about the resistive switching properties of the single layer structures. In this section we will discuss about the resistive switching effect on bilayer structures. As we realized that the resistive mechanisms are dominants by the filamentary conduction mechanisms. The filaments are formed by the oxygen vacancies or defects. If we vary the oxygen concentration in the active layer, the switching properties may improve. To study the effect of oxygen on resistive switching properties, a double layer (oxygen rich and oxygen deficient) SZO based memory devices was proposed by Lin *et al.* [57]. A 20 nm thick SZO film was deposited on LNO/Pt/SiO_2/Si substrate at 500°C by sputtering to study the switching effect on double layer. The film was deposited using pure Ar gas for first 50 min sputtering, then by a mixture of Ar and O_2 (ratio 3:4) for last 10 min. Such film is named as oxygen flow control (OFC) film. For comparison, a 20 nm thin SZO film was also deposited in same condition by using Ar and O_2 (ratio of 3:4) throughout the process. The film is named without (W/O) OFC film. Finally, a 300 nm thick Al TE with a diameter of 150 μm was evaporated on SZO thin films [57].

Figure 24(a) shows the nonpolar switching characteristics, in the both positive and negative voltage direction, of the W/O OFC and OFC memory devices. A high resistance ratio owing to low leakage current at HRS is observed for the W/O OFC i.e. oxygen reached single layer devices. It's also important that here also leakage current at LRS is almost independent of the oxygen flow. Fig. 24(b) shows the statistical chart of $V_{forming}$ and V_{on} of these devices. The $V_{forming}$ and V_{on} are strongly dependent on the process and these are effectively reduced from −6 Volt and −4 Volt to −2.5 Volt and −1.6 Volt, respectively, after OFC process. In addition, this process considerably suppresses the dispersions of

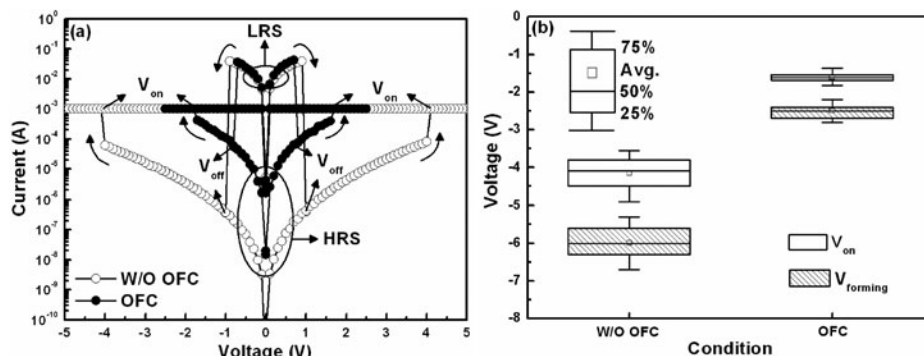

Figure 24. (a) Typical *I-V* characteristics of the W/O OFC and OFC devices and (b) statistical plot of the $V_{forming}$ and V_{on} of the W/O OFC and OFC devices [after ref. 57].

these resistive switching parameters of OFC devices in comparison with those of W/O OFC devices.

The formation and ruptured of the conducting filaments made by oxygen vacancies (OVs) in SZO based RRAM devices have been considered as a dominant factor for switching behaviors [57, 63, 68, 136–141]. Fig. 25(a) schematically shows the as-prepared OFC devices have the OR (oxygen rich) and OD (oxygen deficient) double-layer structure. After forming process by applying high-voltage, the formation and configuration of OVs happen to form the conducting filaments between TE and BE, device switched from original state to LRS, as shown in Fig. 25(b). Due to unusual OVs density between OR and OD layers, physical dimension of the conducting filaments at the OR layer should be narrower than those of the OD layer. Once the large current flows through the filaments, the narrower filaments at the OR layer would be ruptured at first, due to the locally higher power density (thermally assisted OVs oxidation) while the filaments in the OD layer still present and the device is switched to HRS, as shown in Fig. 25(c). Due to the effective reduction and localization of RS region, OFC devices exhibit lower operation voltage and smaller dispersions of switching parameters such as $V_{forming}$ and V_{on} than those of the W/O OFC devices. When a voltage bias is swept to V_{on}, OVs in the OR layer would be generated and aligned

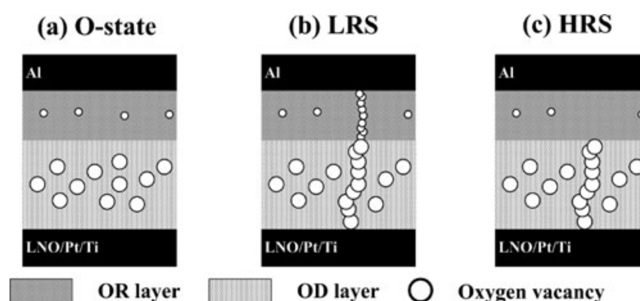

Figure 25. Schematic diagrams of RS mechanism of OFC memory devices (a) before forming process, OFC memory devices show the double-layer structure, (b) the formation of conducting filaments connecting TE and BE, and the memory state is switched from original state to LRS, and (c) the narrower conducting filaments in the OR layer are ruptured by Joule-heating effect while the filaments in the OD layer still remain, the memory state is switched to HRS [after ref. 57].

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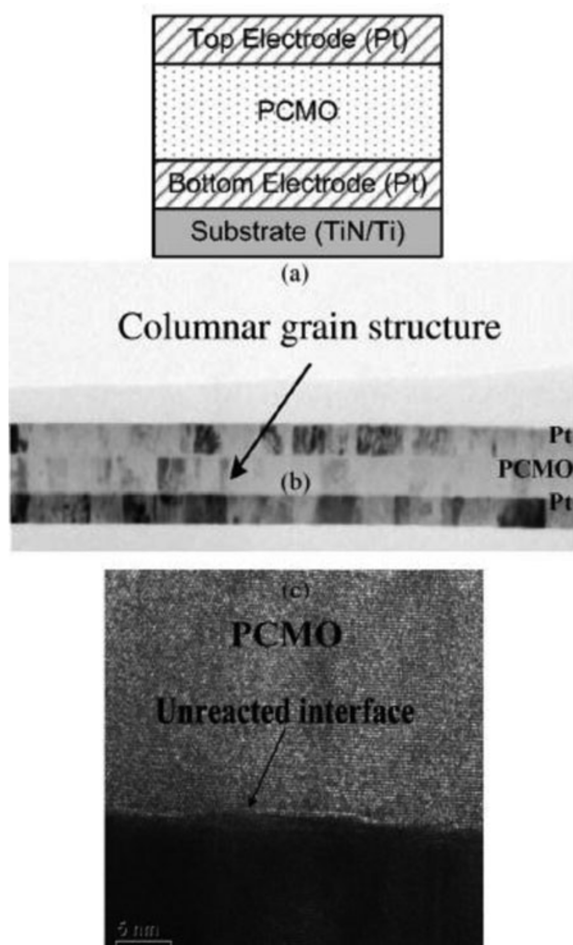

Figure 26. (a) A schematic structure of the PCMO based RRAM device (b) cross-sectional TEM image of the structure. (c) HRTEM image of a PCMO/Pt interface [after ref. 106].

to connect the residual conducting filaments in the OD layer, switching the memory state from HRS to LRS, as shown in Fig. 25(b).

3. Resistive Switching Properties of $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) Film

3.1. *Effect of Electrode*

3.1.1. Resistive switching of PCMO film with Pt electrodes. Chen *et al.* [106] reported the resistive switching properties of PCMO thin films with Pt electrodes. A schematic structure of the $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) devices is shows in Fig. 26(a). A 30 nm thick sputtered deposited PCMO layer is sandwiched between a Pt bottom electrode (BE) and a Pt top electrode (TE). The device was fabricated on a patterned TiN/Ti substrate. Fig. 26(b) shows a cross-sectional transmission electron microscopy (TEM) image of a Pt/PCMO/Pt heterostructure deposited on SiO_2/Si substrate, where the columnar PCMO

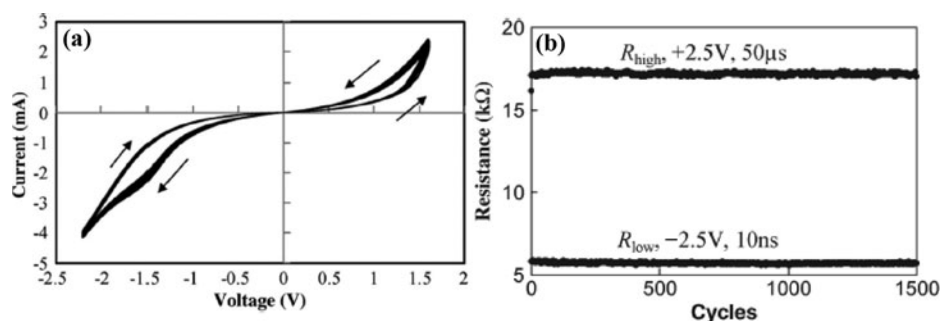

Figure 27. (a) DC *I–V* hysteresis sweep of a 500 nm × 1000 nm PCMO device and (b) EPIR performance of the 500 nm × 1000 nm device [after ref. 106].

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grains are clearly observed. The high-resolution TEM (HRTEM) image in Fig. 26(c) reveals a well-defined and unreacted oxide/metal interface between the PCMO layer and the Pt BE.

Bipolar resistance switching phenomena was observed from the *I–V* hysteresis curve in the PCMO devices as shown in Fig. 27(a). The device switches from the HRS to LRS (set) at +1.6 Volt, while the device switches from the LRS to HRS (reset) at −2.2 Volt. It is observed that the dc voltages required switching the device and it is almost independent on the device size. The EPIR bipolar switching was also observed for these PCMO devices. Fig. 27(b) shows the EPIR performance of the 500 nm × 1000 nm PCMO device for 1.5×10^3 programming cycles. To set the device, 2.5 Volt 50-μs pulse-width voltage pulse was applied to the TE and, while a negative electric pulse of −2.5 Volt with a 10-ns pulse-width, was used to reset the device. R_{high} and R_{low} denote the resistance of the PCMO device at the HRS and LRS, respectively. The EPIR ratio is defined as ($R_{high} - R_{low}$)/R_{low}, which is close to 200% as shown in Fig. 27(b). The average values of the R_{high}'s and R_{low}'s are 17.16 and 5.69 KΩ, respectively and it's almost stable (upto more than 1.5×10^3 cycles) during all of the programming cycles, shows outstanding cycle-to-cycle stability, i.e., the standard deviations of all samples of the R_{high} and R_{low} at all cycles are only 81 and 44 Ω, respectively. The device showed good retention after 24 hour at 150°C, no resistance degradations between two resistance states were observed.

3.1.2. Resistive switching in PCMO films with multilayer graphene electrode. Lee *et al.* reported the resistive switching characteristics in PCMO devices using multilayer graphene (MLG) as a top electrode (TE) [108]. Interfacial-reaction-type resistive switching was observed upon introducing MLG as a conducting electrode to electrochemically functionalize graphene at the MLG/PCMO interface. A 60-nm thick PCMO film was deposited by rf sputtering on Pt/SiO_2/Si substrate. Initially the MLG films were fabricated on nickel films by chemical vapor deposition (CVD) [142]. Finally the MLG films were detached from the nickel layers and transferred to the PCMO/Pt/SiO_2/Si substrate. A structure with Pt TE was also fabricated as a reference for this study.

The good quality of the MLG films was confirmed from the Raman spectroscopy. Sheet resistances of MLG films were in the range of 700±100 Ω/cm^2. The typical current-voltage bipolar switching characteristic of the MLG/PCMO/Pt device is shown in Fig. 28(a). A bias was applied to top electrode (MLG), whereas bottom electrode (Pt) was grounded,

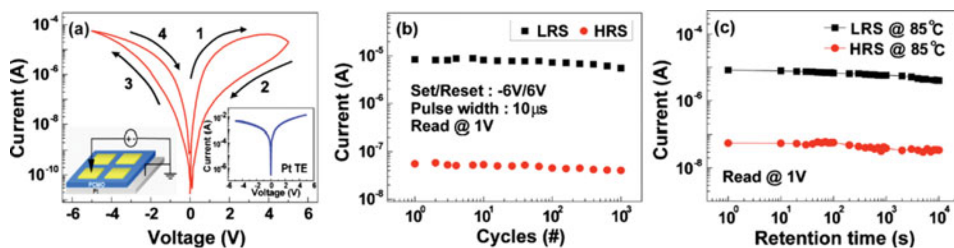

Figure 28. (a) Typical current-voltage characteristics of the PCMO device with MLG electrode, arrows are indicates the direction of dc sweep. The left inset shows the measurement configuration of the devices and the right inset, the current-voltage characteristics of PCMO device with Pt top electrode. (b) Pulse endurance and (c) retention characteristics of MLG/PCMO/Pt, indicating stable HRS and LRS for up to 10^4 s at 85°C [after ref. 108].

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as shown in the left inset of Fig. 28(a). On increasing the applied positive voltage from 0 to 5 V, the device state changed from the LRS to the HRS, whereas on increasing the applied negative voltage from 0 to −5 Volt, LRS was obtained again. No forming process required for this device [106]. No resistive switching observed for the device having Pt TE of this PCMO based device structure, as shown in the right inset of Fig. 28(a). The device shows a negligible degradation of the HRS and LRS upto 10^3 cycles, confirmed from the pulse endurance characteristics as shown in Fig. 28(b). Fig. 28(c) shows the retention characteristics of this device at 85°C. Stable HRS and LRS with high resistance ratio were observed upto 10^4 seconds.

The switching mechanisms of the MLG/PCMO/Pt structures are shown in Fig. 29. When a positive bias is applied, oxygen ions in PCMO are incorporated into the MLG layer and an oxygenated graphene layer is formed at the MLG/PCMO interface, as illustrated in Fig. 29(a). Therefore, the total resistance of the layer is increases and switching from LRS to HRS is achieved. The device acts like GO/PCMO device structure as discussed in the previous section. Conversely, when a negative bias is applied, oxygen ions are extracted from the oxygenated graphene, resulting in the almost dissolution of the oxygenated graphene layer at the MLG/PCMO interface. As a result, the conductivity of oxygenated graphene increases and the device switches to LRS, as shown in Fig. 29(b). It is important to note that for this structure the device switched from the LRS to HRS and then HRS to LRS repeatedly.

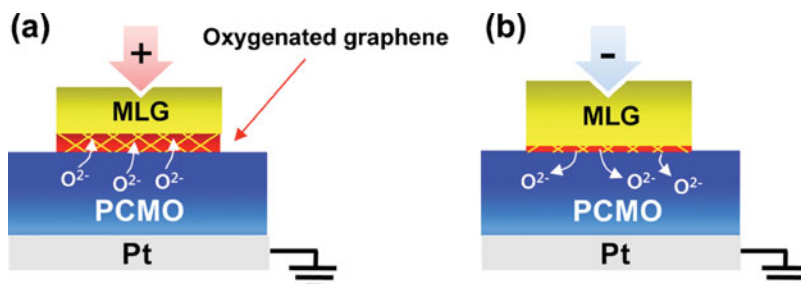

Figure 29. Schematic illustrations of resistive switching behavior of MLG/PCMO/Pt device; (a) HRS and (b) LRS [after ref. 108].

3.2. Effect of Device Structure

3.2.1. Resistive switching in bi-layer PCMO films. In the previous section, we have discussed about the resistive switching effect of single layer PCMO film. We know that the oxygen vacancies are the key factors for resistive switching properties. Liu *et al.* [109] reported about the resistive switching properties in the homogeneous bi-layer *PCMO* thin film devices, where one layer oxygen-rich (OR) and the other one is the oxygen-deficient (OD) film. OR-PCMO (PCMO1), OD-PCMO (PCMO2), and bi-layer (PCMO2/PCMO1) thin films were deposited by PLD on Pt/Ti/SiO_2/Si substrates. Polycrystalline PCMO1 and PCMO2 films were deposited for 5 minutes at 50 and 0.05 mTorr O_2 pressure, respectively. Sputtered Pt top electrode was used to achieve MIM structure.

Mostly PCMO forms Ohmic contact with Pt [109, 143]. The structure with PCMO1 active layer shows lower initial resistance (100–800 Ω), whereas the structure with PCMO2 layer shows relatively higher initial resistance (1–200 MΩ). The two structures show the nonlinear and almost symmetric current–voltage (*I–V)* curves, as shown in Fig. 30(a), with no evidence of hysteresis loops. In compare, the Pt/PCMO2/PCMO1/Pt structures showed bipolar resistive switching behavior, as shown in Fig. 30(a). It required a forming process, of about 4.5 Volt forming voltage, (10 mA current compliance) to switch the device to HRS state, as shown in the inset of Fig. 30(b). After the initial forming process the memory device switched to LRS. The device is reset (switched from LRS to HRS) by sweeping the voltage to positive direction, at about 0.9 Volt. Subsequently, the set process by applying −3 Volt reset voltage, and the nonvolatile switching was observed. Area dependence of the two resistance states is shown in Fig. 30(c). Resistance at LRS is almost independent with the electrode size, whereas the resistance at HRS decreases with electrode area. Which is indicates that the formation and rupture of the localized conductive filaments are responsible for such characteristics of this bilayer structures. *I–V* curve of LRS exhibits Ohmic behavior with a slope of 1 indicates the formation of conducting filaments during set process. However, the *I–V* curve of HRS in the low voltage shows some fluctuation. At low field region the Ohmic conduction (I–V) behavior and in the higher voltage the trap free SCLC conduction mechanism is observed.

3.2.2. Doped PZT/PCMO heterostructure resistive memory. Bourim *et al.* [110], reported the resistive switching characteristics of an all perovskite heterostructure composed of an active Al-Nb co-doped $Pb(Zr_{0.58}Ti_{0.42})O_3$ (PZT) ferroelectric thin film and a semiconducting $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) layer, both sandwiched between the Pt electrodes. The Al and Nb doped PZT and PCMO thin films were grown by PLD. Typical thickness of the deposited crystalline PZT film was ∼15 nm while that for polycrystalline PCMO films was varied from 20 to 240 nm.

Figure 31 shows the typical DC I–V characteristics of the fabricated Pt/PZT/PCMO(60 nm)/Pt device. After first voltage sweep (0→+2 Volt→0→−2 Volt→0) referred to as electroforming in which the current underwent an sudden decrease in the positive voltage region (dashed curve in Fig. 31) that is associated to a strong switching polarization current (charging-discharging at the capacitor electrodes) resulting from the first reorientation and reversal of ferroelectric domains in the PZT film. An increase of voltage sweeping bias amplitude to $V_{max} = \pm 4$ Volt, the reversible counter clockwise I–V hysteresis loops evolved in both positive and negative voltage regions as shown by arrows in the I–V curves of Fig. 31. The switching curves representing up to several cycles exhibit a near-perfect stability and reproducibility as well as highly symmetrical hysteresis curves. To realized the transport properties after the application of a voltage

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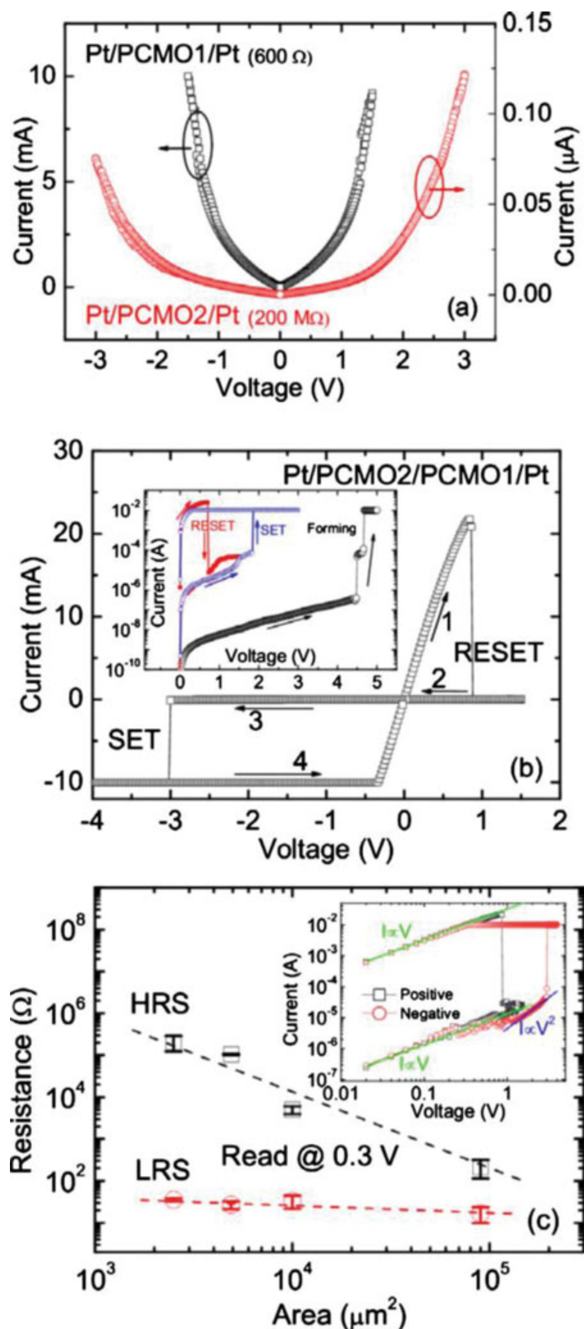

Figure 30. Typical *I–V* characteristics of (a) Pt/PCMO1/Pt and Pt/PCMO2/Pt, (b) Pt/PCMO2/PCMO1/Pt structures in linear scale. The inset of (b) shows the forming process and the unipolar switching during positive voltage sweep. (c) The change of resistance as the device area changes, giving an indication of filament-type switching in Pt/PCMO2/PCMO1/Pt memory devices. The inset of (c) shows the typical *I–V* characteristics and their fit results shown in double-logarithmic scale [after ref. 109].

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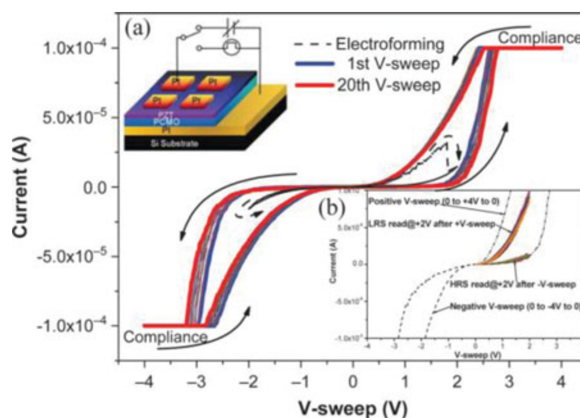

Figure 31. DC I–V hysteresis characteristics of Pt/PZT/PCMO(∼60 nm)/Pt layered structure. V-sweep range of 0→+2 Volt→0→−2 Volt→0 (dashed line) corresponds to electroforming. Inset (a) is a schematic configuration of device and measurement setup, inset (b) shows the probing of resistance states in the positive voltage region [after ref. 110].

sweep cycle of positive or negative polarity demonstrated that a large positive voltage sweep cycle (>2.5 Volt) induces a LRS in the positive voltage region as is probed by the repeated read-out at 2 Volt (inset (b) of Fig. 31), and a successive application of a large negative voltage sweep cycle (<−2.5 Volt) induces a HRS as is probed as well in the positive voltage region by the repeated read-out at +2 Volt (inset (b) of Fig. 31). Similarly, the resistance switching states can also be recognized in the negative voltage region and probed by a negative read bias. Consequently, the hetero-structured PZT/PCMO device showed a bistable resistance switching properties controlled by bipolar switching mode.

Figure 32 presents the obtained I–V hysteresis characteristic for such mesa-structured device with a thinner PCMO layer thickness of ∼20 nm that may generate less stress in PZT film. No electroforming was observed in the first voltage sweep, but two clear humps of different sizes observed in the both regions, during changing the bias polarity. The humps are disappeared when the voltage sweep was limited in a small voltage bias range (inset (a) of Fig. 32). According to Bourim et al., this humps are due to the switching polarization current due to the easy ferroelectric dipoles switching within less constrained PZT in the mesastructure, and they can take place only when the ferroelectric dipoles are fully reversed under a larger voltage sweep (>± 2.5 Volt). In addition, switching characteristics in bias pulse mode with alternating serial pulses of positive and negative polarity (inset (b) of Fig. 32) established that both the HRS and LRS arrived at a steady value immediately after reversing the pulse polarity. Also, good endurance was observed under alternating pulses of opposite polarity, as shown in inset (c) of Fig. 32.

3.3.2. Resistive switching effect in graphene oxide/$Pr_{0.7}Ca_{0.3}MnO_3$ films. Recently Kim et al. reported the grephene oxide (GO)/$Pr_{0.7}Ca_{0.3}MnO_3$ based resistive switching memory device prepared by a spin-coating method at a low temperature (<300°C) [107]. In this case GO is used as an insulating layer and conducting PCMO acts as an oxygen exchange layer, for its higher oxygen vacancy concentration at the surface region [107, 144–146]. The Pt/GO/PCMO/Pt device was fabricated on a Pt/Ti/SiO_2/Si substrate. 25 nm thick PCMO film was deposited using a spin-coating method using Mn, Ca, and Pr acetate hydrate

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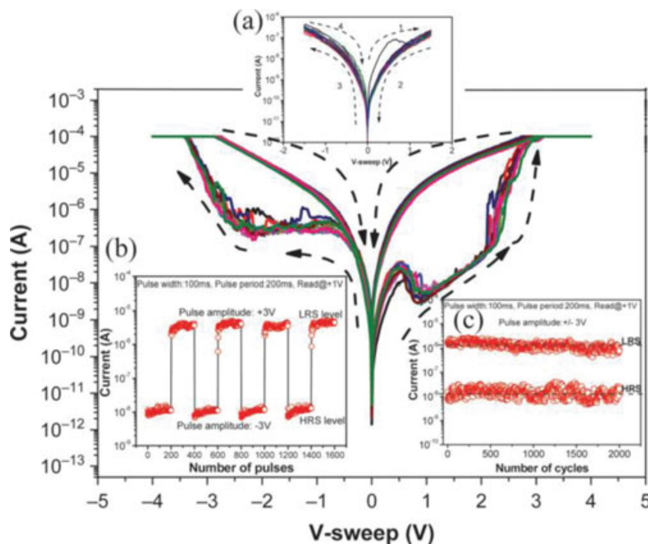

Figure 32. DC I–V hysteresis characteristics of the mesastructured Pt/PZT/PCMO(∼20 nm)/Pt device for 10 consecutive voltage sweeps cycles of 0→+4 Volt→0→−4 Volt→0. Arrows (dashed lines) indicate the sweeping directions and the current evolution. Inset (a) shows the I–V evolution for 10 consecutive voltage sweeps in a short voltage sweep range of 0→+1.5 Volt→0→−1.5 Volt→0. Insets (b) and (c) show switching characteristics in voltage pulse mode (Pulse amplitude: ±3 Volt, pulse width: 100 ms, pulse period: 200 ms and read voltage at +1 Volt) [after ref. 110].

as the source material and 2-methoxyethanol, acetic acid as the solvent. The 30-nm thick graphene oxide was spin-coated on the PCMO layer using a solution containing grapheme oxide particles with H_2O solvent. The film was annealed at 150°C for 30 min using rapid thermal annealing (RTA) process. Finally, Pt top electrodes were deposited by electron beam evaporation.

Figure 33(a) shows the I–V curve for the Pt/GO/PCMO/Pt device, sweep at +1.3 Volt to −1.3 Volt. In this case no forming process was necessary to switch on the device. The set/ reset voltage of the device are ∼ − 0.75 Volt and 0.6 Volt, respectively. In contrast, the Pt/PCMO/Pt control sample showed no resistive switching behavior. Mostly PCMO is

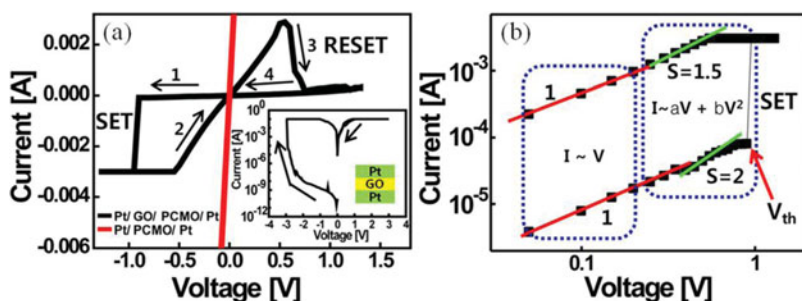

Figure 33. (a) Typical I–V hysteresis curves of the GO/PCMO and PCMO device. The inset shows I–V hysteresis curve of the Pt/GO/Pt device. (b) I–V plot of HRS and LRS of the GO/PCMO device in Log scale [after ref. 107].

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considered as a *p*-type material and forms Ohmic contact with Pt, since the work function of Pt (5.65 eV) or $SrRuO_3$ (5.2 eV) is higher than the electron affinity of PCMO (4.9 eV) [107, 109, 143, 147]. In the previous section, Chen *et al.,* reported that the Pt/PCMO/Pt structure can also show resistive switching behavior [106]. This can be explained clearly by the effect of oxygen vacancy and resistivity of the PCMO material. The sputtered deposited PCMO film of Chen *et al.* [106] should be oxygen reach. I–V characteristic of the Pt/GO/Pt device shows an irreversible permanent breakdown, as shown in inset of Fig. 33(a). Therefore, it is cleared that the main switching behavior for this chemically fabricated structure is due to the oxygen ions movement between two active layers. To realize the conduction mechanisms during set process the curve is replotted in log scale as shown in Fig. 33(b). At low voltage ($<V_{on} \approx 0.35$ Volt) the I–V curve shows Ohmic behavior in the negative sweep region, because the density of thermally generated free carriers inside the films is predominant over the injected charge carriers. The slope (S) increases to 2, indicating trap-associated space charge limited current (SCLC) theory. When applied voltage reaches the threshold voltage (V_{th}), the current increases rapidly due to trap-filled condition. The logI–logV plot exhibits linear Ohmic conduction, followed by a SCLC conduction, which corresponds to the Child's law region [107, 148]. Very stable retention up to 10^4 second was observed in this Pt/GO/PCMO/Pt device at 85°C without any degradation. Compared to the other graphene oxide based memory [107, 145, 146], they obtained the

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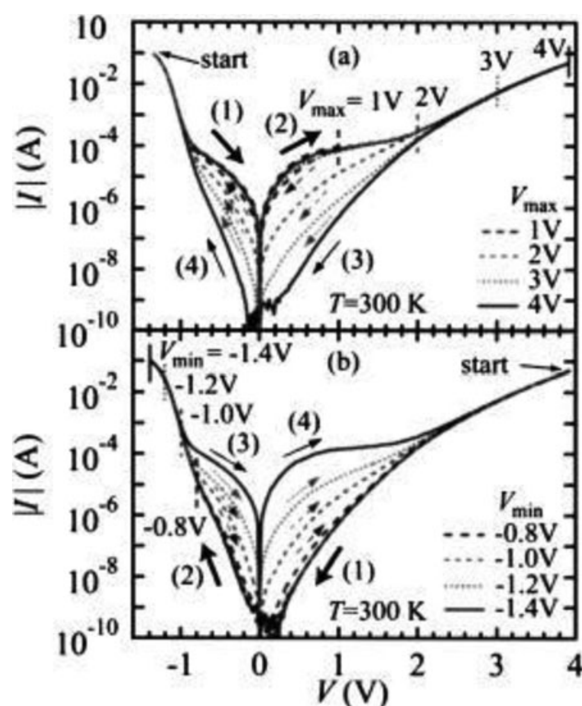

Figure 34. Hysteretic *I–V* characteristics of a SRO/Nb:STO junction measured with different spans of voltage scan. Bias voltage was swept as (a) -1.4 V$\rightarrow$0 V$\rightarrow V_{max}\rightarrow$0 V$\rightarrow -1.4$ V with V_{max} varied as 1, 2, 3, and 4 V, and (b) 4 V$\rightarrow$0 V$\rightarrow V_{min}\rightarrow$0 V$\rightarrow$4 V with V_{min} varied as -0.8, -1.0, -1.2, and -1.4 V. In both cases, chronological sequence of *I–V* curves is represented from (1) to (4) [after ref. 104].

high temperature retention property by incorporating PCMO layer. The evolution of two well-resolved resistance states over 150 cycles was observed from the pulse endurance measurement.

4. Resistance Switching in $SrTiO_3$ Based Film

4.1. Resistance Switching Effect in $SrRuO_3/SrTi_{0.99}Nb_{0.01}O_3$ Junction

Fuji *et al.* [104], reported about the resistive switching effect in a $SrRuO_3$ (SRO) and $SrTi_{0.99}Nb_{0.01}O_3$ (Nb:STO) junctions. Epitaxial SRO thin films (100 nm) were grown on (001) Nb:STO single-crystal substrates by a pulse laser deposition (PLD). The films were annealed at 400°C for 30 minute in oxygen ambient at high pressure.

A large hysteresis in *I–V* characteristics with distinct HRS and LRS are observe at low forward and reverse bias voltage, as shown in Fig. 34(a). As can be seen from the figure, the junction switched to LRS by applying −1.4 Volt bias scan and the junction turned to HRS again by applying 4 Volt bias. Two resistance states were kept unchanged when voltage polarity is changed through 0 Volt [(1)→(2)→(3)→(4)]. *I–V* curve (4) at HRS during set process is nearly a straight line, agreeing with a Schottky barrier model. The junction gives leaky *I–V* characteristics during reset process at positive voltage direction. To understand the evolution of hysteresis by widening the voltage scan span, in Fig. 34(a), the bias voltage was swept as −1.4 Volt→ 0 Volt→V_{max}→0 Volt→−1.4

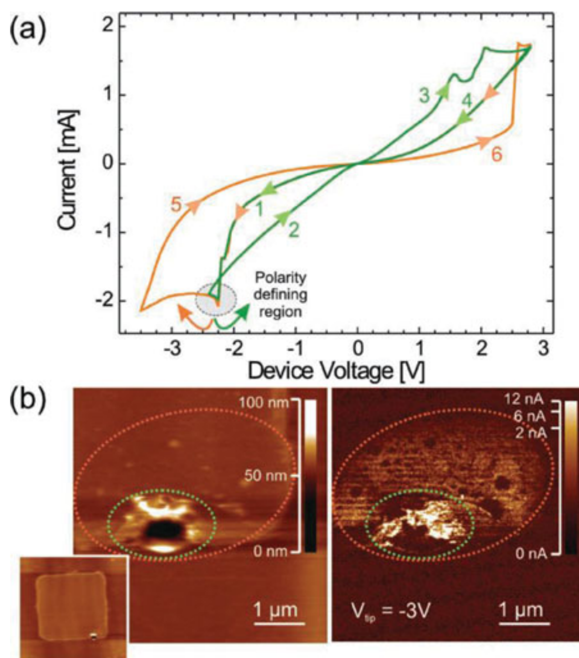

Figure 35. (a) I–V switching characteristic of a Fe-doped $SrTiO_3$ thin film. Two types of switching behaviour exhibiting opposite polarities can be seen in one and at the same junction. (b) Conductive AFM topography and current image of a junction after electroforming and top electrode removal. A well conducting crater (green) as well as a medium conducting region around the crater (orange) is shown [after ref. 105].

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Volt with V_{max} varied as 1, 2, 3, and 4 Volt, where the junction was reset to LRS at the initial stage [see branches of (1) and (2)]. When V_{max} was 1 Volt, the LRS was hardly switched to HRS. As the V_{max} was increased from 2 to 4 Volt, the junction was transformed gradually to HRS [see branches (3) and (4)] and the hysteresis switching window was opened, resulting in the current differences over two orders of magnitude at low voltage regions. In Fig. 34(b), the bias voltage was swept as 4 Volt$\rightarrow$0 Volt$\rightarrow V_{min}\rightarrow$0 Volt$\rightarrow$4 Volt with V_{min} varied as -0.8, -1.0, -1.2, and -1.4 Volt. In a similar manner to the cases of Fig. 40(a), was observed. Therefore, the barrier height reduction and an opening of conducting current path can be developed at appropriate voltage and the path can be ruptured at appropriate reverse bias. When the junction was stressed by voltage pulses, the resistance states was switched between rather steady HRS and variable LRS.

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4.2. Resistive Switching in Fe Doped $SrTiO_3$ Film

The resistive switching property of the Fe-doped $SrTiO_3$ films was reported by Muenstermann *et al.* [105]. By using conductive AFM, they probed the coexistence of a filamentary and an area-dependent switching process. A 500 nm thick 1 at% Fe-doped $SrTiO_3$ thin film switching layer was grown on a metallic single crystal substrate (1at% Nb-doped $SrTiO_3$) by PLD, followed by Pt top electrodes were used to form MIM structure. The initial forming process is required to activate the devices. Fig. 35(a) shows the I–V switching characteristics of this said device. Sweeping starts at 0 Volt to -2.2 Volt, the curve follow the path “1”. If, in a next sweep, the voltage is swept back from -2.2 Volt to 0 Volt (curved green arrow) the sample switches into a LRS (path “2”). Going up to 2.8 Volt and then back to 0 Volt again, to completes the full switching cycle. A stable resistive switching state, shown in green line, is found (1-2-3-4-1), called “counter eightwise” polarity. If, however, the sample resides in branch “1” and (upon reaching -2.2 Volt), the voltage is swept further down to -3.5 Volt, a higher resistance state is reached (branch “5”, orange arrow curve). Going back to positive voltages reverses this switching again (branch “6” to branch “4”). Keeping this higher negative voltage amplitude, a stable second type of switching can be achieved, shown in orange curve (1-5-6-4-1) showing an “eightwise” polarity. Both types of switching occur in the same pad. A repeatable change between both curves can be induced by adjusting the negative voltage amplitude back and forth again. This unusual *I-V* characteristic is reproducible [105, 149]. The two key differences can be stated from these types switching curves (orange and green one). The first one is the dissimilarity in switching polarities (“eightwise” vs. “counter eightwise”) of both curves. Another is the both types of switching differences exhibit different electrode area scaling behaviour: the “counter eightwise” switching type demonstrates no discernable junction size dependence (hinting at a filamentary switching nature). Using definite forming circumstances, Muenstermann et al. fabricate device showing only the “eightwise” switching type.

The underlying surface properties were investigated with conductive AFM (C-AFM). To study the C-AFM, Pt TE was removed completely by gentle way, after forming and switching at several junctions. Fig. 35(b) shows the C-AFM topography and local current distribution of a junction after electroforming process. Inset shows the entire junction area, while the main topography and current images are the magnifications of the lower right part of the junction area. Most of the surface region is smooth and has not been structurally altered by the electroforming step. Only a small region in the lower right part of the junction shows some deformation. Nearly 1 μm wide crater-like structure observed

(marked by a green dashed line). By comparing this image with the images taken of a virgin junction (showing only smooth topography) it can be assumed that the crater is developed during electroforming. The conductivity of the formed junction is measured at a tip bias of −3 Volt, as shown in the right hand side of Fig. 35(b) and is confined near the crater. The crater itself is well conducting (marked in green line) and a somehow broadened area around the crater shows moderate conductivity (marked in orange line). Tip induced resistive switching as well as different resistance states also studied by them in details using C-AFM. The topographic images at four voltage quadrants also studied and explained to realize the resistive switching behavior.

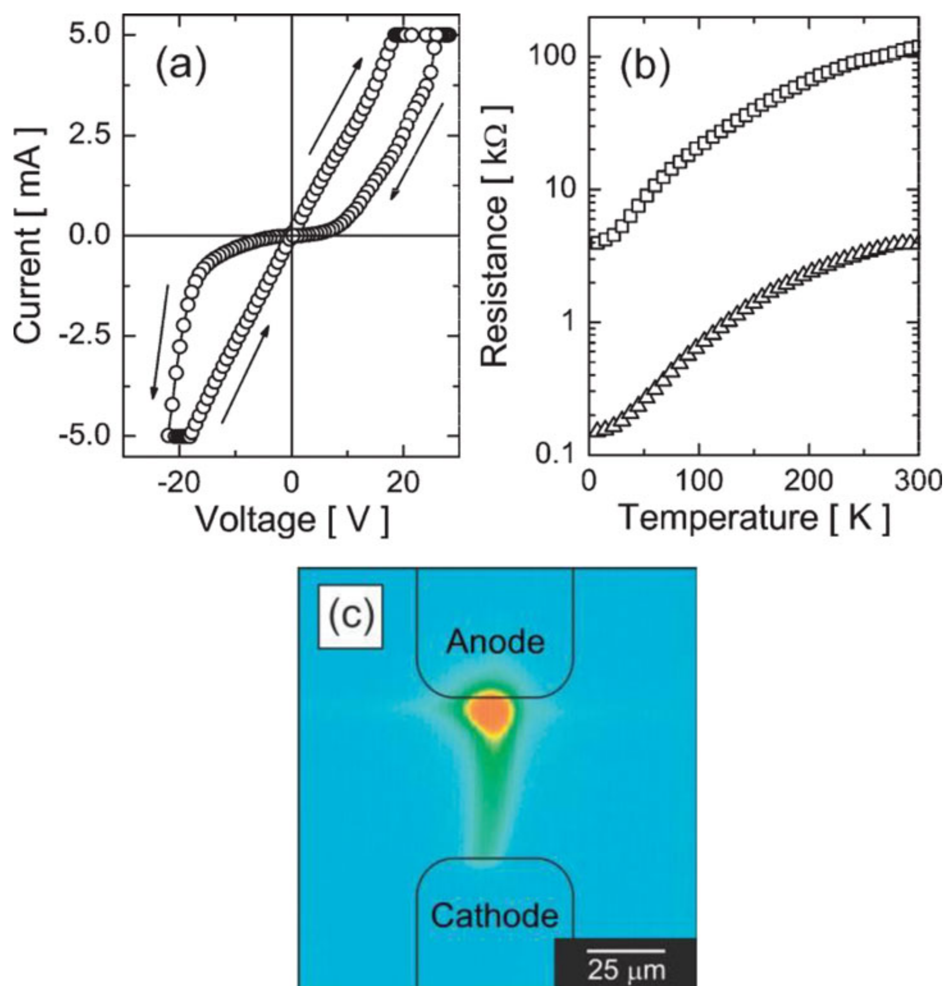

Figure 36. Bistable resistance state and current path in a Cr-doped $SrTiO_3$ single crystal memory cell. (a) I–V switching characteristics of the conditioned Cr-doped $SrTiO_3$ memory cell at ambient temperatures. (b) Temperature dependence of resistance for the LRS and HRS. (c) Infrared thermal image of the memory cell with a current of +5 mA at an applied voltage of 30 Volt. In the color scale, blue and red represent room temperature and elevated temperature, respectively. The electrodes used as anode and cathode for the conditioning process are indicated [after ref. 135].

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4.3. Resistive Switching in Cr-Doped STO Film

Janousch *et al.* [135] reported the role of oxygen vacancies on the resistive switching properties of chromium doped $SrTiO_3$ (Cr:STO) film. Recently, it was observed that $SrTiO_3$ doped with Cr can be conditioned such that it exhibits a bistable resistance state [124, 150–152]. Voltage pulses of opposite polarity switch the resistance of the perovskite reversibly between a HRS and LRS state.

The as-prepared single crystals 0.2 mol% Cr-doped $SrTiO_3$ memory devices, with a resistivity of $\rho > 10^{11}$ Ω-cm was used for this study. The initially insulating Cr-doped $SrTiO_3$ becomes conducting after conditioning process by exposing the crystal to an electrical field of 10^5 Vcm^{-1} for about 30 min. Fig. 36(a) shows the hysteresis I–V characteristics of a conditioned Cr:STO memory cell with a bistable resistance state. Fig. 36(b) displays the temperature dependence of the resistance of the memory cell in the LRS and HRS state. The decrease of resistance upon cooling in the both resistance states indicates the metallic behavior of the films. An infrared (IR) thermal image, as shown in Fig. 36(c), of the memory cell, collected while applying an electrical current of 5 mA at a bias voltage of 30 Volt, as a result ∼150 mW power dissipated in the memory cell. The false-color image in Fig. 36(c) reflects the temperature distribution of the memory cell. The temperature rises in a laterally confined path between the electrodes. Near the anode, the majority of the power is dissipated, reflected by the "hot spot". This indicates that the local resistance is highest in the vicinity of this anode.

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6. Conclusions

This review describes the resistive switching properties of perovskite oxide thin films, mainly three different types of memory element such as, $SrZrO_3$, $Pr_{0.7}Ca_{0.3}MnO_3$ and $SrTiO_3$. In RRAM the redox processes and ionic motion of the oxygen vacancies on the nanoscale play the key role for the switching. The review focuses on the present understanding of the factors which are affecting for the switching properties and types which need to be beat in order to utilize the thought in universal nonvolatile memories. The switching mechanism in the perovskite materials are deeply related to the switching mechanism of high-k oxides. In order to further explore the potential of those types of RRAM and to exploit their potential to the limits, a considerable research effort is still needed with respect to a deeper understanding of the microscopic mechanism of the switching. The crystal structure and fabrication process of the $SrZrO_3$ based memory structures are strongly affected in the switching parameters. On the other hand, the crystal structure of the SZO film is depends on the crystal structure of the bottom LNO electrode. Effects of post deposition annealing and measurement temperature on the resistive switching properties for the SZO based thin films have also reviewed here. The review also give a brief idea about the effect of different metal doping such as vanadium, chromium, molybdenum, niobium and iron, and effect of the doping concentration on resistive switching properties of these perovskite oxide materials. Role of oxygen on the switching properties has been reviewed by modifying the device structure to bilayer oxygen reach and oxygen deficient and inserting another oxide reach or deficient layer such as grapheme based oxide layer, on the perovskite structures. For the SZO based memory system the nonpolar switching properties observed by tuning the oxide thickness to ∼20 nm. In particular, the effects between the chemical, thermal, and electronic phenomena involved in the resistive switching mechanisms discussed briefly in this review are only elucidated to a very small degree. However, the gradually increasing number of outstanding publications by groups all over

the world is a promising indication that this challenging mission has been acknowledged and adopted.

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