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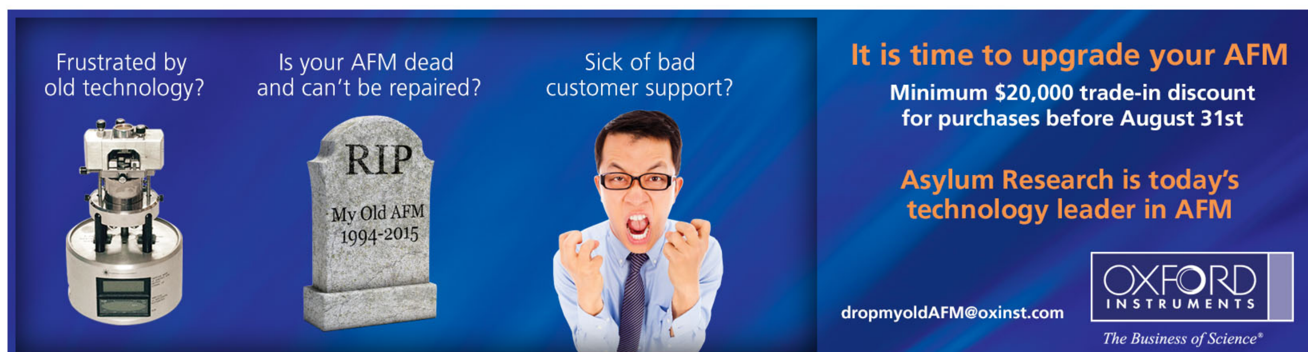

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Influence of an anomalous dimension effect on thermal instability in amorphous-InGaZnO thin-film transistors

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This paper investigates abnormal dimension-dependent thermal instability in amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistors. Device dimension should theoretically have no effects on threshold voltage, except for in short channel devices. Unlike short channel drain-induced source barrier lowering effect, threshold voltage increases with increasing drain voltage. Furthermore, for devices with either a relatively large channel width or a short channel length, the output drain current decreases instead of saturating with an increase in drain voltage. Moreover, the wider the channel and the shorter the channel length, the larger the threshold voltage and output on-state current degradation that is observed. Because of the surrounding oxide and other thermal insulating material and the low thermal conductivity of the IGZO layer, the self-heating effect will be pronounced in wider/shorter channel length devices and those with a larger operating drain bias. To further clarify the physical mechanism, fast I_D-V_G and modulated peak/base pulse time I_D-V_D measurements are utilized to demonstrate the self-heating induced anomalous dimension-dependent threshold voltage variation and on-state current degradation. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4897236]

I. INTRODUCTION

Recently, portable electronic products have been widely applied for consumer uses, especially those using low power consumption IC,[1–3] non-volatile memory,[4–34] and thin film transistors (TFTs).[35–39] Recently, transparent oxide-based semiconductors, such as ZnO and amorphous indium-gallium-zinc-oxide (a-IGZO), have attracted much attention due to their considerable potential applications in flat, flexible, and transparent displays.[40,41] In particular, a-IGZO TFTs possess advantageous properties such as high mobility, excellent uniformity, good transparency to visible light, and low process temperature, making them a promising candidate to be adopted in the next generation of the display industry.[41–43] Therefore, they are very promising alternatives to replace amorphous silicon TFTs for application in active matrix liquid crystal displays (AMLCD) and organic light-emitting diode displays (AMOLED) as switching/driving devices. However, there are some difficulties which are necessary to overcome for oxide TFTs to be practical in these applications, such as instability under gate bias stress, light illumination, or the surrounding ambiance.[44–47] Moreover, a-IGZO TFTs can also be used for gate driver on array (GOA) technology. Conventionally, driving ICs have been fabricated through CMOS technology and mechanically attached to the sides of the panel. However, GOA technology fabricates gate driver ICs on the array itself instead of attaching them to the panel sides. As a result, GOA technology can reduce process steps and cost as well as achieve thinner panels with narrower edges to realize slim border displays.[48,49] However, mobility of driving ICs fabricated by single crystal silicon is about one hundred times that of a-IGZO. As a result, in order to achieve the same driving current, it is necessary to increase channel width and/or decrease channel length of a-IGZO TFTs for GOA operation. However, the degree to which channel length can be decreased is restricted by photolithography. As a result, increasing channel width is a better way to increase driving current. Therefore, investigating the performance and reliability of a-IGZO TFTs with large channel width is of great importance.

II. EXPERIMENT

Back-channel-etching structured n-type a-IGZO TFTs were fabricated on a glass substrate in this work. The double-layer Cu/Mo (500/20 nm) gate electrode films were deposited and then patterned via photolithography on a glass substrate. Then 300-nm-thick Si_3N_4 and 70-nm-thick SiO_2 gate dielectric films were sequentially deposited on the patterned gate electrode by plasma enhanced chemical vapor

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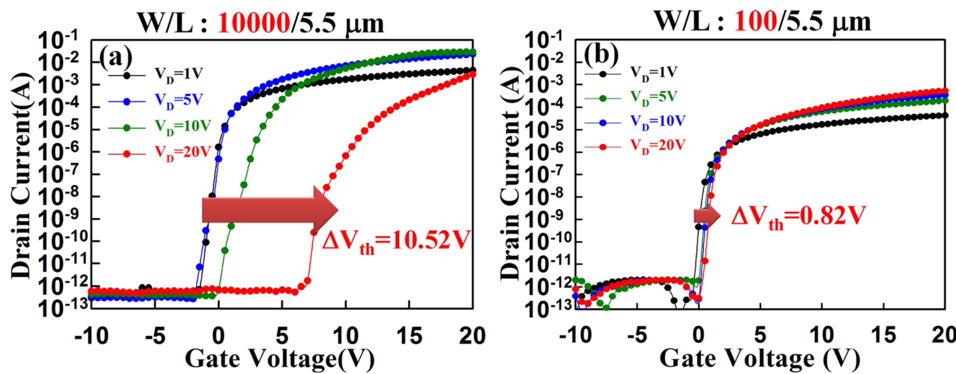

FIG. 1. I_D-V_G transfer characteristic of a-IGZO TFT operated at $V_D = 1$, 5, 10, and 20 V for: (a) W/L = 10 000/5.5 μm and (b) W/L = 100/5.5 μm.

deposition (PECVD). An active layer of 30-nm-thick a-IGZO film was deposited by DC magnetron sputtering using a target of In_2O_3:Ga_2O_3:ZnO = 1:1:1 in atomic ratio at room temperature, and then patterned. The Mo/Cu (20/500 nm) source/drain electrodes were formed by DC-sputtering and then patterned. Finally, 160-nm-thick SiO_2 and 50-nm-thick Si_3N_4 were sequentially deposited as a passivation layer by PECVD. After that the device was annealed in an oven at 300 °C for 2 h in a dark environment. In this paper, the conventional and fast I-V measurements were performed by Agilent B1500A and Agilent B1530A semiconductor analyzers, respectively. The device dimensions of channel width/length (W/L) were 100, 200, 500, 1000, 5000, and 10 000 μm/5.5, 6, 10, 15, and 20 μm. The threshold voltage is defined as the gate voltage when the normalized drain current ($NI_D = I_D \times L/W$) reaches 1 nA, where L and W are channel length and width, respectively. All measurements were performed in a dark environment.

III. RESULT AND DISCUSSION

Figures 1(a) and 1(b) show the I_D-V_G curve at $V_D = 1$, 5, 10, and 20 V, with W/L = 10 000/5.5 μm for Figure 1(a) and W/L = 100/5.5 μm for Figure 1(b). Obviously, threshold voltage increases with increasing drain voltage. Furthermore, the larger the channel width, the larger threshold voltage that can be observed. Conventionally, channel width and drain voltage do not affect threshold voltage in long channel devices. However, an anomalous threshold voltage variation is observed in Figures 1(a) and 1(b).

In order to better understand the dimension and drain voltage-dependent threshold voltage variation, Figures 2(a) and 2(b) characterizes threshold voltage versus various channel lengths at low ($V_D = 1$ V) and high ($V_D = 20$ V) drain voltages for the W = 100 and 10 000 μm devices. Clearly, at low measurement drain voltage ($V_D = 1$ V), both W = 100 and 10 000 μm devices with various channel lengths have nearly the same threshold voltage. On the other hand, at a high measurement drain voltage ($V_D = 20$ V), threshold voltage is also independent of channel length for the device with relatively small channel width (W = 100 μm) but exhibits dimension-dependent threshold voltage variation for the device with relatively large channel width (W = 10 000 μm). In previous literatures, threshold voltage shift results from electrons trapping at the IGZO/SiO_2 interface or in SiO_2 bulk under positive gate bias stress (PGBS),[50–53] or high current stress.[54,55] However, in our research, we found that threshold voltage increases at a shorter channel length for devices with large channel width and operated at high drain voltage (Figures 1 and 2) without imposing stress biases, unlike that found in previous literature.

To further inspect this anomalous phenomenon and explain more precisely, Figure 3(a) illustrates the threshold voltage shift versus various channel widths and drain voltages at a fixed channel length (L = 5.5 μm). Similarly, Figure 3(b) shows the threshold voltage shift versus various channel length and drain voltages, but at a fixed channel width (W = 10 000 μm). Threshold voltage shift is defined as V_{th}(measurement)-V_{th}(at $V_D = 1$ V). Note that at low drain voltage ($V_D = 5$ V), threshold voltage shift is negligible and unapparent, with the same being true for relatively small channel widths (W = 100 μm) and/or relatively long channel lengths (L = 20 μm) at all drain voltages, as shown in Figures 3(a) and 3(b). When W ≧ 500 μm, L ≦ 10 μm, and V_D ≧ 10 V, a significant threshold voltage shift can be observed with increased channel width and increased drain voltage, or with decreased channel length and increased drain voltage. Accordingly, it is reasonable to speculate that

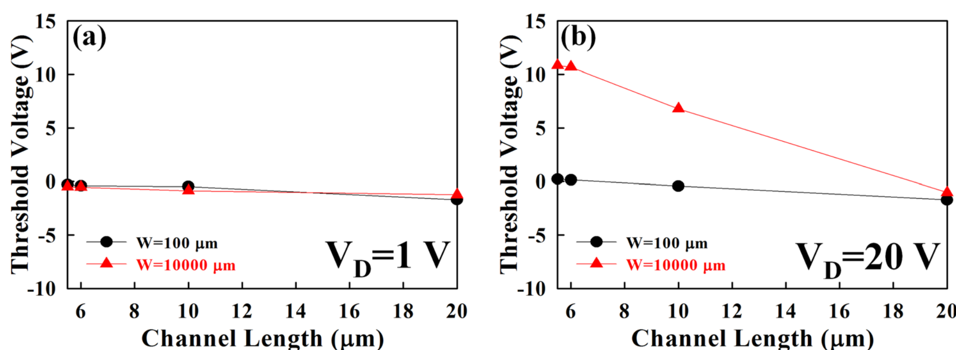

FIG. 2. Threshold voltage dependent on channel length, with W = 100 and 10 000 μm at (a) $V_D = 1$ V (b) $V_D = 20$ V.

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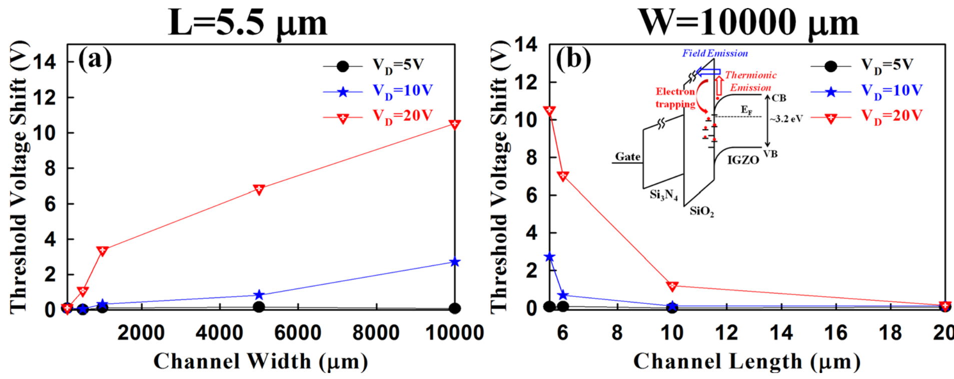

FIG. 3. Dependence of threshold voltage shift on drain voltage and (a) channel width and (b) channel length. The inset of (b) illustrates the thermionic-field emission process of electron trapping.

the abnormal dimension-dependent threshold voltage variation may in fact be induced by the self-heating effect.[56] It is well known that the self-heating effect arises in silicon-on-insulator (SOI) MOSFETs and low-temperature-polycrystalline silicon (LTPS) TFTs because the surrounding oxide or other thermal insulating materials make it difficult to dissipate the heat generated in the active layer when high current flows through the channel, a situation quite similar to that found in the IGZO channel layer.[57] In addition, the thermal conductivity of IGZO is much lower than Si and is comparable to SiO_2. Therefore, heat dissipation in IGZO TFTs is relatively more difficult than in Si-based TFTs.[58,59] Because the larger drain voltage will form a higher drain current, resulting in higher power ($P = IV$), the heat in channel will be higher, resulting in a more severe self-heating effect. Furthermore, because the temperature is highest at the center of the channel region and the heat dissipate to the surrounding materials along the channel width direction, larger channel widths make heat dissipation in the channel more difficult, again resulting in a more pronounced self-heating effect.[57,60] Moreover, the shorter the channel length, the higher drain current flowing through the channel, resulting in more heat generated in the channel. As a result, either a larger channel width or a shorter channel length combined with a higher operated drain bias will induce a more severe self-heating effect, resulting in more pronounce threshold voltage shift. The inset of Figure 3(b) shows the energy band diagram. When the large channel width and/or short channel length TFT is operated at high drain voltage, significant self-heating effect will occur, and channel electrons will be trapped at the IGZO/SiO_2 interface or in SiO_2 bulk through the thermionic-field emission process, resulting in a larger observed threshold voltage.[54–56] In addition, from Figure 1(a), note that threshold voltage shifts with a small variation of the slope in the transfer characteristics. This indicates that some shallow sub-conduction band trap states are created at the IGZO active layer/gate dielectric interface during the self-heating-induced trapping process, resulting in a small amount mobility and subthreshold swing degradation. However, this small amount of subthreshold swing and mobility degradation cannot explain the very large threshold voltage variation. The dominant mechanism of threshold voltage variation may in fact results from the self-heating induced-charge trapping phenomenon.

To confirm the proposed self-heating effect-induced anomalous dimension and drain voltage-dependent threshold voltage variation, fast I_D-V_G measurement is performed. Figure 4(c) illustrates the waveform of the conventional

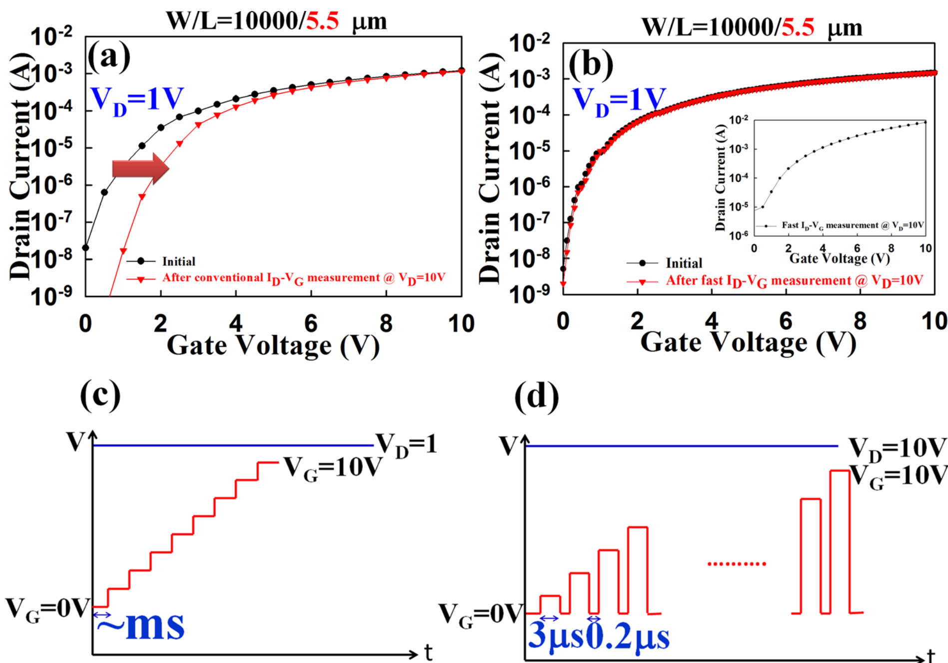

FIG. 4. The transfer characteristic of a-IGZO TFT with $W/L = 10\,000/5.5\ \mu m$ before and after measuring at high drain voltage ($V_D = 10$ V) by (a) conventional I_D-V_G measurement, and (b) fast I_D-V_G measurement. The inset in (b) illustrates the fast I_D-V_G curve. (c) and (d) show the waveform of conventional and fast I_D-V_G measurement, respectively.

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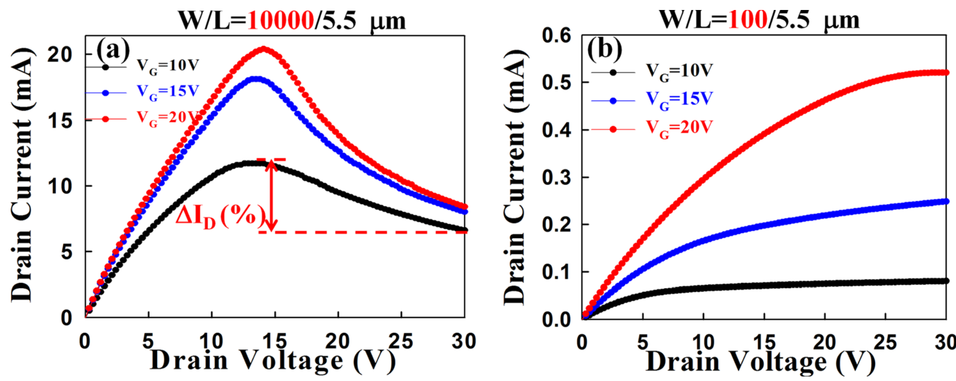

FIG. 5. I_D-V_D output characteristic of a-IGZO TFT operated at $V_G = 10$, 15, and 20 V for (a) W/L = 10 000/5.5 μm and (b) W/L = 100/5.5 μm.

I_D-V_G measurement, in which drain voltage is fixed with gate voltage performed stepwise. Note that the time scale of each gate voltage step is on the order of tens of milliseconds (ms). For comparison, Figure 4(d) shows the waveform of fast I_D-V_G measurement, in which drain voltage is fixed with gate voltage performed in a pulse. Significantly, the time scale of peak/base time is rather short, approximately on the order of microseconds (μs). Note that the inset of Figure 4(b) shows the fast I_D-V_G curve, which exhibits good switching characteristics, indicating that the gate capacitance can become effectively charged during the fast I_D-V_G measurement. From previous research,[54] sufficient heating time is necessary for Joule heating to take place within the channel, resulting in a pronounced self-heating effect-induced charge trapping phenomenon. This sufficient heating time is approximately on the order of tens of ms. Because the gate pulse peak/base time in fast I_D-V_G measurement is on the order of μs, the short heating time is insufficient for Joule heating to occur. Therefore, use of the fast I_D-V_G measurement will exclude the self-heating effect induced-charge trapping phenomenon, and therefore threshold voltage shift can also be excluded. The measurement sequences of Figures 4(a) and 4(b) are as follows. First, the I_D-V_G curve is measured by conventional I_D-V_G measurement at low drain voltage ($V_D = 1$ V) to avoid the self-heating effect and act as the initial state. Second, the I_D-V_G curve is measured at high drain voltage ($V_D = 10$ V) by conventional I_D-V_G measurement for Figure 4(a), or by fast I_D-V_G measurement for Figure 4(b). Finally, the I_D-V_G curve is measured by conventional I_D-V_G measurement at low drain voltage ($V_D = 1$ V) to serve as the final state. Clearly, there is a positive threshold voltage shift between initial and final states after conventional I_D-V_G measurements at high drain voltage ($V_D = 10$ V), as shown in Figure 4(a). During the conventional I_D-V_G measurement ($V_D = 10$ V), there was sufficient heating time for Joule heating to occur, leading to the self-heating effect-induced charge trapping phenomenon and resulting in the threshold voltage shift between initial and final states. Conversely, during the fast I_D-V_G measurement ($V_D = 10$ V), the insufficient heating time required for Joule heating results in no threshold voltage shift being observed, as shown in Figure 4(b). The fast I_D-V_G measurement further corroborates that the abnormal dimension and drain voltage- dependent threshold voltage variation does in fact result from the self-heating effect-induced charge trapping phenomenon.

Figures 5(a) and 5(b) show the I_D-V_D output characteristic at a fixed channel length (5.5 μm) and different channel widths (10 000 μm and 100 μm, respectively). Compared to the W = 100 μm device, the W = 10 000 μm one exhibits an anomalous output characteristic. When the measurement drain voltage exceeds approximately 15 V, drain current decreases instead of saturating with an increase in drain voltage.

To provide insight into this anomalous on-state current degradation phenomenon, we define on-state current degradation percentage (ΔI_D %) as [$I_{D,max}$(measurement)-I_D(at $V_D = 30$ V)]/$I_{D,max}$(measurement). Figure 6 shows the dependence of on-state current degradation (%) on channel width and length. Clearly, on-state current degradation (%) increases with increasing channel width and/or decreasing channel length. From previous discussions, it is reasonable to speculate that this abnormal on-state current degradation may be induced by the self-heating effect. The heat dissipation in channel will be rather difficult for the larger channel width devices, and the current flowing through the channel will be larger with the shorter channel length devices, resulting in more heat accumulation in the channel. As a result, a severe self-heating effect-induced charge trapping phenomenon will occur, resulting in a considerable threshold voltage shift. Because of this large threshold voltage shift, the abnormal drain current decreases as drain voltage increases when $V_D \geqq 15$ V, as shown in Figure 5(a).

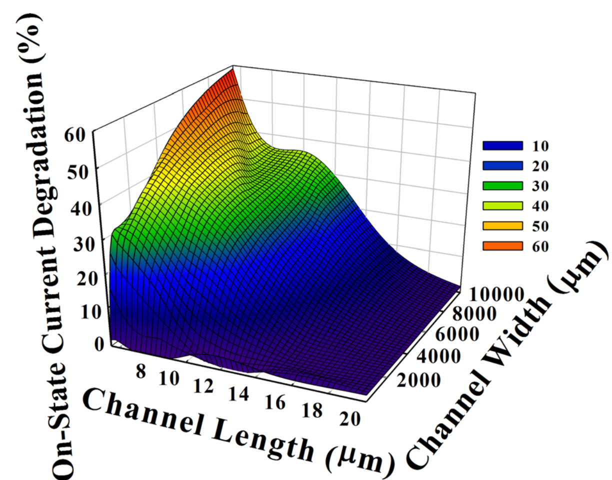

FIG. 6. Dependence of on-state current degradation on channel width and length.

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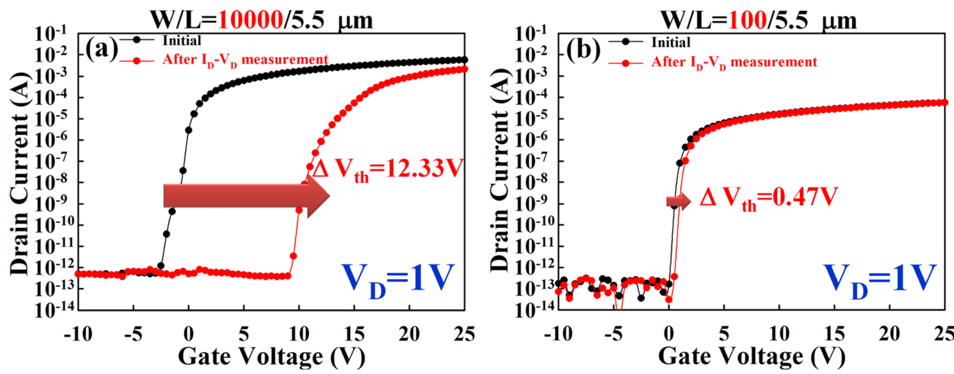

FIG. 7. I_D-V_G transfer characteristic of a-IGZO TFT before and after I_D-V_D measurement for (a) W/L = 10 000/5.5 μm and (b) W/L = 100/5.5 μm.

In order to confirm the on-state current degradation results from this self-heating effect-induced charge trapping phenomenon, a measurement sequence was designed as Figures 7(a) and 7(b). First, the I_D-V_G curve is measured at low drain voltage ($V_D = 1$ V) to avoid the self-heating effect and act as the initial state. Second, the I_D-V_D curve is measured. Finally, the I_D-V_G curve is measured at low drain voltage ($V_D = 1$ V) to serve as the final state. Clearly, there is a positive threshold voltage shift between initial and final states after I_D-V_D measurements for the large channel width (W = 10 000 μm) device, as shown in Figure 7(a). During the I_D-V_D measurement, the high drain voltage region ($\sim V_D \geqq 15$ V) will generate high drain current, resulting in more heat accumulating in the channel, leading to the self-heating effect-induced charge trapping phenomenon and resulting in the threshold voltage shift between initial and final states. On the contrary, because heat dissipation is relatively easy for the small channel width (W = 100 μm) device, there is a much smaller threshold voltage shift between initial and final states for the W = 100 μm device.

To further corroborate the proposed mechanism, the pulse I_D-V_D measurement (various peak/base times) was adopted, as shown in Figure 8. Figure 8(a) shows the dependence of on-state current degradation on peak time at a fixed base time (10 ms), while (b) shows this dependence on base time at fixed peak time (50 ms). The insets of Figures 8(a) and 8(b) illustrate the waveform of the drain pulse. Figure 8(c) shows the conventional I_D-V_D measurement and pulse I_D-V_D measurements. In conventional I_D-V_D measurement, gate voltage is fixed with drain voltage performed stepwise. Note that the time scale of each drain voltage step is on the order of tens of milliseconds (ms). For comparison, in pulse I_D-V_D measurement, gate voltage is fixed with drain voltage performed in a pulse form, and we can modulate various peak/base times to extract the on-state current degradation at various drain pulses. Previous research[54] has indicated that sufficient heating time is necessary for Joule heating to take place within the channel, resulting in a pronounced self-heating effect-induced charge trapping phenomenon. As a result, if on-state current degradation does indeed result from self-heating effect-induced charge trapping phenomenon, the deterioration degree should decrease as the heating time, i.e., the peak time, decreases. As shown in Figure 8(a), when the peak time is 50 ms, the degradation approaches that of conventional I_D-V_D measurement, and the degradation decreases when the peak time decreases. When

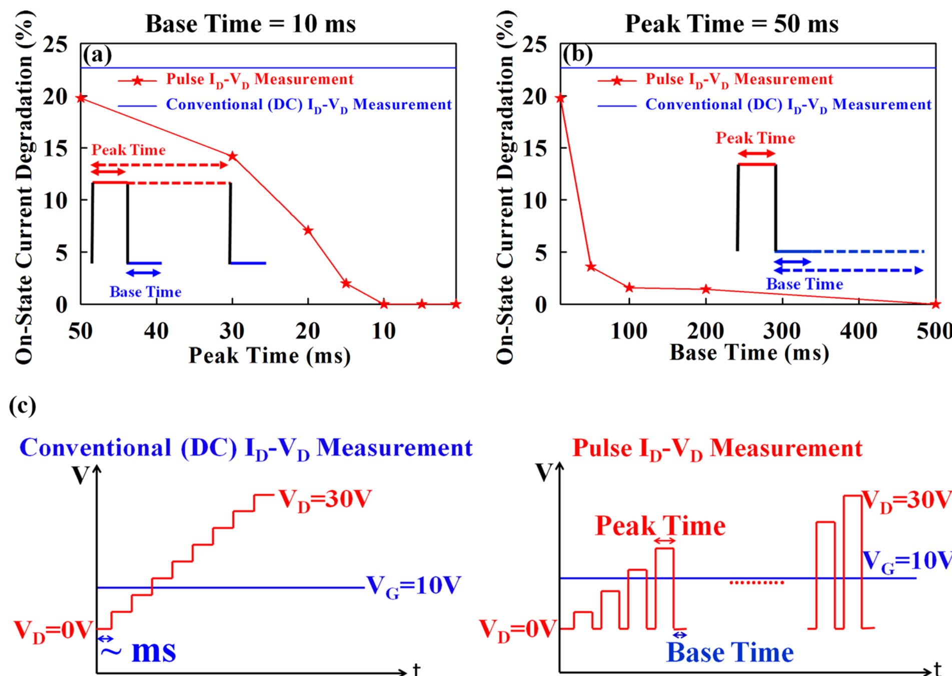

FIG. 8. Dependence of on-state current degradation on (a) peak time (fixed base time = 10 ms) and (b) base time (fixed peak time = 50 ms). The insets of (a) and (b) show the waveforms of drain pulse at various peak times (fixed base time) and various base times (fixed peak time), respectively. (c) Schematic diagrams of conventional and pulse I_D-V_D measurement.

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the peak time is smaller than 10 ms, no on-state current degradation is observed. Furthermore, from previous literature, cooling time is also an important factor influencing the Joule heating to occur within the channel.[55] As a result, if on-state current degradation does indeed result from the self-heating effect-induced charge trapping phenomenon, the deterioration degree should decrease as the cooling time, i.e., the base time, increases. As shown in Figure 8(b), when the base time is 10 ms, the deterioration approaches that of conventional I_D-V_D measurement, and decreases when the base time increases. When the base time is larger than 500 ms, an insignificant amount of on-state current degradation is observed. This comparison of conventional and pulse (various peak/base time) I_D-V_D measurements further corroborates that the abnormal dimension-dependent on-state current degradation does in fact result from the self-heating effect-induced charge trapping phenomenon. Note that the effective cooling time is much longer than the effective heating time, at least by a factor of twenty. This is because the thermal conductivity of IGZO is much lower than Si and is comparable to SiO_2. Therefore, heat dissipation in IGZO TFTs is relatively more difficult than in Si-based TFTs.

IV. CONCLUSION

The anomalous dimension effect on thermal instability in a-IGZO TFTs has been investigated. Devices with larger channel widths and/or shorter channel lengths and which are operated at higher drain voltages will produce larger threshold voltages and more severe on-state current degradation, with the effect becoming even more pronounced as channel width or drain voltage increases and/or channel length decreases. This is due to the surrounding oxide and other thermal insulating material and the low thermal conductivity of the IGZO layer. The more pronounced self-heating effect is a product of both the more difficult heat dissipation in wider channels as well as the higher drain current in devices operated at higher drain voltages and shorter channel length. Because sufficient heating time (approximately on the order of tens of ms) is necessary for Joule heating to take place within the channel, the fast I_D-V_G and modulated various peak/base pulse time I_D-V_D measurements are performed to confirm the proposed mechanism. Because the time scale of the peak/base time in the fast I_D-V_G measurement is shorter, on the order of μs, the heating time is insufficient for Joule heating, resulting in no observed threshold voltage shift. The fast I_D-V_G measurement confirms that the abnormal dimension-dependent threshold voltage variation is due to the self-heating effect induced-charge trapping phenomenon. Furthermore, the pulse I_D-V_D measurement again demonstrates that the abnormal dimension-dependent threshold voltage variation and on-state current degradation indeed results from the self-heating effect induced-charge trapping phenomenon. Further, the effective cooling time is much longer than the heating time, indicating that IGZO is a low thermal conductivity material compared to Si, and is comparable to SiO_2. From this research, device dimension is a significant factor that governs the thermal instability of a-IGZO TFTs for the use of GOA technology. How to lessen or even eliminate the self-heating effect induced charge trapping phenomenon is of great importance for GOA technology.

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