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Citation: Applied Physics Letters **105**, 143505 (2014); doi: 10.1063/1.4896995
View online: http://dx.doi.org/10.1063/1.4896995
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/105/14?ver=pdfcov
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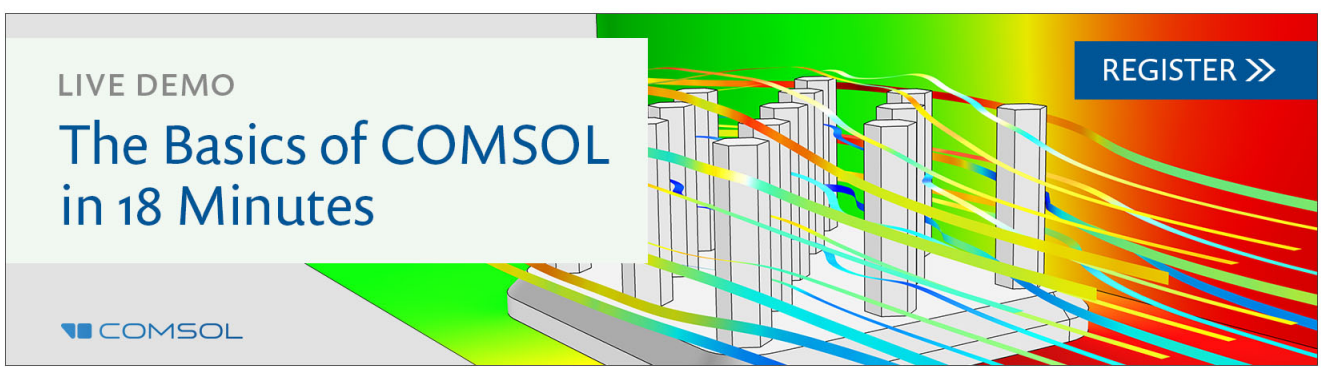

Electron-electron scattering-induced channel hot electron injection in nanoscale n-channel metal-oxide-semiconductor field-effect-transistors with high-k/metal gate stacks

Jyun-Yu Tsai,[1] Ting-Chang Chang,[1,2] Ching-En Chen,[3] Szu-Han Ho,[3] Kuan-Ju Liu,[1] Ying-Hsin Lu,[1] Xi-Wen Liu,[1] Tseung-Yuen Tseng,[3] Osbert Cheng,[4] Cheng-Tung Huang,[4] and Ching-Sen Lu[4]

[1]*Department of Physics, National Sun Yat-Sen University, Kaohsiung, Taiwan*
[2]*Advanced Optoelectronics Technology Center, National Cheng Kung University, Tainan, Taiwan*
[3]*Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan*
[4]*Device Department, United Microelectronics Corporation, Tainan Science Park, Tainan, Taiwan*

(Received 1 August 2014; accepted 20 September 2014; published online 7 October 2014)

This work investigates electron-electron scattering (EES)-induced channel hot electron (CHE) injection in nanoscale n-channel metal-oxide-semiconductor field-effect-transistors (n-MOSFETs) with high-k/metal gate stacks. Many groups have proposed new models (i.e., single-particle and multiple-particle process) to well explain the hot carrier degradation in nanoscale devices and all mechanisms focused on Si-H bond dissociation at the Si/SiO_2 interface. However, for high-k dielectric devices, experiment results show that the channel hot carrier trapping in the pre-existing high-k bulk defects is the main degradation mechanism. Therefore, we propose a model of EES-induced CHE injection to illustrate the trapping-dominant mechanism in nanoscale n-MOSFETs with high-k/metal gate stacks. © *2014 AIP Publishing LLC*.
[http://dx.doi.org/10.1063/1.4896995]

Consumer electronic products which combine display design,[1–4] memory circuits,[5–9] and IC circuits have become considerably more popular in the past few years. To achieve high speed, low gate leakage current, and power consumption, the continuous scaling down of metal oxide semiconductor field electrical field transistors (MOSFETs) is driving toward using high-k dielectric.[10–14] However, charge trapping in high-k gate stacks remains a key reliability issue, since it causes threshold voltage (V_{TH}) shift and drive current degradation[15–18] due to the filling of pre-existing high-k bulk defects.[19–21] Additionally, the issue of charge trapping effect has been found to have a great impact on hot carrier degradation (HCD), since hot carriers tend to be injected into the high-k layer, especially in short channel devices.[22,23] In long channel devices, maximum impact ionization (I.I.) condition-induced interface state generation is mainly located at the drain side and dominated the HCD. On the contrary, electron trapping dominates the HCD for short channel devices, and some studies believe that this electron trapping is due to avalanche hot electron (AHE) injection by I.I.[22,24] However, we use a short channel device which has a body current (IB) peak demonstrated that electron trapping was dominated by channel hot electron (CHE) injection rather than AHE injection at the high vertical field stress condition of gate voltage (V_G) = drain voltage (V_D). Furthermore, a model of electron-electron scattering (EES)-induced CHE injection is proposed to illustrate the charge trapping-dominant mechanism in nanoscale n-channel MOSFETs (n-MOSFETs) with high-k/metal gate stacks. In addition, positive bias stress (PBS) was used in this work to eliminate cold carrier injection from the channel region.

TiN/HfO_2 n-MOSFETs with an interlayer (IL) thickness of 10 Å were studied in this paper as an element of high-performance 28-nm complementary MOS technology. Devices were fabricated using a self-aligned transistor which progressed via the gate-last process. First, high quality thermal oxides with thicknesses of 10 Å were grown on a (100) Si substrate as an IL oxide layer. After standard cleaning procedures, 20 Å of HfO_2 film was sequentially deposited by atomic layer deposition followed by deposition of a poly-Si dummy gate. Next, self-aligned ion implantation was performed and then activated for source/drain at 1025 °C. After the removal of the dummy gate, 10 nm of TiN film was deposited by radio frequency physical vapor deposition. In this study, gate lengths (L) of 500 nm, 80 nm, and 35 nm were selected for the long and short channel devices investigation. The HCD condition for long channel devices was stress at $V_G \sim 1/2V_D$ with fixed $V_D = 2.7$ V, where maximum body current ($I_{B,max}$) occurred. For short channel devices, the stress conditions of L = 35 nm were $V_G = V_D = 1.8$ V, while for 80 nm they were at a varying V_G with fixed $V_D = 2.2$ V. The stress was briefly interrupted to measure the forward (F mode) linear drain current-gate voltage (I_D-V_G), reverse (R mode, source/drain interchanged) linear I_D-V_G, F mode saturation I_D-V_G, and R mode saturation I_D-V_G to monitor transconductance (Gm) and V_{TH} shift which was extracted at constant $I_D = 1\ \mu$A. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer and a Cascade M150 probe station.

Fig. 1 shows the I_D-V_G and corresponding Gm-V_G at the linear region measurement after HCD for short channel (L = 35 nm) high-k/metal gate n-MOSFETs. For the HCD, $V_G = V_D$ was the worst case condition for the nanoscale devices and degraded the sub-threshold swing (S.S.), the ON-state current (I_{ON}), and the Gm. More significantly, the V_{TH} shift was not totally caused by interface state generation, with electron trapping at the high-k layer also playing an important role. Moreover, the inset of Fig. 1 shows the

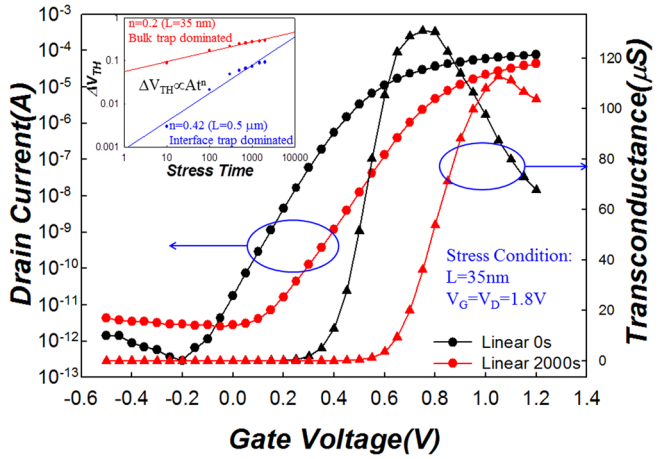

FIG. 1. I_D-V_G and corresponding Gm-V_G at linear region measurement. Inset shows the power law with a time exponent ~0.2 and ~0.42 for short and long channels, respectively.

power law with a time exponent ~0.2 for short channel devices ($L = 35$ nm), indicating that the degradation was dominated by charge trapping rather than interface state generation.[30,35] In contrast, the power law with a time exponent ~0.42 of long channel devices ($L = 0.5$ μm) indicates that the degradation was dominated by interface state generation rather than charge trapping.[25,29]

Figures 2(a) and 2(b) show the F mode I_D-V_G and the R mode I_D-V_G curves measured at the saturation region during HCD, respectively. It can observably find that they have similar V_{TH} shifts due to the electron trapping occurs above part of the channel and the energy band rises to form a barrier height at the channel, as shown in the inset of Figs. 2(a) and 2(b), which a phenomenon completely different from the long channel device. Moreover, it is also worthy to investigate how the electron could be trapped above part of the channel and extend to the drain side in the high-k layer after HCD. According to a previous study,[22] for short channel devices, the I.I. occurs not only at the drain side but also along the entire channel; thus, the electron trapping may be attributed to AHE injection by I.I. Furthermore, Fig. 2(d) shows I_B-V_G curves of long and short channel devices when V_D was fixed at certain stress voltages. It can be seen that the I_B (I.I. current) of the long channel device shows an I_B peak, which indicates that the largest I.I. rate occurs there. However, for the short channel device, I_B increases while V_G increases, so no I_B peak occurs. This phenomenon may suggest that electron trapping comes from AHE generation by I.I., especially since the stress V_D in the nanoscale channel could deplete most of channel region and lead to a strong electric field almost entirely distributed along the channel, as shown in Fig. 2(c).

To further confirm whether or not electron trapping was dominated by AHE injection, another $L = 80$ nm short channel device with an I_B peak was selected for investigation. First, it is necessary to determine what kinds of electron injection were most likely to contribute to the HCD. Figure 3(a) indicates the three most likely electron injection mechanisms making up HCD, which are CHE injection, AHE injection, and cold carrier injection.[26] CHE injection does not require as high an energy as I.I., but just sufficient to cause channel electron to become hot and inject to the high-k layer. AHE injection, in contrast, depends on I_B and should result in the severest V_{TH} degradation during I_B maximum HCD. Cold carrier injection occurs due to the electron trapping in pre-existing high-k bulk traps from the inversion layer of the channel by either Fowler-Nordheim or direct tunneling. Fig. 3(b) shows the I_B-V_G curves of the 80 nm short channel device when $V_D = 2.2$ V. In these devices, HCD conditions of $V_G = 1.6$ V ($I_{B,max}$), 1.8 V, and 2.0 V, with $V_D = 2.2$ V, could be selected to demonstrate whether or not electron trapping was dominated by AHE injection. Because if AHE injection dominates the V_{TH} degradation, $V_G = 1.6$ V has the maximum I.I. rate and should exhibit V_{TH}

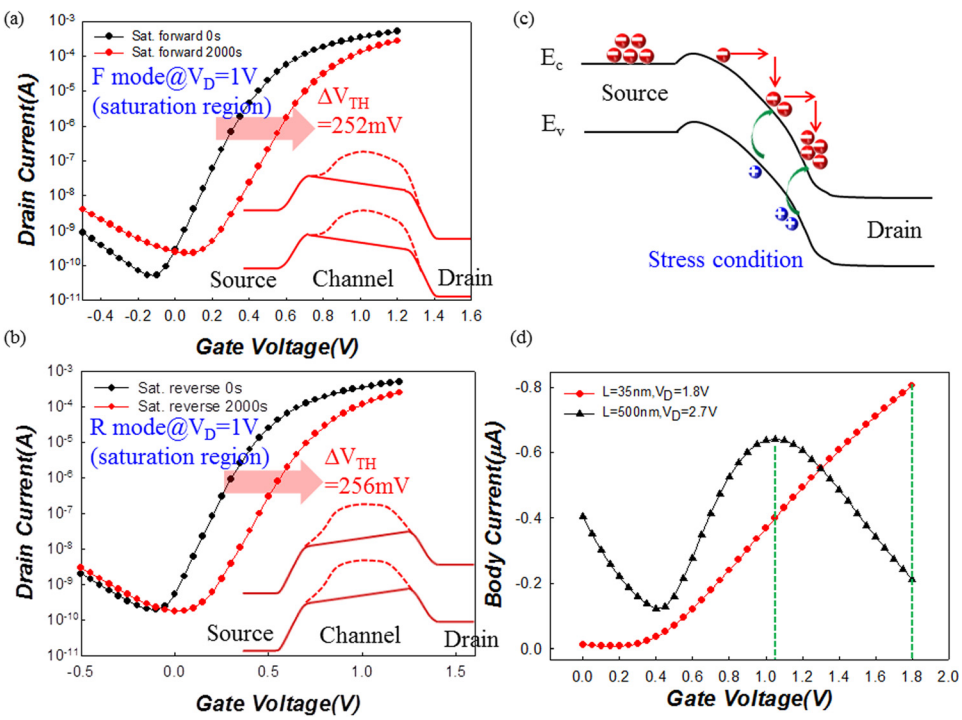

FIG. 2. (a) Forward and (b) reverse I_D-V_G at the saturation region measurement result for similar V_{TH} shifts in the short channel device. Insets show the similar barrier heights (dashed line) rising after hot electron trapping at the saturation region measurement. (c) The lateral energy band diagram of short channel HCD illustrating that stress V_D depletes part of the channel. (d) I_B-V_G measurement of $L = 500$ nm and 35 nm devices at each stress V_D.

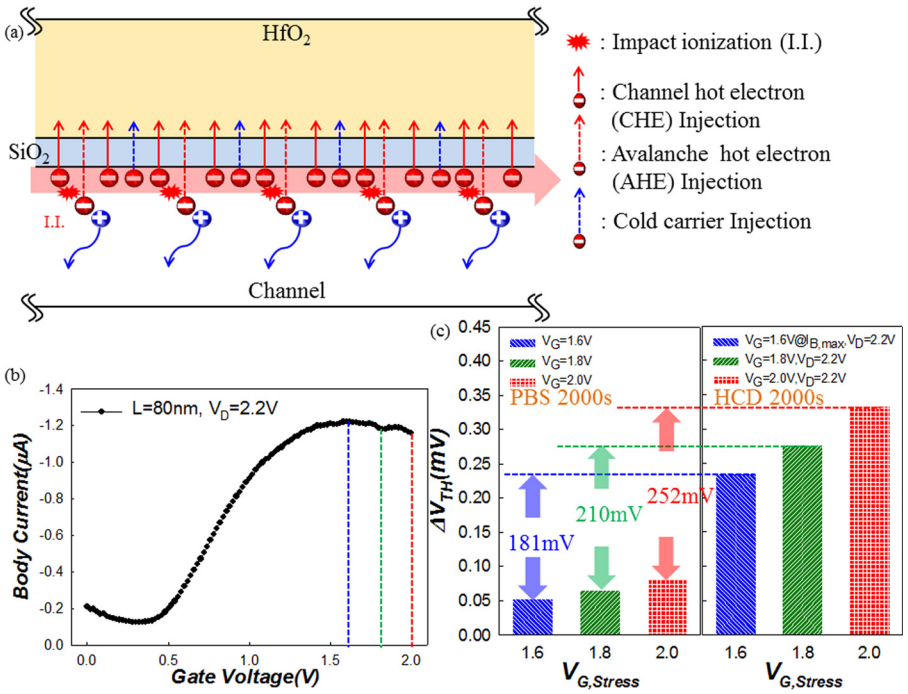

FIG. 3. (a) Diagram indicating that HCD is caused mainly by CHE, AHE, and cold carrier injection. (b) I_B-V_G curve of L = 80 nm device measured at stress $V_D = 2.2$ V. (c) V_{TH} shift compared for various V_G after HCD and PBS 2000 s.

degradation more severe than either 1.8 V or even 2.0 V. However, Fig. 3(c) shows the V_{TH} shift induced by HCD and PBS for various V_G. For HCD, the cold carriers associated with PBS have a simultaneous effect on the channel region due to pre-existing traps;[27,28] thus, the cold carrier injection should be eliminated by PBS for better clarification. After removing V_{TH} shift due to cold carrier injection, surprisingly the V_{TH} shift of $V_G = 2.0$ V was still more severe than $V_G = 1.6$ V, even though maximum I.I. occurs at $V_G = 1.6$ V, a trend contrary to AHE dominated degradation. Based on these V_{TH} shift experimental results, therefore, the hot electron trapping mechanism of HCD from impact ionization is injected into the high-k bulk defects should be modified. Obviously, the CHE also plays an important role in HCD with nanoscale channel devices. However, how the CHE could be trapped into high-k layer is also worth to know.

For the nanoscale channel devices, we think that the EES-induced CHE injection mechanism makes the significant contribution of hot electron trapping from the channel to the drain side at the high vertical field stress condition of $V_G = V_D$. Fig. 4(a) shows the interaction of EES-induced CHE; when two electrons collide, they scatter, with one becoming more energetic while the other becomes weaker. In general, many groups demonstrate that low energetic electrons can gain sufficient energy from EES to rupture Si-H bonds, leading to interface state generation at HCD, as shown in Fig. 4(b).[31,32] However, in high-k dielectric devices, we propose that the channel hot electrons become more energetic after EES interaction and not only rupture Si-H bonds but also overcome the barrier height of SiO_2 to trap in the high-k layer, shown in Fig. 4(c). Moreover, at larger V_G, a more significant V_{TH} shift after HCD exists, which is due to the higher carrier concentration inducing more EES,[31,33] in turn leading to more EES-induced CHE trapping in the high-k layer at larger stress V_G conditions.

To further confirm our assumption, Fig. 5 shows the correlation of the degradation of F and R modes $I_{D,sat}$ with V_{TH} shift measured at the saturation region during HCD with various stress V_G. The low stress V_G condition shows the largest difference between the F and R modes, corresponding to the lack of uniform degradations along the channel length.[32] All the F modes exhibit lower degradation of V_{TH} at the same $I_{D,sat}$ degradation level. This is because interface state generation is always concentrated near at the drain side; therefore, the

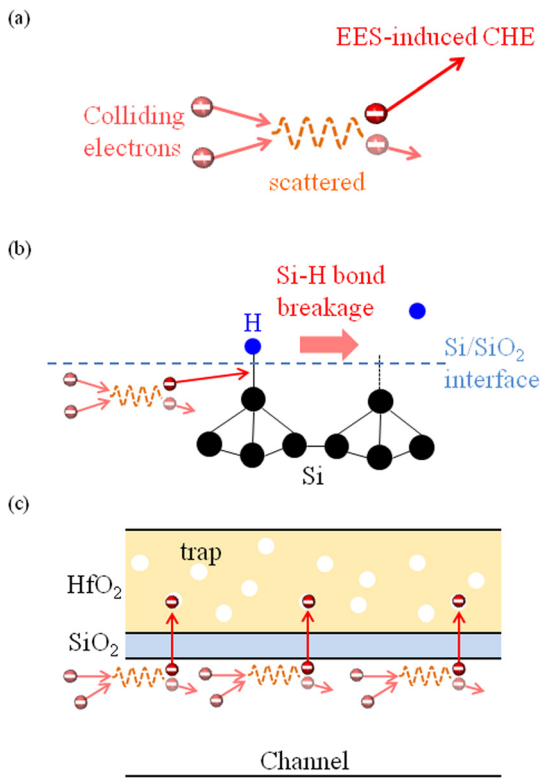

FIG. 4. (a) During the EES process, two electrons collide, one becoming more energetic while the other becomes weaker. (b) Si-H bond dissociation, leading to interface state generation. (c) The model of EES-induced CHE injection in the high-k bulk defects.

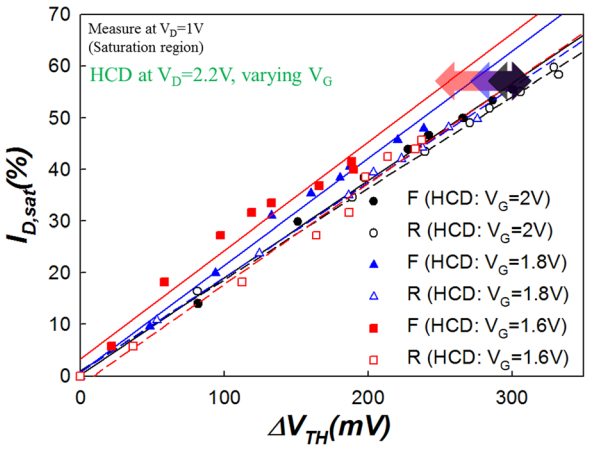

FIG. 5. The degradation of F (solid line) and R (dashed line) modes $I_{D,sat}$ with V_{TH} shift for different HCD conditions at various stress V_G.

measured V_D in F mode will deplete a portion of interface states in the channel, resulting in a lower degradation of V_{TH}. In the same way, the high stress V_G condition shows no significant difference between the F and R modes after HCD, meaning that it produces uniform degradations along the channel length. This is because the driving force is shift from energy-driven (electric field) to current-driven (carrier concentration)[34] HC damage. Besides, carrier concentration is a key factor to enhance EES rate in HCD for short channel devices. Thus, HC damage is not more only distributed at the drain side but also entire channel region, especially under high stress V_G. Therefore, EES-induced CHE injection is also simultaneously uniformly distributed at the high-k layer. This corresponds to our previous results shown in Figs. 2(a) and 2(b). Based on this observation, EES-induced CHE injection should not be ignored for HCD, especially in nanoscale devices.

This work investigates the EES-induced CHE injection in nanoscale n-MOSFETs with high-k/metal gate stacks. For short channel devices, although interface state generation also influences the HCD, hot electron trapping in the high-k bulk defects from the channel to the drain side dominate the HCD. Moreover, our detailed study shows that EES-induced CHE injection has a significant contribution to hot electron trapping at the high vertical field stress condition of $V_G = V_D$.

Part of this work was performed at United Microelectronics Corporation. The work was supported by the National Science Council under Contract No. NSC-103-2112-M-110-011-MY3.

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