Electrical-Stress Effects and Device Modeling of 0.18-μm RF MOSFETs

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***Abstract*—In this paper, a novel microstrip-line layout is used to make accurate measurements of the minimum noise figure ($\mathrm{NF_{min}}$) of RF MOSFETs. A low $\mathrm{NF_{min}}$ of 1.05 dB at 10 GHz was directly measured for 16-finger 0.18-μm MOSFETs, without de-embedding. Using an analytical expression for $\mathrm{NF_{min}}$, we have developed a self-consistent dc current–voltage, S-parameter, and $\mathrm{NF_{min}}$ model, where the simulated results match the measured device characteristics well, both before and after electrical stress.**

***Index Terms*—Lifetime, minimum noise figure ($\mathrm{NF_{min}}$), model, RF noise, stress.**

I. Introduction

SILICON RF MOSFETs [1]–[12] are now widely used for wireless communications, due to improvements of their RF noise and high-frequency gain performance as the technology has evolved. One of the key issues involves accurate determination of the RF performance degradation of the Si MOSFETs under continuous operation [1]–[5]. This is especially important for RF ICs compared with their digital and analog counterparts due to the tight requirements regarding impedance matching, low RF noise, and high gain. The use of ever-increasing communication frequencies, for instance from wireless LANs to ultrawideband (UWB) (3.1–10.6 GHz), makes this issue even more important, since the RF noise and gain both degrade with increasing frequency. A sound understanding of the RF performance degradation of MOSFETs is desirable. Another important issue is that the large parasitic effects from the high-RF-loss Si substrates play an important role for the as-measured $\mathrm{NF_{min}}$ [8]–[12]. De-embedding procedures for both "open" and "short" layouts are used to obtain the $\mathrm{NF_{min}}$ [13]. Here, we address these issues using a novel microstrip transmission-line layout. This permits accurate determination of the minimum noise figure ($\mathrm{NF_{min}}$) without requiring de-embedding. The success of this approach is evident from the very low as-measured $\mathrm{NF_{min}}$ of 1.05 dB at 10 GHz for our 16-finger 0.18-μm RF MOSFETs. We have developed a self-consistent dc current–voltage (*I–V*), S-parameters, and $\mathrm{NF_{min}}$ device produced and showed with the measured data. We subjected the devices to a hot-carrier stress of $V_{\mathrm{gs}} = 1/2V_{\mathrm{ds}} = 1.5$ V for 5000 s to obtain $\sim$ 20% degradation of the driving current (equivalent to 12.5 years lifetime at 1.8 V). The same device imitated and predicted the measured post-stress data well, provided that the drive current degradation was known. This approach can be used in circuit design as a tool for predicting the RF performance degradation under continuous operation.

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II. Experimental Procedure

In this paper, we used 0.18-μm RF MOSFETs that had multiple gate fingers (16 and 32 fingers) to reduce the thermal noise [8]–[12] generated from the gate resistance. The multiple-gate-finger 0.18-μm MOSFETs have 2.5-μm gate width, 4.0-nm gate oxide thickness, and 200-nm poly-Si thickness. A novel microstrip transmission-line layout was used, instead of a conventional coplanar waveguide (CPW) structure [8]–[12], to shield the substrate-resistance-generated noise of the RF probing pads. Thus, no complicated de-embedding procedures for the RF noise generated from the RF pads and the "through" CPW lines were required. We used this accurate measurement method to monitor degradation of the RF performance with electrical stress. The fabricated devices were stressed electrically at $V_{\mathrm{gs}} = 1/2V_{\mathrm{ds}} = 1.5$ V for 5000 s. The devices were characterized by dc *I–V*, S-parameters, and $\mathrm{NF_{min}}$ measurements, before and after stress, using an HP4155C, an HP8510C network analyzer, and an ATN-NP5B noise-parameter measurement system, respectively. From the measured data, we developed a self-consistent model, with a Berkeley short-channel IGFET model (BSIM) core, to simulate the device characteristics before and after stress [8]–[12].

III. Results and Discussion

A. DC Characteristics

The dc characteristics (I_d–V_d and I_d–V_g) for 16- and 32-finger 0.18-μm RF MOSFETs are compared in Fig. 1(a) and (b), before and after hot-carrier stress. The saturation drain current ($I_{d,\mathrm{sat}}$) decreases with stress time to a 20% degradation. The I_d degradation is also evident in the I_d–V_g curves, where additional threshold voltage (V_t) and subthreshold slope (SS) degradations occur with stress. After hot-carrier stress, V_t increases from 0.475 to 0.675 V and the SS shifts from 85 to 110 mV/decade. These degradations are due to electron

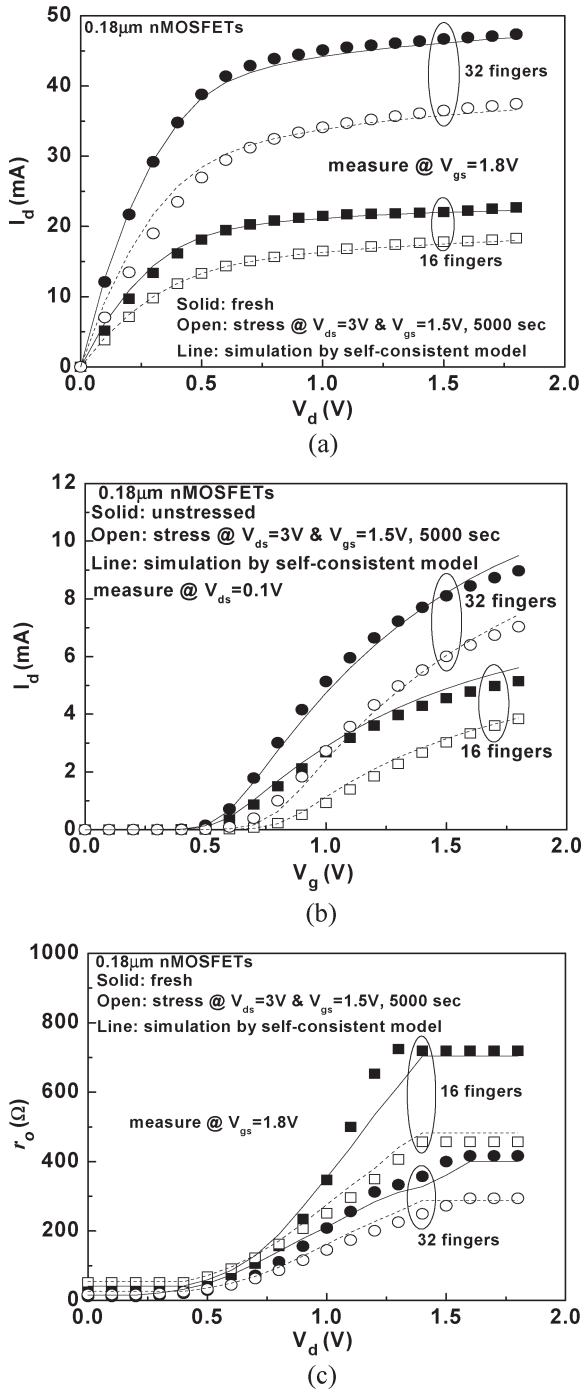

Fig. 1. Measured and modeled dc (a) $I_d - V_d$ and (b) $I_d - V_g$, and (c) $r_o - V_d$ characteristics of 16- and 32-finger RF MOSFETs before (solid symbols) and after (open symbols) hot-carrier stress. The line represents the simulation using a self-consistent device model.

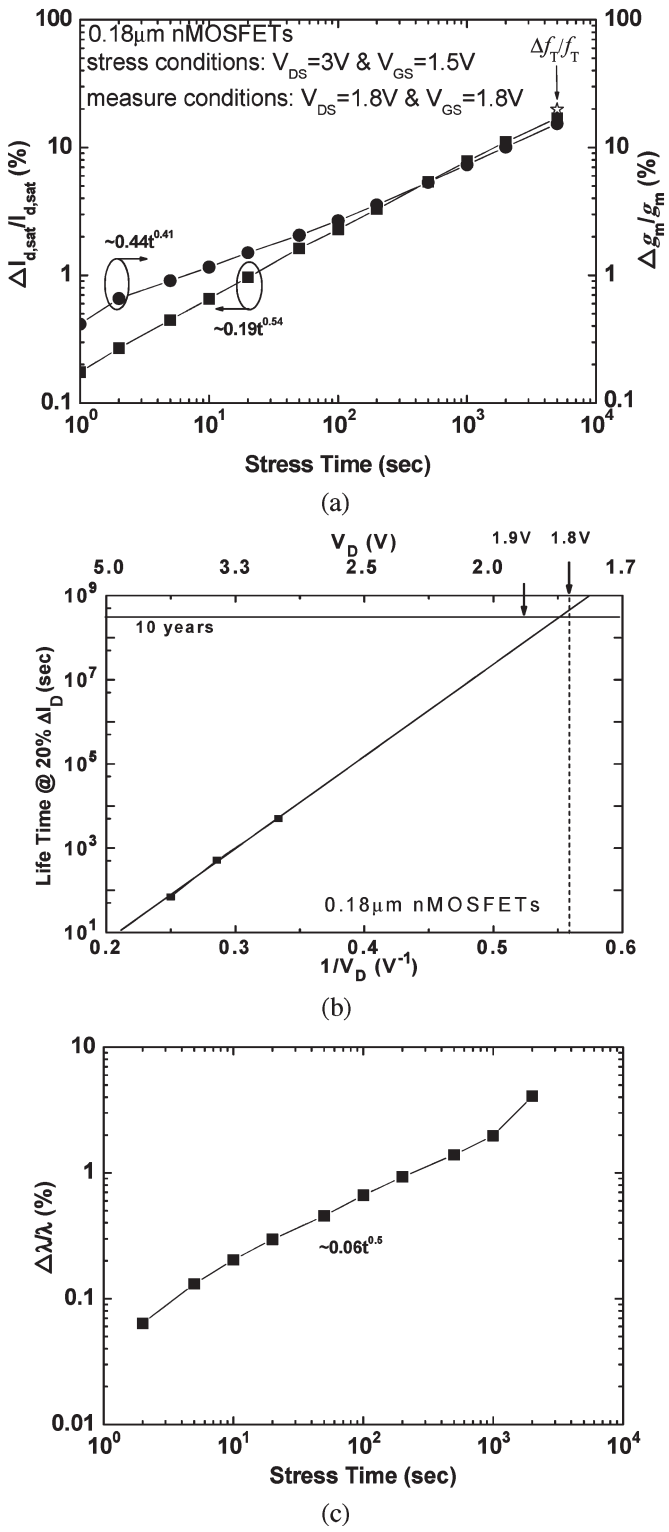

Fig. 2. (a) Time dependence of $I_{d,\mathrm{sat}}$ and g_m degradation for 0.18-μm RF MOSFETs. (b) The lifetime at 20% $\Delta I_{d,\mathrm{sat}}/I_{d,\mathrm{sat}}$ for 0.18-μm RF MOSFETs. The stress conditions were equivalent to 12.5 years of continuous operation at 1.8 V or a 2.7-year lifetime at 1.9 V overdrive. (c) Time-dependent degradation of the drain-current noise correlation factor λ.

trapping and oxide-Si interface state generation on the drain side of the devices, which result in the higher V_t and lower electron mobility in the channel, respectively [14]–[16]. In addition, the output resistance r_o $(= 1/\partial I_d/\partial V_{\mathrm{ds}})$, shown in Fig. 1(c), also decreases after stress, which is important for the RF gain and matching in a circuit.

Fig. 2(a) illustrates the time dependence of the $\Delta I_{d,\mathrm{sat}}/I_{d,\mathrm{sat}}$ degradation for 0.18-μm RF MOSFETs, under the worst hot-carrier stress conditions of $V_{\mathrm{gs}} = 1/2V_{\mathrm{ds}} = 1.5$ V. The $I_{d,\mathrm{sat}}$ degrades monotonically with increasing stress time, which is typical for hot-carrier stress. Fig. 2(b) displays the lifetime for a 20% $I_{d,\mathrm{sat}}$ reduction in the devices, under different stress voltage conditions. The extrapolated lifetime follows an

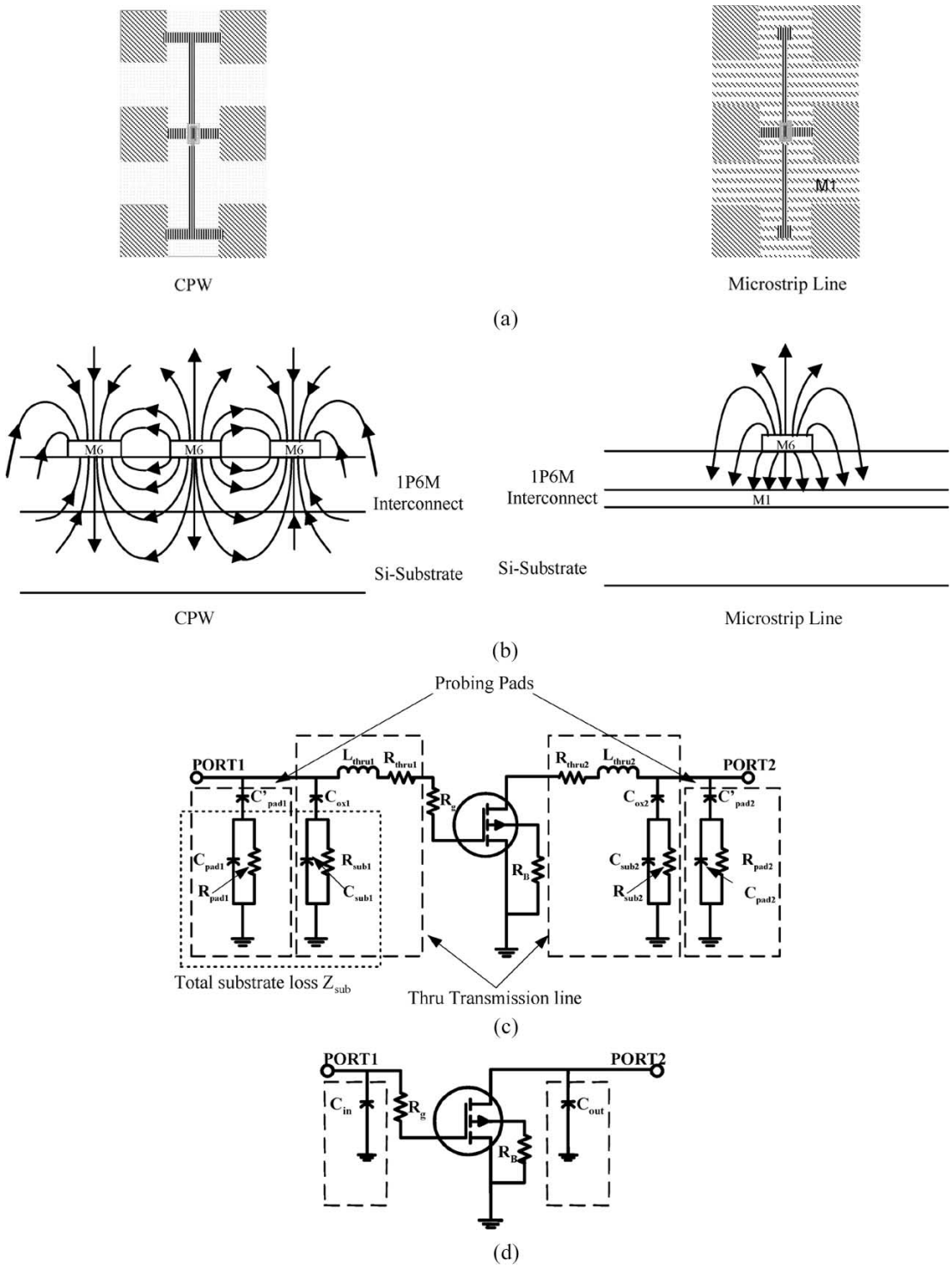

Fig. 3. (a) Layout for conventional CPW and novel microstrip lines of low-noise 0.18-μm MOSFETs. For the microstrip-line design, M1 and M6 are used to form the transmission line and the $R_{\rm pad}$- and $R_{\rm sub}$-generated noises are screened by M1. (b) Cross-sectional view of different CPW and novel microstrip lines. (c) Equivalent circuit model for RF MOSFETs using CPW transmission lines. (d) Equivalent circuit model for RF MOSFETs using microstrip transmission lines.

exponential dependence on $1/V_d$ [5], and thus our stress conditions mimic continuous operation at 1.8 V for 12.5 years, or at 1.9 V overdrive for 2.7 years. Fig. 2(c) shows the channel-length modulation coefficient λ as a function of stress time. This was obtained from the r_o and I_d using $\lambda = 1/r_{\rm o}I_d$. The linear variation of λ with the stress time is important for modeling the $I_d{-}V_d$ after stress.

B. Novel Microstrip Transmission-Line Layout and $\rm NF_{min}$ *Reduction*

As mentioned above, the RF noise is difficult to measure in Si MOSFETs due to the large noise generated from the parasitic substrate loss [8]–[12], [17], [18]. Fig. 3(a) shows the layout of conventional CPW and microstrip lines. In the conventional CPW layout, the electromagnetic (EM) waves can penetrate

deeply into the low-resistivity Si substrate [shown in Fig. 3(b)] to cause the loss, and increasing $\mathrm{NF_{min}}$. Fig. 3(c) shows the equivalent circuit model for RF MOSFETs using a conventional CPW transmission-line layout, where accurate modeling of the as-measured $\mathrm{NF_{min}}$ was previously obtained by considering the thermal noise generated from the pad (R_{pad}) and transmission lines (R_{sub}) [9]. The RF noise from R_{pad} and R_{sub} dominate the as-measured $\mathrm{NF_{min}}$ rather than from the intrinsic noise of an MOSFET. Therefore, de-embedding is required to give the smaller intrinsic $\mathrm{NF_{min}}$ [9]. However, the procedures for de-embedding open RF pads and through transmission lines, which occupy additional layout area, are complicated and can produce errors. To overcome these problems, we propose a microstrip-line layout, also shown in Fig. 3(a). In sharp contrast, the microstrip layout can confine the EM waves within the low-loss backend dielectric [19], as also shown in Fig. 3(b). Thus, the Metal-1 (M1) is used as a shield to prevent EM waves penetrating the high-loss and noisy Si substrate. Because the M1 is used as the ground plane of the microstrip transmission line, above the lossy Si substrate, the R_{pad}- and R_{sub}-generated noise can be screened out, and thus do not contribute to the as-measured $\mathrm{NF_{min}}$. This is the strong merit of using the new microstrip layout without the complicated $\mathrm{NF_{min}}$ de-embedding procedure used in the conventional CPW layout.

To demonstrate this approach, in Fig. 4(a) and (b), we show the as-measured $\mathrm{NF_{min}}$ for the 16- and 32-finger 0.18-μm RF MOSFETs, respectively, where both the data from standard CPW and microstrip transmission-line layouts are shown for comparison. A large $\mathrm{NF_{min}}$ reduction of 0.5–2.5 dB was obtained using the microstrip transmission-line design, as the frequency was increased from 1 to 18 GHz, even without de-embedding. At 10 GHz, the as-measured $\mathrm{NF_{min}}$ was reduced to 1.05 and 1.12 dB for the 16- and 32-finger 0.18-μm MOSFETs, respectively. This as-measured low $\mathrm{NF_{min}}$ is close to the de-embedded value of standard CPW layout [9] (also shown in Fig. 4), which indicates that the microstrip transmission-line design can successfully shield the thermal noise from the lossy R_{pad} and R_{sub} and yield accurate $\mathrm{NF_{min}}$ values. This indicates the good accuracy of directly measured $\mathrm{NF_{min}}$ by using microstrip-line layout without de-embedding or possible causing errors, which also confirmed the successful shielding of EM waves from the lossy Si substrate shown in Fig. 3(b). This is the lowest reported $\mathrm{NF_{min}}$ for a 0.18-μm MOSFET and is comparable with the data for 0.13-μm devices $(L_g = 80\ \mathrm{nm})$ [9]–[11]. The low $\mathrm{NF_{min}}$ of 1.05 dB at 10 GHz is sufficient for UWB (3.1–10.6 GHz) applications.

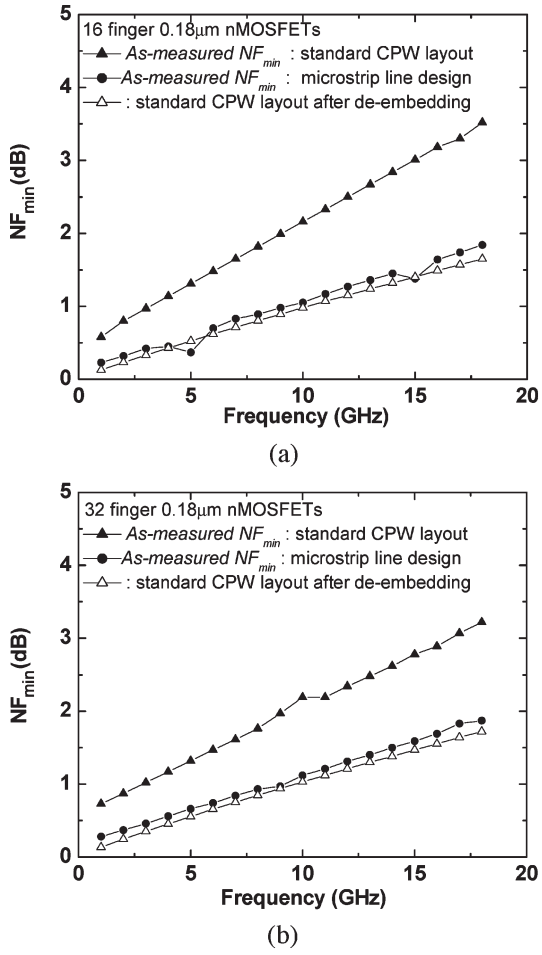

Fig. 4. Comparison of the as-measured $\mathrm{NF_{min}}$ data of a standard CPW layout and a microstrip transmission-line design for (a) 16- and (b) 32-finger 0.18-μm RF MOSFETs.

C. RF Performance

Fig. 5(a) and (b) shows the measured S-parameters of the 16- and 32-finger 0.18-μm RF MOSFETs, respectively, for both fresh and stressed devices. The hot-carrier stress has little effect on S_{11} and S_{12}, which is due to the unchanged input capacitance (C_{gs}) and only slightly altered feedback capacitance (C_{gd}) after stress. In contrast, significant change occurred for S_{21} and S_{22} for both multifingered devices. The degraded S_{21} after stress is due to the reduced forward gain and is related to the lower transconductance (g_m). The degraded S_{22}, as shown in the horizontal left shift in the Smith chart, comes from a decrease of r_o, as shown in the dc $I_d{-}V_d$ characteristics of Fig. 1(a). This will result in poor output impedance matching in a circuit.

The effects of stress on the frequency dependence of the RF current gain $|H_{21}|^2$ and the $G_{\max}$ at the maximum stable gain (MSG) region, for a 16-finger device, are shown in Fig. 6(a). The $|H_{21}|^2$ follows the typical -20-dB/dec slope and $G_{\max}$ at MSG follows a -10-dB/dec slope [20]. The $G_{\max}$ is used here since the unilateral gain (U) gives unrealistic higher gain than $G_{\max}$ [20]. The stress lowers the cutoff frequency (f_t) from 48.3 to 38.7 GHz. This amounts to a 19.8% degradation of f_t, similar to the dc drive current reduction. Fig. 6(b) displays the $f_t{-}V_g$ and $g_m{-}V_g$ dependences for the 16-finger 0.18-μm RF MOSFETs, before and after stress. Note that the f_t curve follows the g_m curve with respect to V_g, and the stress not only lowers the f_t and g_m but also shifts both curves by the amount of ΔV_t. Although in an RF circuit, it is desirable to use a low V_g bias to reduce the dc power dissipation, the shift of the f_t curve after stress should be considered and the MOSFETs should rather be biased in the saturation region with a larger V_t. For 0.18-μm RF MOSFETs, a higher V_g bias of 1.2 V is suggested, rather than 1.0 V, when one considers the stress effects.

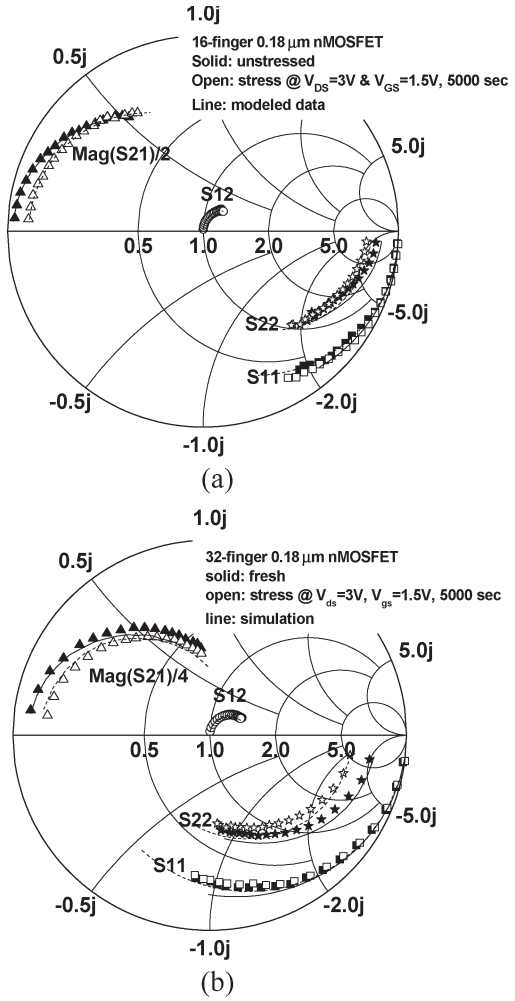

Fig. 5. Measured and modeled S-parameters for (a) 16- and (b) 32-finger 0.18-μm RF MOSFETs before (solid symbols) and after (open symbols) hot-carrier stress. The lines represent the simulated data.

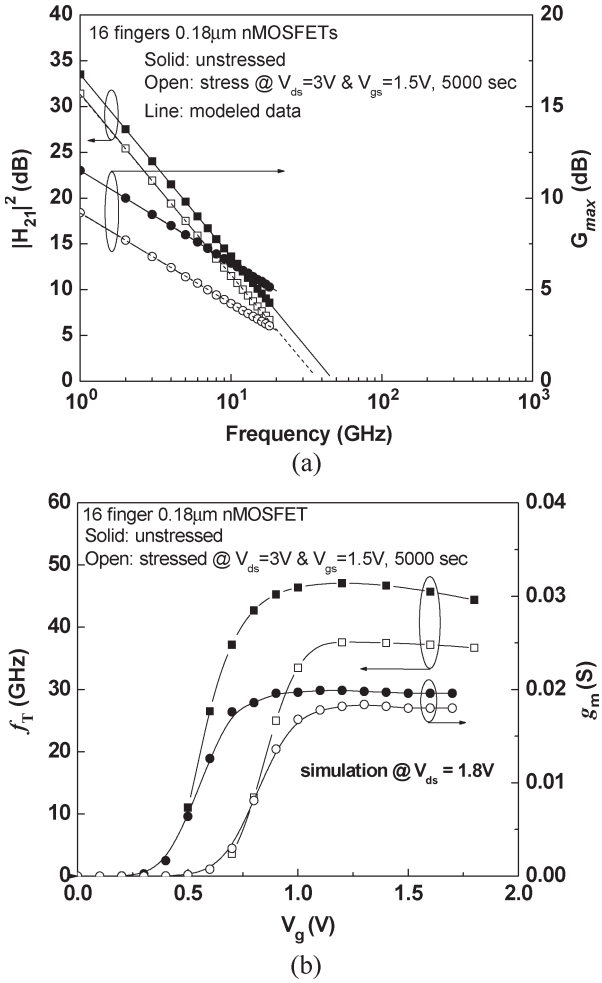

Fig. 6. (a) Measured and simulated $|H_{21}|^2$ and $G_{\max}$ versus frequency. (b) The f_t versus V_g for 16-finger 0.18-μm RF MOSFETs, before (solid symbols) and after (open symbols) hot-carrier stress.

Fig. 7(a) and (b) shows the measured $\mathrm{NF}_{\min}$ of the 16- and 32-finger devices employing the microstrip transmission-line design. At 10 GHz, the $\mathrm{NF}_{\min}$ was 1.05 and 1.12 dB for the 16- and 32-finger devices, respectively. The $\mathrm{NF}_{\min}$ after hot-carrier stress increased over the whole measured frequency range. At 10 GHz, $\mathrm{NF}_{\min}$ increased from 1.05 to 1.37 dB for the 16-finger devices and from 1.12 to 1.46 dB for the 32-finger devices. Such $\mathrm{NF}_{\min}$ increase should also be considered in RF-circuit design.

D. Device Modeling Before and After Stress

Since the hot-carrier stress has significant effects on both dc and RF performance, accurate modeling of the device performance after stress is needed. We first established the device model for unstressed devices. The circuit model is shown in Fig. 3(d), where a BSIM core (level 3.2) is used with only added parasitic gate resistance (R_g), substrate resistance (R_b), input (C_{in}), and output (C_{out}) shunt capacitances; these are summarized in Table I. Note that the BSIM model can simulate the dc characteristics of CMOS devices well, but it is still challenging to model the RF performance, especially the $\mathrm{NF}_{\min}$. This is because of the large parasitic effects from the high-RF-loss Si substrate. Although using open pad and through transmission-line layout followed by a complicated de-embedding procedure can develop the self-consistent transistor model of dc, S-parameters, and $\mathrm{NF}_{\min}$ [9], it is highly desirable to develop a simple method to directly measure the RF performance such as $\mathrm{NF}_{\min}$ without additional layout and de-embedding. The device model shown in Fig. 3(d) is simpler than the one used for the CPW case shown in Fig. 3(c), since the substrate RF losses from the pads and transmission lines are successfully shielded.

The simulated dc $I_d{-}V_d$, $I_d{-}V_g$, and $r_o{-}V_d$ curves are included in Fig. 1(a)–(c), respectively. The modeled RF S-parameters, $|H_{21}|^2$, $G_{\max}$, and $f_t{-}V_g$ are shown in Figs. 5 and 6, respectively. Good agreement between the measured and modeled dc *I–V*, RF S-parameters, $|H_{21}|^2$, $G_{\max}$, and f_t were all obtained self-consistently using the simple equivalent circuit model incorporating the microstrip-line design.

To get an accurate model for $\mathrm{NF}_{\min}$, we have used an analytical equation previously derived from the equivalent noise circuit of MOSFETs [8], [9]

$$\mathrm{NF}_{\min} = 1 + 2\gamma\left(1 + \frac{g_m R_g}{\gamma}\right)^{\frac{1}{2}} \frac{f}{f_t}. \tag{1}$$

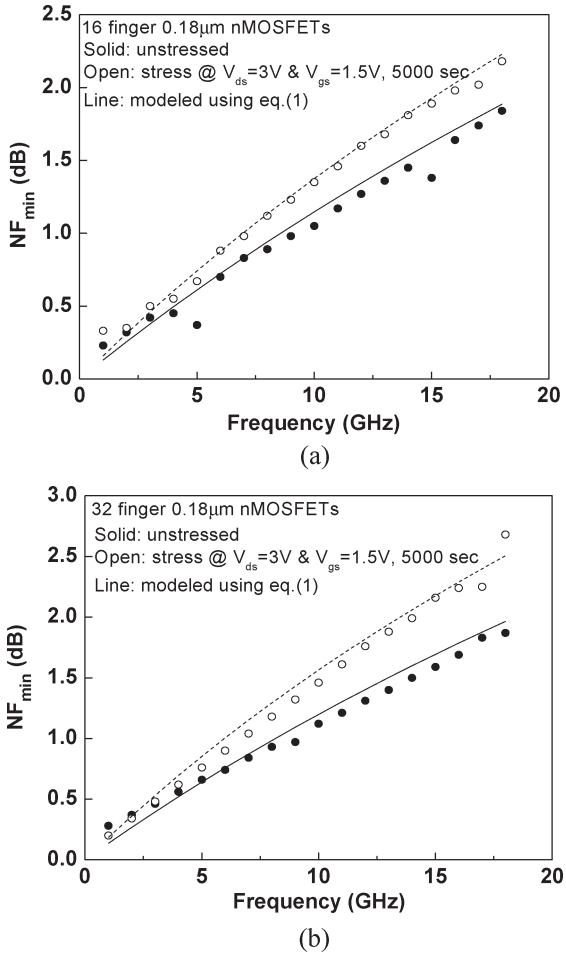

Fig. 7. Measured and modeled $\mathrm{NF_{min}}$ of (a) 16- and (b) 32-finger 0.18-μm MOSFETs before and after hot-carrier stress.

TABLE I
DEVICE PARAMETERS USED FOR MULTIFINGERED 0.18-μm RF MOSFETs

MOSFETs	$\mathrm{R_g}$ (Ω)	$\mathrm{R_b}$ (Ω)	$\mathrm{C_{gs}}$ (F/m)	$\mathrm{C_{gd}}$ (F/m)
16 fingers	6.6	128.4	1.1×10^{-9}	5.9×10^{-10}
32 fingers	3.4	69.7	1.1×10^{-9}	5.9×10^{-10}

Here, γ is the drain–current noise correlation factor, which has an ideal value of 2/3 [21], [22]. Close agreement between measured and simulated $\mathrm{NF_{min}}$ is shown in Fig. 7, in addition to the good agreement for the dc *I–V*, *S*-parameters, and RF gain, as shown above. The device parameters for the $\mathrm{NF_{min}}$ simulation, for both unstressed devices, are summarized in Table II, where the γ values used in the simulation were 0.67 and 0.7 for the 16-and 32-finger devices, respectively. These values are close to the ideal value of 2/3.

After achieving good agreement for the dc and RF characteristics of fresh 0.18-μm MOSFETs, we have simulated the device characteristics after stress. Using the criteria of 20% $I_{d,\mathrm{sat}}$ degradation, as shown in Fig. 2 after continuous operation, we first obtained good agreement of the simulated dc $I_d{-}V_d$, $I_d{-}V_g$, and $r_o{-}V_d$ with measurements shown in Fig. 1. Without changing the values of the parasitic R_g, R_b, C_{in}, and C_{out} in the equivalent circuit model, good agreement was obtained between the simulated RF *S*-parameters, $|H_{21}|^2$, $G_{\max}$, and $\mathrm{NF_{min}}$ and the measured data (see Figs. 5–7). The drain-current noise correlation factor γ was kept constant before or after hot-carrier stress for the same multifinger devices. The $g_m R_g$ term in (1) only plays a minor role for $\mathrm{NF_{min}}$, since by using parallel fingers, the R_g and $g_m R_g/\gamma$ are reduced. Therefore, the $\mathrm{NF_{min}}$ degradation appears to be dominated by the cutoff frequency f_t.

TABLE II
DEVICE PARAMETERS USED IN THE $\mathrm{NF_{min}}$ SIMULATION FOR 16- AND 32-FINGER 0.18-μm MOSFETs, BEFORE AND AFTER HOT-CARRIER STRESS

Device parameters	before stress		after 5,000 sec stress	
	16 finger	32 finger	16 finger	32 finger
f_T(GHz)	48.3	48.0	38.7	37.2
γ	0.67	0.7	0.67	0.7
g_m(S)	0.02	0.039	0.017	0.034
$\mathrm{R_g}$ (Ω)	6.55	3.45	6.55	3.45
g_m*$\mathrm{R_g}$/γ	0.196	0.192	0.167	0.168

The good agreement between simulated and measured data, before and after stress, indicates that the self-consistent model, for the microstrip transmission-line layout design, can be useful in predicting the RF MOSFETs degradation under continuous operation, as long as the degree of I_{ds} degradation is known from the stress data.

IV. CONCLUSION

We have successfully developed a model to predict device dc *I–V*, *S*-parameters, and $\mathrm{NF_{min}}$ by using a microstrip transmission-line-layout design. Close agreement was obtained for the accurate $\mathrm{NF_{min}}$ measurements and the analytical $\mathrm{NF_{min}}$ simulation. This approach is important as a tool in predicting the RF performance degradation of MOSFETs in a circuit where the devices are under continuous bias operation.

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