Novel Two-Bit HfO_2 Nanocrystal Nonvolatile Flash Memory

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***Abstract*—This paper presents a novel nonvolatile poly-Si-oxide–nitride–oxide–silicon-type Flash memory that was fabricated using hafnium oxide (HfO_2) nanocrystals as the trapping storage layer. The formation of HfO_2 nanocrystals was confirmed using a number of physical analytical techniques, including energy-dispersive spectroscopy and X-ray photoelectron spectroscopy. These newly developed HfO_2 nanocrystal memory cells exhibit very little lateral or vertical stored charge migration after 10 k program/erase (P/E) cycles. According to the temperature-activated Arrhenius model, we estimate that the activation energy lies within the range 2.1–3.3 eV. These HfO_2 nanocrystal memories exhibit excellent data retention, endurance, and good reliability, even for the cells subjected to 10 k P/E cycles. These features suggest that such cells are very useful for high-density two-bit nonvolatile Flash memory applications.**

***Index Terms*—Flash memory, hafnium oxide (HfO_2), nanocrystals, nonvolatile memories.**

I. Introduction

POLY-Si-OXIDE–NITRIDE–OXIDE–SILICON (SONOS)-type structure memories, which include nitride and nanocrystal memories, have recently attracted much attention for their application in the next-generation nonvolatile memories [1]–[10]. They exhibit many advantages, e.g., easy to fabricate, high program/erase (P/E) speed, low programming voltage and power consumption, and better potential for scalability below the 70-nm node, according to the International Technology Roadmap for Semiconductors (ITRS) [11]. Unfortunately, many concerns still remain for this type of memories. For conventional SONOS memory, erase saturation and vertical stored charge migration [7], [8] are two major drawbacks, whereas for nanocrystal memories, the most challenging tasks are how to maintain acceptable charge capability of the discrete storage nodes and fabricate nanocrystals with constant size, high density, and uniform distributions [9]. In recent years, various ONO processing technology [10] and alternative trapping layer material [12] have been investigated to improve the cell data retention. For example, the use of an Al_2O_3 trapping layer and $HfAlO_3$ to replace Si_3N_4 has been considered because their material bandgaps and high trap densities provide superior P/E speed and data retention [12], [13]. Moreover, various kinds of nanocrystals, such as silicon (Si), germanium (Ge), and metal nanocrystals, may be used to provide charge storage for nonvolatile memories [1]–[6].

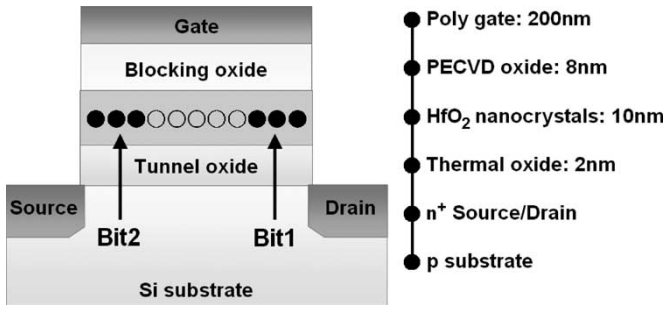

Fig. 1. Schematic representation of the HfO_2 nanocrystal Flash memory cell structure and localized charge storage.

In this paper, we propose a novel technique that is fully compatible with the current CMOS technologies in forming very localized HfO_2 nanocrystals for application in high-density two-bit nonvolatile Flash memory. This approach utilizes spinodal decomposition of hafnium silicate after rapid thermal annealing (RTA) treatment at a sufficiently high temperature [14], [15]. Using this technique, we can readily isolate the HfO_2 nanocrystals from each other within an SiO_2-rich matrix. With a large bandgap offset between HfO_2 and SiO_2, memory cell using HfO_2 nanocrystal may exhibit superior characteristics, such as a larger memory window, high P/E speeds, long retention time, excellent endurance [16], [17], and strong immunity against disturbance. In addition, by comparing to those published ones using Si, Ge, and metal nanocrystals [1]–[6], our HfO_2 nanocrystal memory possesses many advantages, such as larger memory window and better data retention. Moreover, high-temperature process for the source/drain (S/D) activation is no longer detrimental because this step can help further stabilize the HfO_2 nanocrystal; however, it will oxidize the other nanocrystals and lead to a decrease in memory window. The process is very simple, reproducible, and reliable, with less metal contamination concern.

II. Device Fabrication

An example of the fabrication process of the HfO_2 nanocrystal memory devices is demonstrated by a local oxidation of silicon (LOCOS) isolation process on a p-type, 5- to 10-$\Omega \cdot$ cm, (100) 150-mm silicon substrate (Fig. 1). First, a 2-nm tunnel oxide was thermally grown at 1000 °C in a vertical furnace

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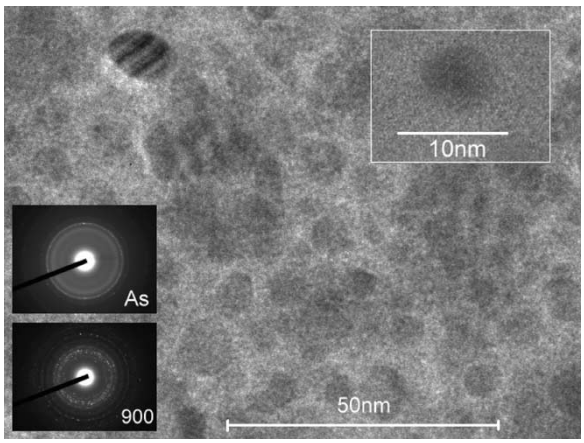


Fig. 2. Planar-view HRTEM image of the HfO_2 nanocrystals. The cell size is 5–8 nm, and the dot density is $0.9-1.9 \times 10^{12}$ cm^{-2}. The inset shows the diffraction patterns of the as-deposited and 900 °C RTA-treated samples.

system. Next, a 12-nm amorphous $HfSiO_x$ silicate layer was deposited by cosputtering with pure silicon (99.9999% pure) and pure hafnium (99.9% pure) targets in an oxygen gas ambient. The cosputtering process was performed with 7.6×10^{-3} Torr at room temperature (RT) and with precursors of O_2 [3 standard cubic centimeters per minute (sccm)] and Ar (24 sccm); in which both direct current (dc) sputter powers were set at 150 W. The samples were then subjected to RTA treatment in an O_2 ambient at 900 °C for 1 min to convert the $HfSiO_x$ silicate film into the separated HfO_2 and SiO_2 phases. Their compositions were identified using both energy-dispersive spectroscopy (EDS) and X-ray photoelectron spectroscopy (XPS). An 8-nm blocking oxide was then deposited through high-density plasma chemical vapor deposition (HDPCVD), followed by an N_2 densification process at 900 °C for 1 min. Subsequently, poly-Si deposition, gate patterning, S/D implanting, and the remaining standard CMOS procedures were completed to fabricate the HfO_2 nanocrystal memory devices.

Fig. 2 shows planar-view high-resolution transmission microscopy (HRTEM) image of the HfO_2 nanocrystals. The average nanocrystal size was 5–8 nm; the density was as high as $0.9-1.9 \times 10^{12}$ cm^{-2}. Clearly, the nanocrystals were well separated in two dimensions within the SiO_2, in which the average distance is > 5 nm. This isolation of the nanocrystals prevents the formation of effective conductive paths between adjacent nodes. The mechanism responsible for the formation of HfO_2 nanocrystal is through the phase separation of hafnium silicate into a crystallized structure [14]. For the Hf-silicate layer, the compositions within metastable extensions of the spinodal are unstable, and HfO_2 nanocrystal will be formed and wrapped up by SiO_2 after cooling down from RTA processing. In addition, it is clear from the diffraction patterns that the as-deposited film was amorphous and that the sample subjected to RTA was polycrystalline. The HfO_2 nanocrystals have monoclinic crystalline structures. Table I lists the original average concentrations of the individual elements in the as-deposited amorphous $HfSiO_x$ silicate layer, as determined through EDS analysis at a spatial resolution less than 2.0 nm. We observe that the as-deposited $HfSiO_x$ layer comprised ca. 40 mol% HfO_2 and 60 mol% SiO_2; the average elemental concentrations of Hf, Si, and O were 12.61%, 18.99%, and 68.40%, respectively. At this elemental composition, we can readily reproduce high-density HfO_2 nanocrystal dots embodied within an SiO_2-rich matrix after RTA in an O_2 ambient.

TABLE I
AVERAGE ELEMENTAL COMPOSITIONS IN THE $HfSiO_x$ SILICATE LAYERS, AS EXAMINED THROUGH EDS ANALYSIS OF THE AS-DEPOSITED AND 900 °C RTA-TREATED SAMPLES

	Hf (%)	Si (%)	O (%)
Asdep	12.6	19	68.4
900°C inside	24.62	22.74	52.64
900°C outside	2.84	39.65	57.51

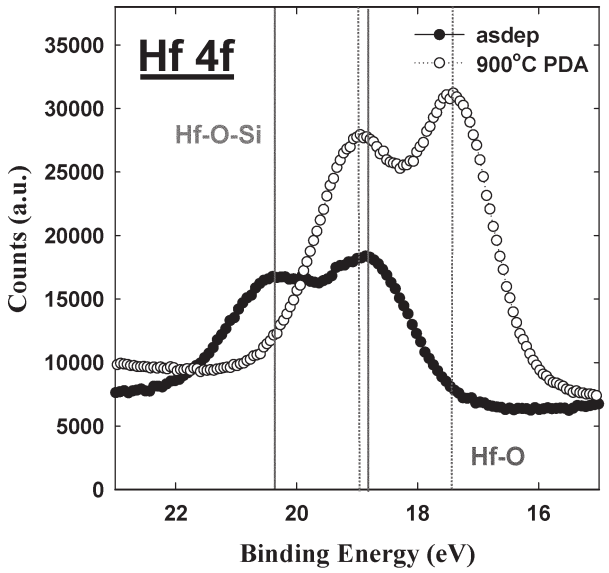
We have also performed XPS measurements using an Al Kα X-ray source (1486.6-eV photons) to determine the bonding environments of the Hf and Si atoms. Fig. 3(a) shows the Hf 4f photoemission peaks of the as-deposited Hf-silicate film before and after its postdeposition annealing (PDA) at 900 °C under O_2. In the as-deposited film, we observe well-defined $4f_{5/2}$ and $4f_{7/2}$ feature peaks that correspond to Hf–O–Si bonding. We confirmed that HfO_2 nanocrystals formed after RTA through the observed shifts of these peaks to lower binding energies ($4f_{5/2}$: ca. 18.9 eV; $4f_{7/2}$: ca. 17.4 eV) [18], [19]. Fig. 3(b) shows Si 2p XPS spectra of the as-deposited Hf-silicate film before and after RTA. Again, the Si–O bonds in SiO_2 network (104 eV) are prominent; their peak intensity increased after PDA. These results provide definite evidence for phase separation occurring in the PDA-treated Hf-silicate film.

For the cell operation, channel hot-electron injection and band-to-band hot-hole injection for the programming and erasing, respectively, have been used. All cells described in this paper have dimensions of length/width $(L/W) = 1/2$ μm. Fig. 4 demonstrates the feasibility of performing two-bit operation with our HfO_2 nanocrystal memories through a reverse-read scheme in a single cell. From the $I_{ds}-V_{gs}$ curves, it is clear that we could employ forward and reverse reads to detect the information stored in the programmed bit1 and bit2, respectively. The read operation was achieved using a reverse-read scheme. Table II summarizes the bias conditions for two-bit operation.

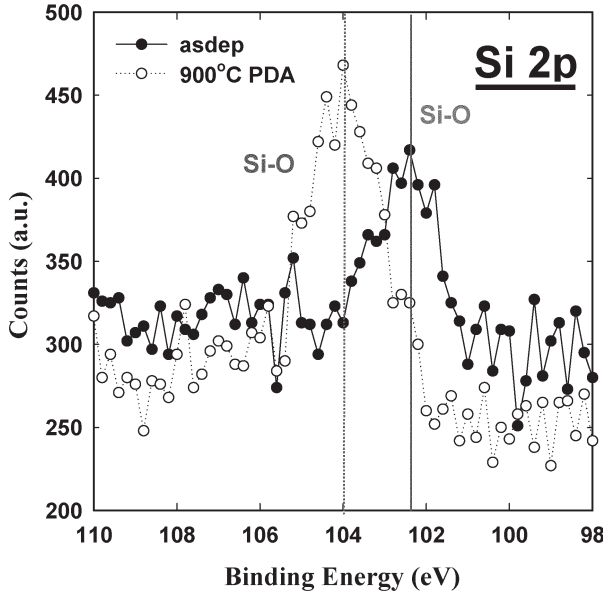
III. RESULTS AND DISCUSSION

A. Migration of Storage Charges

One of the major advantages that HfO_2 nanocrystal Flash memory has over floating-gate flash erasable programmable read-only memory (EEPROM) is its better data retention, which is attributed to its excellent capability of locally trapping charges with no significant lateral or vertical migration. We can measure the degrees of migration from the cells after the cycling. One method for characterizing the lateral extent of the trapped electrons is to monitor the variation of the threshold voltage V_t for a programmed memory cell in the presence of a changing drain current V_d [19]. Fig. 5 shows a plot of the measured V_t versus V_d as a function of the measuring



(a)



(b)

Fig. 3. XPS spectra of the as-deposited and 900 °C RTA-treated samples. (a) Hf 4f. (b) Si 2p. These spectra indicate that the Hf-silicate was fully converted to HfO_2 and SiO_2 through phase separation after PDA at 900 °C under O_2.

temperature in a programmed cell after 10 k P/E cycling. Here, V_t is defined as the applied gate voltage at which the drain current is 1 μA. Inasmuch as channel hot-electron injection is used for the cell programming, the trapped electrons in the HfO_2 nanocrystal trapping layer are more likely to be located near the n^+ drain junction. These trapped electrons will raise the potential barrier near the drain side and increase the value of V_t. The degree of the V_t shift is believed to be proportional to the trapped electron density if the drain terminal is maintained at a relatively low potential (e.g., $V_d = 0.1$ V). When a sufficiently high drain bias (e.g., $V_d = 1.5$ V) is applied, however, the drain depletion region will be extended toward the channel and, consequently, block the influence from the trapped electrons for the measured $I_d - V_g$ characteristics [20].

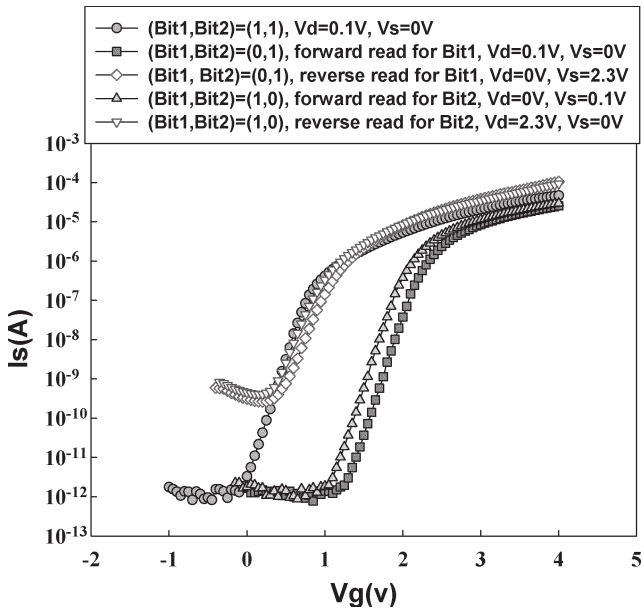


Fig. 4. $I_{ds} - V_{gs}$ curves of the two-bit memory in a cell; forward read and reverse read for programmed bit1 and programmed bit2.

TABLE II
OPERATION PRINCIPLES AND BIAS CONDITIONS UTILIZED DURING THE OPERATION OF THE HfO_2 NANOCRYSTAL FLASH MEMORY CELL

		Program	Erase	Read
Bit 1	V_g	9V	-5V	2.3V
	V_d	9V	10V	0V
	V_s	0V	0V	>1.6V
Bit 2	V_g	9V	-5V	2.3V
	V_d	0V	0V	>1.6V
	V_s	9V	10V	0V

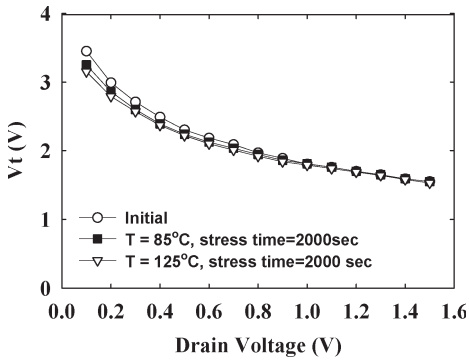


Fig. 5. Vertical charge migration characteristics of the HfO_2 nanocrystal Flash memory cells after 10 k P/E cycling.

Therefore, this proposed technique can detect the lateral profile of the trapped electrons. To enhance the storage charge movement in the HfO_2 nanocrystal trapping layer, the programmed samples were subjected to high-temperature baking at 80 °C and 125 °C for 2000 s, respectively. Remarkably, the $V_t - V_d$ curves for the cycled device and the baked devices exhibit very little difference, suggesting that lateral migration of the storage charges in the HfO_2 nanocrystal trapping layer is rather

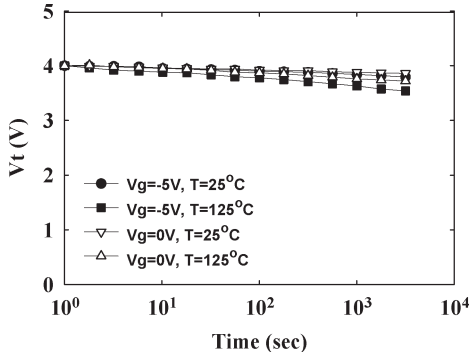


Fig. 6. Lateral charge migration characteristics of the HfO_2 nanocrystal Flash memory cells after 10 k P/E cycling.

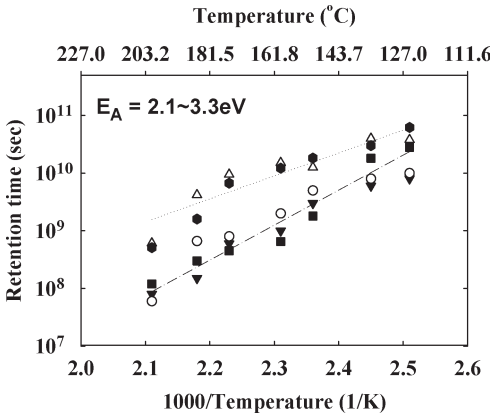


Fig. 7. Activation energy characteristics of the HfO_2 nanocrystal Flash memory cells taken from five samples.

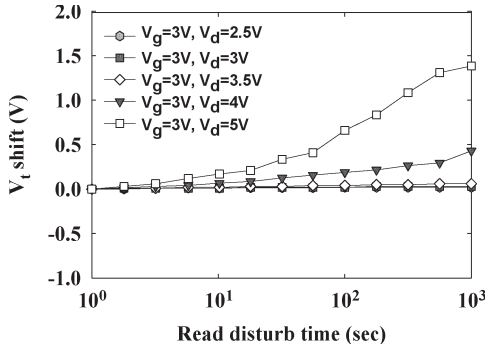


Fig. 8. Read disturbance characteristics of the HfO_2 nanocrystal memory devices. No significant V_t shift occurred for $V_d < 4$, even after 1000 s at 25 °C.

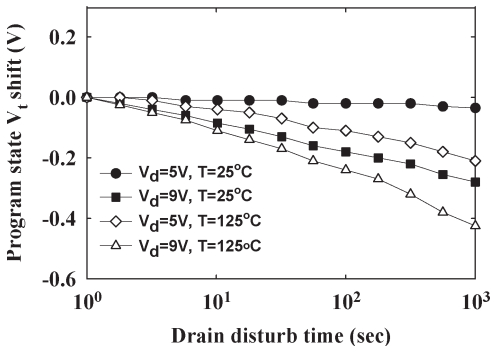


Fig. 9. Drain disturbance characteristics of the HfO_2 nanocrystal memory cells. After 1000 s at 25 °C, only a 0.3-V drain disturb margin was observed.

insignificant. It was attributed to the effective isolation of each nanocrystal within the SiO_2 matrix. Next, we investigated the influence of the vertical field on charge retention, i.e., vertical migration. Fig. 6 shows the V_t variation over time for various stress conditions for the 10 k P/E cycled cells. Visible charge loss was observed when the applied gate voltage and temperature were raised up to -5 V and 125 °C. We thought that although the trap energy level in the nanocrystal is quite deep, the generated defects and interface traps of the 2-nm tunnel oxide after 10 k P/E cycled stress will help stored charges escape via trap-assisted tunneling. Therefore, vertical charge migration is more observable than lateral charge migration in our memory cell. We also calculated the activation energy for the traps of the HfO_2 nanocrystals in the new cells (Fig. 7). Activation energy tracing is used widely to characterize the Arrhenius relation extracted from the temperature dependence of charge loss from nonvolatile memory as a function of time. For a given charge loss threshold criterion (in our case, 20% is used), the failure rates obtained at high temperature (125 °C–200 °C) can then be extrapolated to the nominal operating conditions. The model is based on a classical temperature-activated Arrhenius law, expressed in the form $t_R = t_0 \times e^{E_a/kT}$, where t_0 is the retention time corresponding to an infinite temperature, E_a is the activation energy, T is the temperature, and k is the Boltzmann constant [21]. The activation energy, which is determined from the slopes of five samples, lies in the range 2.1–3.3 eV, Obviously, it is higher than those values previously reported for conventional SONOS memories [22]–[24].

B. Disturbance

Fig. 8 demonstrates the read-disturbance-induced erase-state threshold voltage instability in a localized HfO_2 nanocrystal trapping storage Flash memory cell under several operation conditions. For a two-bit operation, the applied bitline voltage in a reverse-read scheme must be sufficiently large (> 1.5 V) to be able to "read through" the trapped charge in the neighboring bit. The read-disturb effect is the result of two factors: the word line and the bit line. The word-line voltage during read may enhance RT drift in the neighboring bit [25]. On the other hand, a relatively large read bit-line voltage may cause unwanted channel hot-electron injection and, subsequently, result in a significant threshold voltage shift of the neighboring bit. In our measurements, the gate and drain biases were applied and the source was grounded. The results demonstrate clearly that almost no read disturbance occurred in our HfO_2 nanocrystal Flash memory under low-voltage reading ($V_g = 3$ V; $V_d = 2.5$ V). For a larger memory window, we found that only a small read disturbance (ca. 0.3 V) can be observed after operation at $V_d = 4$ V after 1000 s at 25 °C.

Fig. 9 shows the programming drain disturbance of our HfO_2 nanocrystal Flash memory. Two different drain voltages ($V_d = 5$ and 9 V) were applied in the programming drain disturbance measurements at two different temperatures ($T = 25$ °C and 125 °C). We observed that a sufficient programming

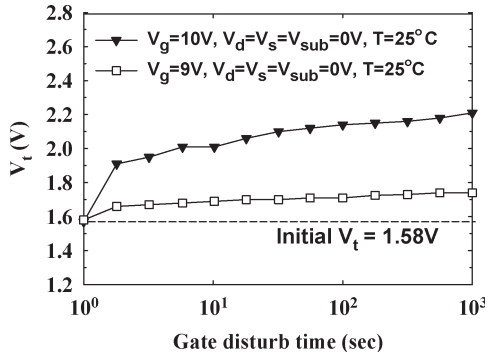


Fig. 10. Gate disturbance characteristics of the HfO_2 nanocrystal memory devices. A threshold voltage shift of only 0.22 V occurred after stressing at $V_g = 9$ V and $V_s = V_d = V_{\rm sub} = 0$ V for 1000 s.

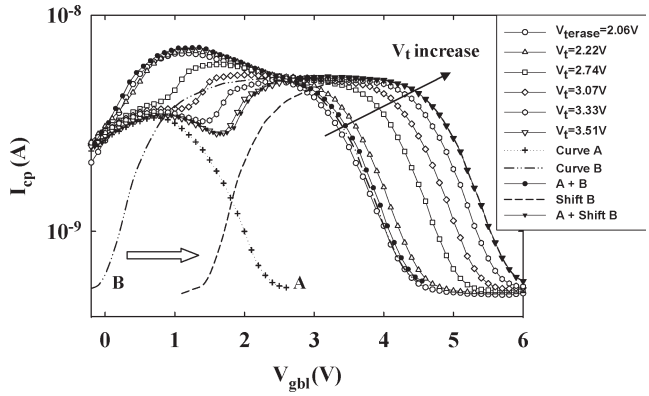


Fig. 11. Plots of $I_{\rm cp}$ versus $V_{\rm gbl}$ for the HfO_2 nanocrystal memory cell after F–N programming to different V_t levels.

drain disturb margin exists ($\Delta V_t < 0.4$ V), even after programming at a value of V_d of 9 V under high temperature ($T = 125\ ^\circ$C) and after stressing for 1000 s. Fig. 10 shows the gate disturbance characteristics in the erasing state. Gate disturbance may occur during programming for the cells sharing a common word line while one of the cells is being programmed. We observed a threshold voltage shift of only 0.16 V, i.e., negligible disturbance, under the following conditions: $V_g = 9$ V; $V_s = V_d = V_{\rm sub} = 0$ V; stressed for 1000 s. It is interesting to know why this memory can exhibit such excellent gate disturbance characteristics with such a thin tunnel oxide; a nonnegligible current will be present in the tunnel oxide when a voltage of 9 V is applied to the gate electrode. Using a serial capacitor voltage divider model, we estimated that the voltage drop at the tunnel oxide would be 0.98 V if the trapping layer is assumed to be an HfO_2 film rather than a nanocrystal. Although a 0.98-V drop will cause a significant leakage current through an individual 2-nm oxide layer, the data retention in the memory cell is related not only to the direct tunneling leakage current induced by such a voltage but also to the total tunneling situation in the whole gate stack, i.e., the effect that the potential barrier presented by the high-k material has on the tunneling current must be taken into account. In other words, it is incorrect to state that a large direct tunneling current will definitely exist in the interfacial layer and, in turn, that it will induce significant disturbance during programming.

C. Charge Pumping Characteristics

The charge pumping (CP) measurement was used to investigate the characteristics of our HfO_2 nanocrystal Flash memory. We used a trapezoidal gate pulse having a fixed pulse amplitude with varying $V_{\rm gbl}$. The substrate current (the so-called "charge pumping current," $I_{\rm cp}$) as a function of $V_{\rm gbl}$ was measured. The gate pulse have a frequency of 1 MHz and a 50% duty cycle; the rising and falling times were both 2 ns. Fig. 11 shows plots of the program-state charge pumping current $I_{\rm cp}$ versus $V_{\rm gbl}$ for our HfO_2 nanocrystal memory cell. Fowler–Nordheim (F–N) tunneling was used to program the cell with V_t levels from 2.06 to 3.51 V. The open symbols represent the measured data. The program-state $I_{\rm cp}$ curve shifted increasingly toward the right upon increasing the value of V_t as a result of an increase in the amount of injected charge in the HfO_2 nanocrystal trapping layer. Interestingly, a hump appeared in the left-hand edge of the curve in compliance with this shift. We decompose the resultant $I_{\rm cp}$ curve mathematically into two individual curves, i.e., A and B, in a fresh memory cell. We speculate that these two $I_{\rm cp}$ curves arise from interlacing of the SiO_2 matrix and HfO_2 nanocrystals within the trapping layer. In other words, the memory is composed of two kinds of devices that have different gate dielectric configurations. The extracted threshold voltage in curve A is larger than that in curve B, even for a fresh memory, because the value of equivalent oxide thickness (EOT) of the gate stack in the region containing SiO_2 matrix is larger than that in the part containing the HfO_2 nanocrystals. We believe that curve A is related to the SiO_2 matrix, and curve B corresponds to the HfO_2 nanocrystals. With programming, it is clear that the $I_{\rm cp}$ curve arising from the region containing the SiO_2 matrix undergoes almost no shift, and the resultant distortion appearing in the measured $I_{\rm cp}$ curve is caused mainly by the charging of the HfO_2 nanocrystal. This result implies that the programming charge was stored almost entirely within or around the HfO_2 nanocrystal rather than in the SiO_2 matrix. To confirm this hypothesis, we traced the measured curve by adding curve A to a horizontally shifted curve B; this approach works quite well. In addition, we also analyzed the devices formed from a pure HfO_2 trapping layer on top of an SiO_2 tunnel oxide structure. It was observed that only curve B shifted horizontally when programming (data not shown). Consequently, we conclude that HfO_2 nanocrystals can behave as an excellent local charge trapping centers.

D. Characteristics After P/E Cycling

Fig. 12 shows the endurance characteristics of the HfO_2 nanocrystal memory cell. The programming and erasing conditions were $V_g = V_d = 9$ V for 10 μs and $V_g = -5$ V, $V_d = 10$ V for 1 ms, respectively. Remarkably, the values of V_t in the program and erase states did not increase significantly up to 10^5 P/E cycles, whereas the memory window underwent a significant narrowing after 10^6 cyclic operations. The spatial distributions for electron and holes are localized during the channel hot-electron injection and band-to-band hot-hole injection for the programming and erasing, respectively, of our HfO_2 nanocrystal memory. If the electron distribution does

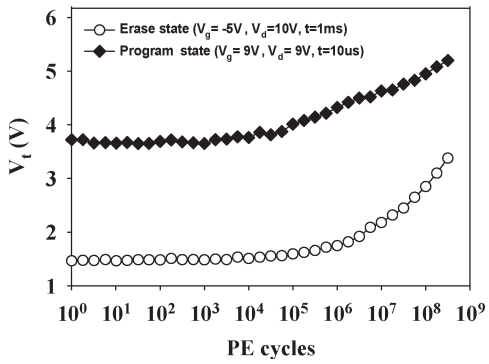


Fig. 12. Endurance characteristics of the HfO_2 nanocrystal memory after 10 k P/E cycling.

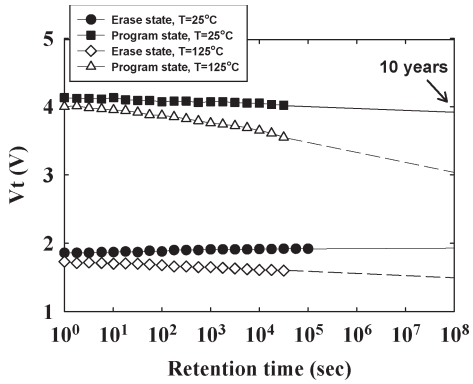


Fig. 13. Retention characteristics of the HfO_2 nanocrystal memory after 10 k P/E cycling at 25 °C and 125 °C. No significant charge loss occurred at 25 °C, and only a very low charge loss occurred at 125 °C.

not completely match that for the hole, then each P/E cycle will leave a few electrons in the trapping layer [26]. This so-called "hard-to-erase" phenomenon cannot be eliminated readily when using band-to-band hot-hole erasing. Obviously, this is not an issue for our memory because the enhanced local electric field across the thin tunnel oxide in the region just beneath the nanocrystals can help in the injection of holes. Fig. 13 illustrates the retention characteristics of the HfO_2 nanocrystal memory devices for a 10 k P/E stressed HfO_2 nanocrystal memory cell both at RT ($T = 25$ °C) and above ($T = 125$ °C). Relative to the fresh device, the device operated at RT retained its good retention time (up to 10^5 s) for 10% charge loss [16]. We ascribe this result to the combined effects of the tight embrace of the HfO_2 nanocrystals by the SiO_2-rich matrix and the sufficiently deep trap energy level of our memories (extracted activation energy: 2.1–3.3 eV). Therefore, despite the tunnel oxide having a thickness as low as 2 nm, no significant lateral or vertical charge migration occurred; as a result, the device displays superior retention characteristics for charge storage. At the temperature at 125 °C, we observed a more significant charge loss during the program state. This strong temperature dependence was predictable from the large activation energy, but the detailed mechanism remains under further investigation. Table III presents a comparison of our results with those of recent investigations into new devices [2], [5], [8]. Our system shows a number of salient features. First, our HfO_2 nanocrystal memories exhibit larger memory windows than do the other systems because of the large trap density of the high-k dielectric materials. Second, with respect to the P/E speed, we obtained a high speed of operation because we used channel hot-electron programming and band-to-band hot-hole erasing. Finally, we observed good retention with no vertical or lateral migration as a result of the HfO_2 na nocrystals being isolated effectively within the SiO_2 matrix.

TABLE III
MEMORY CHARACTERISTICS OF THE DEVICE FABRICATED IN THIS STUDY AND THE COMPARISON WITH REPORTED DATA FOR VARIOUS SONOS-TYPE MEMORY CELLS

	Memory windows (volts)	20% charge loss at RT (sec.)	Write/ Erase speed (sec.)	Migration
This Work	1.2V ~5V	$>10^8$	P:$>10^{-6}$ E:$>10^{-4}$	No migration
HfO2 [8]	1.5V ~4V	$>10^5$	P:$>10^{-6}$ E:$>10^{-4}$	Lateral
Si dots [2]	0.5V ~2.2V	$>10^8$	P:$>10^{-6}$ E:$>10^{-1}$	N/A
Metal dots [5]	1V ~7V	$>10^6$	P:$>10^{-3}$ E:$>10^{-3}$	N/A
SONOS [8]	1.2V ~5.2V	$>10^8$	P:$>10^{-6}$ E:$>10^{-5}$	Vertical

IV. CONCLUSION

In this paper, we propose a novel, simple, reproducible, and reliable technique for the design of high-density HfO_2 nanocrystals through the spinodal decomposition of hafnium silicate. Our nanocrystal memory exhibits superior characteristics in terms of negligible lateral or vertical migration of stored charge and good disturbance characteristics. The cells after 10 k P/E cycling also show a long retention time and excellent endurance. With this superior performance, we believe that HfO_2 nanocrystal Flash memory is quite suitable for the two-bit operation and that it has great potential for replacing the ONO stack in conventional SONOS-type Flash memories.

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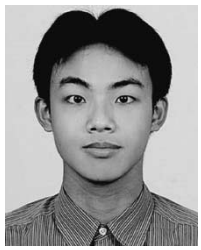

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