Evaluation of Stability, Performance of Ultra-Low Voltage MOSFET, TFET, and Mixed TFET-MOSFET SRAM Cell With Write-Assist Circuits

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***Abstract*—In this work, we propose a mixed TFET-MOSFET 8T SRAM cell comprising MOSFET cross-coupled inverters, dedicated TFET read stack and TFET write access transistors for ultra-low voltage operation. Exploiting both the merits of TFET and MOSFET devices, the proposed SRAM cell provides significant improvement in SRAM stability, V_{min} and performance. The stability and performance of the proposed cell are evaluated and compared with the conventional MOSFET 8T cell and pure TFET 8T cell using mixed-mode TCAD simulations based on published design rules for 22 nm technology node. Besides, the impacts of the device design of the proposed SRAM cell on the stability are also investigated. Various write-assist techniques to enhance the write-ability across $V_{DD} = 0.2$ to 0.7 V for these SRAM cells are comparatively assessed. The results indicate that the proposed mixed TFET-MOSFET cell topology is viable for ultra-low voltage operation while MOSFET cell provides better stability and performance for high voltage operation.**

***Index Terms*—Tunnel field-effect transistor (TFET), TFET SRAMs, ultra-low voltage, write-assist circuits.**

I. Introduction

Reducing the power consumption in processors, mobile devices, and bio-medical electronics is one of the most challenging task. Voltage scaling is an efficient way to reduce the power consumption. The conventional 6T SRAM cell achieves large storage capacity. However, it suffers from read disturb, half-select disturb, and the conflicting read/write requirements. Consequently, the stability of 6T SRAM cell degrades significantly as V_{DD} scales down, limiting the achievable V_{min} for overall system.

Tunnel field-effect transistor (TFET) device with the band-to-band tunneling as the major current transport mechanism enables steeper than 60 mV/dec subthreshold swing, and is considered as a promising device to replace MOSFET device for ultra-low voltage/power operation [1]–[5]. However, the asymmetric source/drain design and transport mechanism result in uni-directional current conduction [6], which severely impacts the pass-gate based circuits and SRAMs [6]–[9].

In this work, we propose a mixed TFET-MOSFET 8T SRAM cell which exploits both the advantages of TFET and MOSFET devices for ultra-low voltage operation. The merits of the proposed cell versus the conventional MOSFET 8T SRAM cell and the pure TFET 8T SRAM cell in stability and performance are comprehensively assessed [26]. Besides, the impacts of the threshold voltage design of the MOSFET and TFET devices and the device design parameters of the TFET devices on the SRAM stability and V_{min} are also investigated. With increasing variability for scaled devices, read/write-assist circuits are indispensable for SRAM, especially at low voltage. Various write-assist techniques including the negative bit-line (NBL) write-assist [22], transient voltage collapse (TVC) write-assist [23], [24], and data-aware write-assist [25] are extensively assessed and compared for these SRAM cells.

This paper is organized as follows. Section II introduces the device design, characteristics, and TCAD simulation methodology used in this work. Section III describes the proposed mixed TFET-MOSFET 8T cell including the impacts of different device designs. Section IV presents the cell layouts based on published design rules for 22 nm technology node. Section V comparatively addresses the stability and performance, and evaluates various write-assist circuit techniques for these SRAM cells. Section VI concludes the paper.

II. Device Design, TCAD Methodology, and Switching Characteristics

A. Device Design and TCAD Methodology

In this work, we consider the PNPN type TFET [3] for its capability to achieve sub-threshold swing below 60 mV/dec at room temperature. The device structures of the PNPN TFET, p-i-n TFET and conventional MOSFET are shown in Fig. 1. Notice that p-i-n TFET, with inferior sub-threshold swing and drive current compared with PNPN TFET [27], is included here for investigation of the stability and V_{min} of the proposed mixed SRAM cell with different TFET device designs hence different TFET device characteristics in Section IV. Double-gate (DG)

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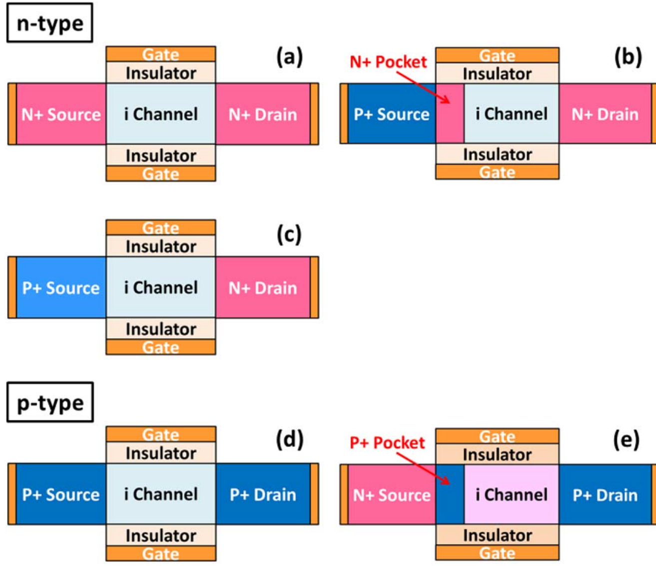

Fig. 1. Structures of (a) n-type MOSFET, (b) n-type PNPN TFET, (c) n-type p-i-n TFET, (d) p-type MOSFET, and (e) p-type NPNP TFET.

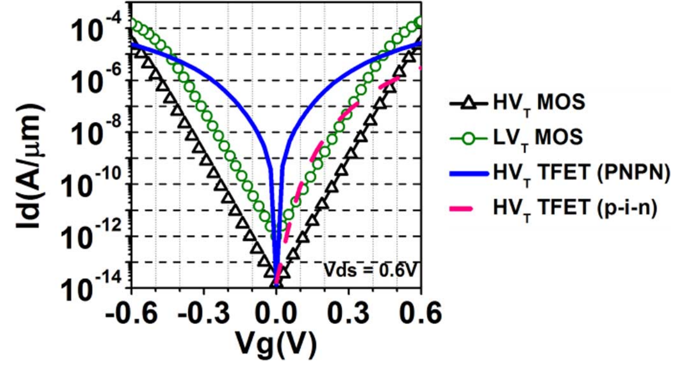

Fig. 2. Ids-Vgs characteristics at $\mathrm{Vds} = 0.6$ V of n-/p-type DG $\mathrm{LV_T}$ and $\mathrm{HV_T}$ MOSFET devices, DG PNPN/NPNP TFET devices, and DG p-i-n TFET device.

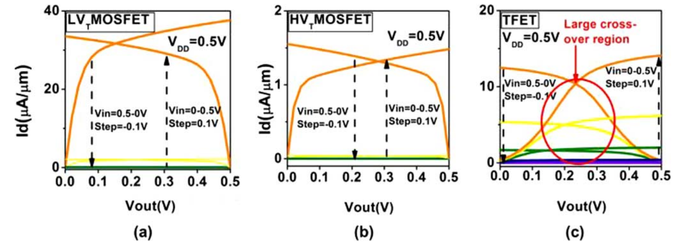

Fig. 3. Device switching characteristics of (a) DG $\mathrm{LV_T}$ MOSFET, (b) DG $\mathrm{HV_T}$ MOSFET, and (c) DG TFET in an inverter.

structures are used, with the gate length $\mathrm{L_{eff}} = 25$ nm, silicon body thickness $\mathrm{T_{Si}} = 6$ nm, equivalent oxide thickness $(\mathrm{EOT}) = 0.6$ nm, high-κ dielectric $(\mathrm{HfO_2}, \mathrm{permittivity} = 25)$, the $\mathrm{n^+}$ and $\mathrm{p^+}$ regions doped to $2 \times 10^{20}/\mathrm{cm}^3$, and the pocket region doped to $1.2 \times 10^{20}/\mathrm{cm}^3$. Fig. 2 shows the Ids-Vgs characteristics of the TFET (PNPN/NPNP), p-i-n TFET, and $\mathrm{LV_T}$ and $\mathrm{HV_T}$ DG MOSFET (N/PMOS) at $\mathrm{Vds} = 0.6$ V. The TFET and MOSFET devices/circuits are analyzed using atomistic TCAD mixed-mode simulations. The nonlocal band-to-band tunneling model which is applicable to arbitrary tunneling barrier with nonuniform electric field is used for TFET simulations [16]. The tunneling paths are dynamically determined according to the gradient of the band energy. The $\mathrm{I_{on}/I_{off}}$ ratio and S.S. of PNPN TFET device are calibrated with [3] and the OFF state current is set with available Si TFET experimental data. The p-i-n TFET device is designed to have the same OFF state current as the PNPN TFET device. The DG MOSFET devices with two different $\mathrm{V_T}$ designs are considered to investigate the impact of different MOSFET $\mathrm{V_T}$ designs on the SRAM stability and performance. The $\mathrm{HV_T}$ MOSFET device is designed with the same OFF state current as the PNPN TFET device for low power operation, while the $\mathrm{LV_T}$ MOSFET device is designed with higher leakage current around pA/μm as shown in Fig. 2. The PNPN TFET device can be seen to have superior current drive and subthreshold slope at very low gate bias, followed by a broad soft transition region before its current saturates. While at high gate bias, the current drive of PNPN TFET device is inferior to the $\mathrm{LV_T}$ MOSFET.

B. Device and Circuit Switching/Output Characteristics

Fig. 3 show the switching Id-Vds characteristics of $\mathrm{LV_T}, \mathrm{HV_T}$ MOSFET and PNPN TFET devices in an inverter. The delayed saturation in TFET device results in large cross-over region/current between the n-type and p-type devices in TFET inverter which degrades the sharpness of voltage transfer characteristic (VTC) of the TFET inverter and the stability in TFET SRAM cell. In the following sections, “p-i-n TFET” will be explicitly stated, and “TFET” will be used for “PNPN” TFET devices for simplicity.

III. Ultra-Low Voltage SRAM Cell Designs

A. Conventional MOSFET/TFET 8T SRAM Cell

The conventional 6T SRAM cell faces many challenges with increasing variations in deep sub-100 nm technologies [10], especially at low supply voltages. Alternative SRAM cells such as 8T cell and 10T cell have been proposed for robust low voltage operations [11]–[15]. In this work, the conventional 8T SRAM cell [11], which utilizes dedicated read buffer to decouple the read current from the cell storage node to eliminate the read disturb and enhance the read stability, is used as the basic cell structure due to its technical viability with uni-directional TFET devices. Fig. 4 shows the schematics of MOSFET/TFET 8T SRAM cell structures and the corresponding read/write current paths. The bracket in the symbol of TFET device indicates the tunnel junction in the TFET device.

For MOSFET 8T SRAM cell, the read disturb is eliminated through the dedicated read stack which decouples the cell storage nodes from read current while the bi-directional write access transistors provide the “push-pull” action to enhance write-ability during write operation. However, MOSFET 8T SRAM cell suffers from write half-select disturb (Fig. 5) where the half-select cells on the selected row $(\mathrm{WWL}[0] = \mathrm{V_{DD}})$ perform “dummy” read, thus experiencing cell disturb similar to the read disturb in the conventional 6T cell. The MOSFET 8T SRAM cell is thus not suitable for bit-interleaving architecture.

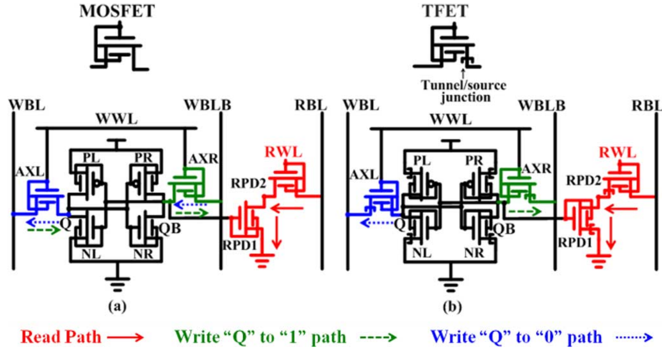

Fig. 4. Cell structures and corresponding read/write paths for (a) conventional MOSFET 8T SRAM cell and (b) TFET 8T SRAM cell.

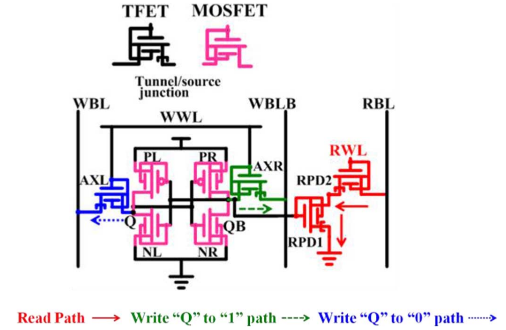

Fig. 6. Cell structure and corresponding read/write paths of proposed mixed TFET-MOSFET 8T SRAM cell where MOSFET devices are used in the cross-coupled inverter pair.

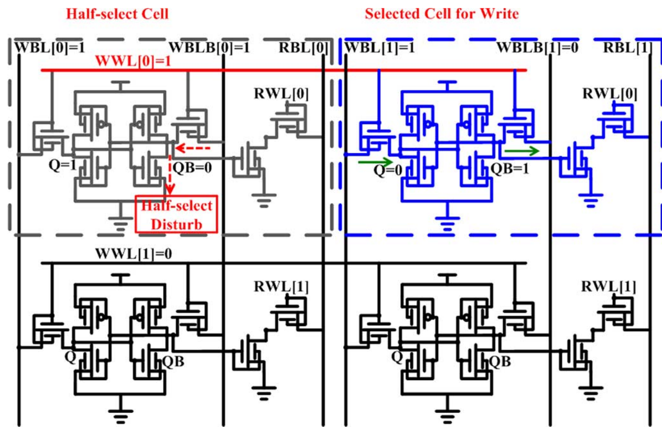

Fig. 5. Schematic of 8T SRAM cell array showing the selected cell for Write and half-select disturb current path through the half-selected cell for MOSFET 8T SRAM.

For TFET 8T SRAM cell, the read stability is improved by the dedicated read stack as in the MOSFET 8T cell. Moreover, the superior current drive and subthreshold slope of TFET at low voltage significantly enhance the read performance over the MOSFET 8T cell at low voltage. Furthermore, the uni-directional write access transistors eliminate write half-select disturb, thus facilitating bit-interleaving architecture for enhanced soft error immunity with error correction code (ECC) [17]. However, there are two drawbacks for the TFET 8T cell. First, the large cross-over region in TFET device degrades the hold/read static noise margin (HSNM/RSNM) and write static noise margin (WSNM). Secondly, the lack of "push-pull" action during write operation due to uni-directional write access transistors degrades the write-ability.

B. Mixed TFET-MOSFET 8T SRAM Cell

Based on the previous discussion of the pros and cons of MOSFET and TFET 8T SRAM cells and realizing that mixing TFET and MOSFET devices is manufacturally possible since the process of TFET device is compatible with CMOS process [5], Fig. 6 shows the proposed mixed TFET-MOSFET 8T SRAM cell and corresponding read/write paths. The cell features MOSFET cross-coupled inverters for improved HSNM and RSNM, dedicated TFET read stack for enhanced read stability and read performance and TFET write access transistors to facilitate bit-interleaving architecture. Furthermore, with MOSFET cross-coupled inverters, the write-ability of the proposed mixed TFET-MOSFET 8T cell is significantly enhanced over the MOSFET 8T cell and TFET 8T cell in the low voltage regime due to the disparity of the current drive between the write access TFET device and the holding (pull-up) PMOSFET at low voltage. By properly designing the TFET and MOSFET devices to increase the voltage where TFET current and MOSFET current cross-over (e.g., III-V TFET or V_T designs on MOSFET and TFET devices), the effective voltage range for improved write-ability of the mixed TFET-MOSFET cell will be broadened. The impact of different TFET device design (e.g., p-i-n TFET) and the V_T design of the MOSFET device on the SRAM stability and performance of the mixed TFET-MOSFET 8T cell will be addressed in Section IV. Exploiting both the merits of TFET and MOSFET devices, the proposed mixed TFET-MOSFET 8T cell provides significant improvement in SRAM stability, V_{min} and performance for ultra-low voltage operation. It should be noted that the proposed cell utilizes the disparity of current drive between TFET device and MOSFET device for improved write-ability at ultra-low voltage. However, at higher supply voltage, the current drive disparity reverses, and MOSFET device provides higher current drive than the TFET device (Fig. 2). While TFET-based circuits aim at energy-efficient ultra-low voltage operation, it would be desirable in practice to cover higher V_{DD} range up to 0.5–0.7 V. Hence, write-assist circuits to extend TFET or mixed TFET-MOSFET SRAM cell operation to 0.5–0.7 V need to be developed. This will be addressed in Section V.

IV. Stability and Layout

In this section, the stability and layout of the MOSFET, TFET, and mixed TFET-MOSFET 8T SRAM cell are comparatively assessed.

A. Stability

Fig. 7 show the respective hold, read, write, and half-select SNM of the LV_T and HV_T MOSFET 8T cell, TFET 8T cell, mixed p-i-n TFET-MOSFET 8T cell comprising HV_T MOSFET cross-coupled inverters and mixed TFET-MOSFET

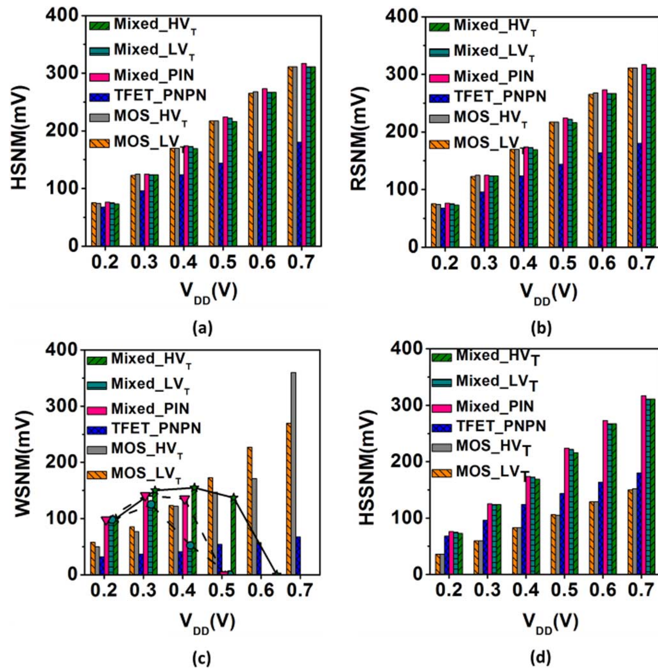

Fig. 7. Stability of LV_T and HV_T MOSFET 8T SRAM cell, TFET SRAM cell, mixed p-i-n TFET-MOSFET 8T SRAM cell comprising HV_T MOSFET cross-coupled inverter and mixed TFET-MOSFET 8T SRAM cell comprising LV_T and HV_T MOSFET cross-coupled inverter across $V_{DD} = 0.2$ V–0.7 V: (a) HSNM, (b) RSNM, (c) WSNM, and (d) HSSNM.

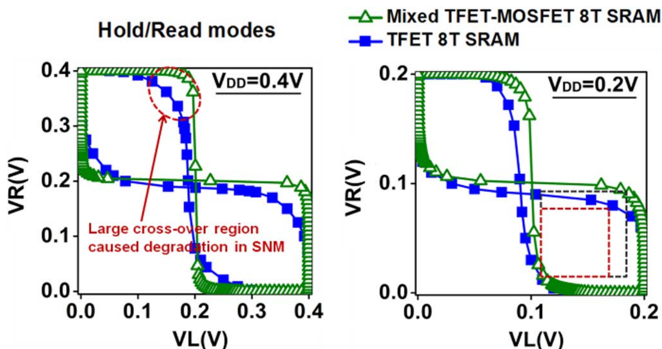

Fig. 8. Butterfly curves of TFET and mixed TFET-MOSFET 8T SRAM cell comprising HV_T MOSFET cross-coupled inverter in hold/read modes at $V_{DD} = 0.4$ V and $V_{DD} = 0.2$ V.

8T cell comprising LV_T and HV_T MOSFET cross-coupled inverters, respectively, for V_{DD} ranging from 0.2 V to 0.7 V.

1) *Hold/Read SNM*

For 8T cell configuration, the read SNM (RSNM) equals hold SNM (HSNM). As shown in Fig. 7(a) and (b), both the LV_T and HV_T MOSFET 8T cell and the mixed TFET-MOSFET 8T cell comprising of LV_T and HV_T MOSFET cross-coupled inverters exhibit comparable HSNM and RSNM. The TFET 8T cell shows larger degradation in both HSNM and RSNM, especially for $V_{DD} \geqq 0.3$ V, due to the large cross-over region in TFET devices which degrades the sharpness of cell inverter VTC and can be observed in the transition region of the butterfly curves shown in Fig. 8. The actual amount of degradation will depend on the output conductance of the manufactured TFET devices and MOSFET devices in weak inversion conditions. As V_{DD} scales down to 0.2 V, the HSNM/RSNM degradation of the TFET 8T cell becomes less as cross-over region in TFET devices is reduced.

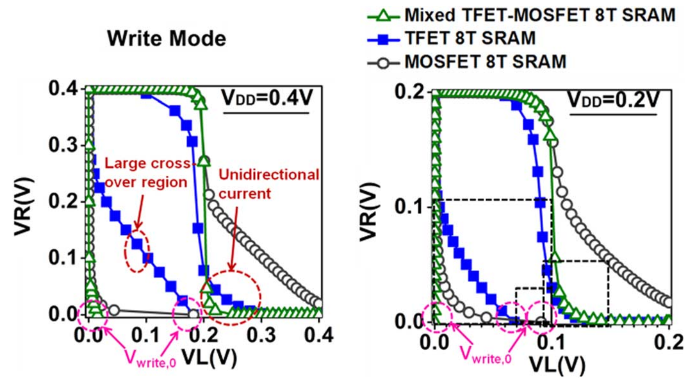

Fig. 9. Butterfly curves of HV_T MOSFET, TFET, and mixed TFET-MOSFET 8T SRAM cell comprising HV_T MOSFET cross-coupled inverters in write mode at $V_{DD} = 0.4$ V and $V_{DD} = 0.2$ V.

2) *Write SNM*

Fig. 7(c) shows the write SNM (WSNM) of the SRAM cell topologies versus V_{DD}. The TFET 8T cell shows significant degradation in WSNM across V_{DD} range from 0.2 V to 0.7 V since the uni-directional conduction of TFET write-access transistor deprives the push-pull action during write operation, which can be observed in the write butterfly curves of TFET and mixed TFET-MOSFET 8T cell in Fig. 9(a). Meanwhile, the large cross-over region in TFET devices causes large $V_{Write,0}$ (determined by the current balance between the write access transistor and the holding transistor) as shown in Fig. 9(a), thus further degrading the write-ability. As V_{DD} scales down to 0.2 V, the WSNM of TFET 8T cell becomes comparable to that of MOSFET 8T cell as shown in Fig. 9(b) since the cross-over transition region is reduced. Among the SRAM cell topologies, for low voltage operation ($V_{DD} < 0.5$ V), the proposed mixed TFET-MOSFET 8T cell comprising HV_T MOSFET cross-coupled inverter exhibits superior WSNM with 150% to 310% improvement compared with the TFET 8T SRAM cell. While the proposed cell still lacks push–pull action during write operation, the $V_{Write,0}$ is significantly reduced, especially at low voltages, due to the steep swing of the TFET device and the disparity of current drive between the write access TFET and the holding PMOSFET, thus providing most significant improvement in write-ability among all these SRAM topologies. However, for the proposed mixed TFET-MOSFET 8T cell comprising LV_T MOSFET devices and that of the proposed mixed cell using p-i-n TFET and HV_T MOSFET devices, they exhibit worse write-ability and the WSNM diminishes at $V_{DD} = 0.5$ V. This is due to decrease of the drive current disparity between the write access PNPN TFET/p-i-n TFET devices and LV_T/HV_T holding PMOSFET. It should be noted that the proposed mixed TFET-MOSFET SRAM topology

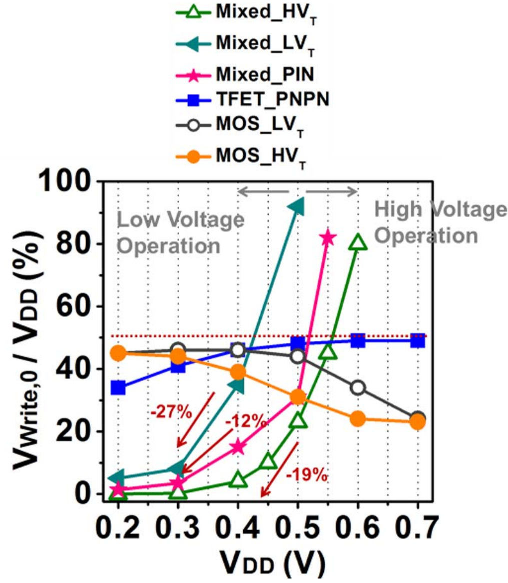

Fig. 10. Weighting of $V_{Write,0}$ versus V_{DD} of LV_T, HV_T MOSFET 8T SRAM cell, TFET 8T SRAM cell, mixed p-i-n TFET-MOSFET 8T SRAM cell comprising HVT MOSFET cross-coupled inverter, and mixed TFET-MOSFET 8T SRAM cell comprising LV_T and HV_T MOSFET cross-coupled inverter from $V_{DD} = 0.2$ V to 0.7 V.

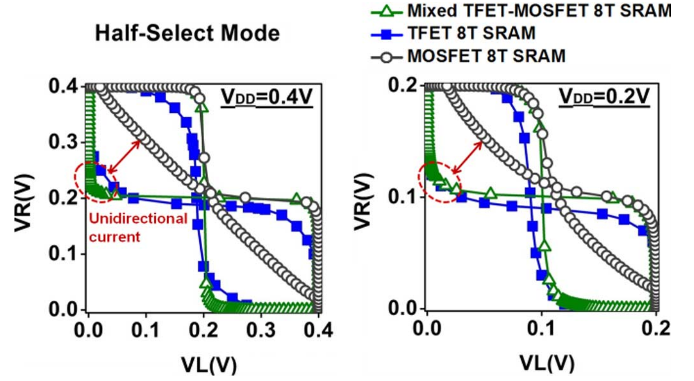

Fig. 11. Butterfly curves of HV_T MOSFET, TFET, and mixed TFET-MOSFET 8T SRAM cell comprising HV_T MOSFET cross-coupled inverters in half-selected mode at $V_{DD} = 0.4$ V and $V_{DD} = 0.2$ V.

is suitable for other MOSFET and TFET device structures. However, since the ON state current of the TFET device and the subthreshold swing are not as good as PNPN TFET device, and the MOSFET device has very low threshold voltage, the write-ability becomes worse and the write operation range becomes narrower. Hence, the MOSFET and TFET device should be carefully designed to have large write operation range.

It should also be noticed that the WSNM of the mixed TFET-MOSFET 8T cell shows an unique reflective trend as indicated by the dashed lines in Fig. 7(c) and the margin vanishes as V_{DD} is raised above 0.6 V for mixed TFET-MOSFET SRAM cell comprising HV_T cross-coupled inverters, while the WSNMs of MOSFET and TFET 8T cells exhibit monotonic trend with V_{DD}. This is because as V_{DD} becomes higher, the current drive of the holding PMOSFET overwhelms that of the write access TFET as shown in Fig. 2, resulting in significantly larger $V_{Write,0}$ which can be observed in Fig. 10. As a result, write failure occurs. On the other hand, when V_{DD} scales down to below 0.6 V, the disparity of the current between the holding HV_T PMOSFET and write access TFET reverses and write stability improves. Between 0.5 V and 0.4 V, the decrement of $V_{Write,0}$ of the proposed cell is larger than the reduced margin caused by lowered supply voltage which can be clearly seen with the weighting of $V_{Write,0}$ versus V_{DD} shown in Fig. 10, thus causing a reflection point near $V_{DD} = 0.4$ V. Similar trend can be observed for mixed TFET-MOSFET SRAM cell comprising LV_T cross-coupled inverters and for mixed cell using p-i-n TFET device and HV_T cross-coupled MOSFET devices. The proposed cell with HV_T MOSFET devices provides sufficient write-ability at ultra-low supply voltage for V_{DD} below 0.5 V. Additional write-assist circuit would be required to extend V_{DD} above 0.6 V, and will be discussed in Section V.

3) *Half-Select SNM*

Fig. 7(d) shows the half-select SNM (HSSNM) of the SRAM cell topologies versus V_{DD}. It is observed that TFET, mixed TFET-MOSFET, and mixd p-i-n TFET-MOSFET 8T cells with uni-directional TFET write access transistors show larger HSSNM than the MOSFET 8T cell. At $V_{DD} = 0.5$ V, the enhancement of HSSNM of mixed TFET-MOSFET 8T cell is about 106% and 50% compared with the MOSFET 8T cell and TFET 8T cell, respectively. The large improvement results from the fact that with uni-directional TFET write access transistors, the "dummy" read current of the half-selected cells cannot flow through the cell storage nodes, hence the half-selected disturb is significantly reduced. This can be clearly observed in the butterfly curves shown in Fig. 11 indicated by the spanning arrows. For the proposed mixed TFET-MOSFET 8T cell with the MOSFET cross-coupled inverters, the HSSNM improves further due to sharper VTC (reduction of the cross-over region) compared with the TFET cross-coupled inverters as shown in Fig. 11.

The stabilities of the SRAM cell topologies are summarized in Table I where the LV_{DD} indicates operating at low supply voltages ($V_{DD} \leqq 0.5$ V) and HV_{DD} indicates operating at high supply voltages. The circle symbol indicates excellent stability, the triangle indicates moderate stability, while the cross stands for poor stability. It is clear that for operating at ultra-low voltage, the proposed mixed TFET-MOSFET 8T SRAM cell comprising HV_T cross-coupled inverters provides substantial merits over the MOSFET and TFET 8T SRAM cell. While for operating at high supply voltage, the MOSFET 8T SRAM cell appears to provide better stability.

For the following section, we will assess the layout and SRAM performance. Here, we use the HV_T MOSFET, TFET, and mixed TFET-MOSFET 8T cell comprising HV_T MOSFET cross-coupled inverters as examples.

TABLE I
COMPARISON OF STABILITY FOR LV_T, HV_T MOSFET 8T SRAM CELL, TFET 8T SRAM CELL, MIXED p-i-n TFET-MOSFET 8T SRAM CELL COMPRISING HV_T MOSFET CROSS-COUPLED INVERTER AND MIXED TFET-MOSFET 8T SRAM CELL COMPRISING LV_T AND HV_T MOSFET CROSS-COUPLED INVERTER FOR OPERATING AT LOW SUPPLY VOLTAGE AND HIGH SUPPLY VOLTAGE, RESPECTIVELY

Type	Mixed HV_T MOS		Mixed LV_T MOS		Mixed p-i-n HV_T MOS	
	LV_{DD}	HV_{DD}	LV_{DD}	HV_{DD}	LV_{DD}	HV_{DD}
Hold SNM	O	O	O	O	O	O
Read Disturb Free	O	O	O	O	O	O
Write-ability	O	X	△*	X	△*	X
Half-Select Disturb Free (Bit-interleave)	O	O	O	O	O	O
Type	TFET		HV_T MOS		LV_T MOS	
	LV_{DD}	HV_{DD}	LV_{DD}	HV_{DD}	LV_{DD}	HV_{DD}
Hold SNM	△	△	O	O	O	O
Read Disturb Free	O	O	O	O	O	O
Write-ability	X	△	△	O	△	△
Half-Select Disturb Free (Bit-interleave)	O	△	X	△	X	△

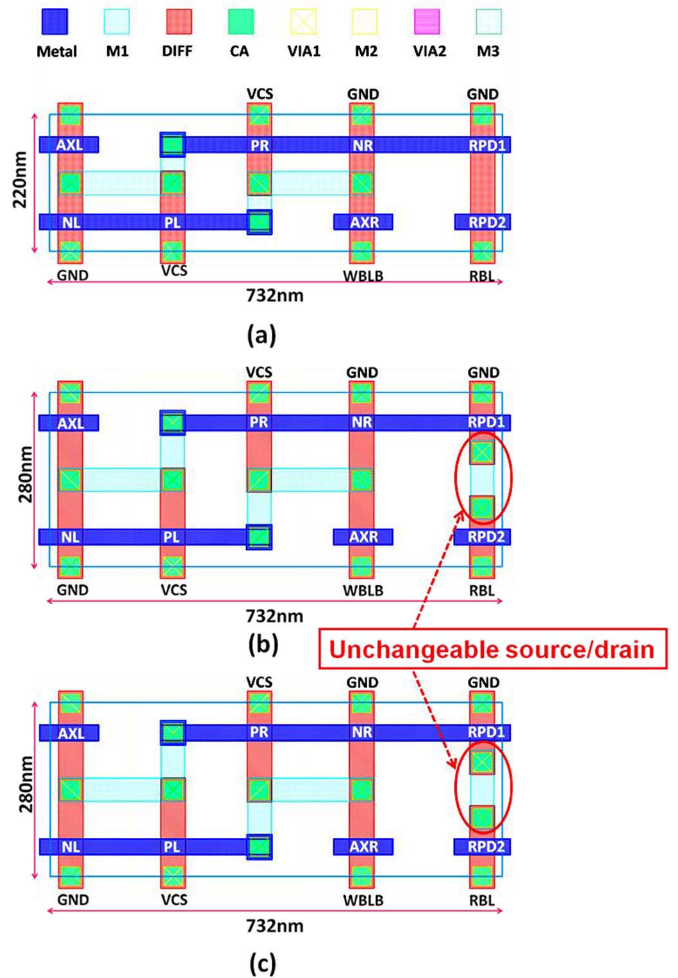

Fig. 12. Layout of (a) MOSFET 8T SRAM cell, (b) TFET 8T SRAM cell, and (c) mixed TFET-MOSFET 8T SRAM cell based on design rules listed in Table II.

B. Layout

Fig. 12(a), (b), and (c) shows the layout of MOSFET, TFET, and mixed TFET-MOSFET 8T cells, respectively. The layouts are based on published design rules for 22 nm technology node and proportionally estimated parameters [18]. Table II summarizes the pertinent design rules used in this work. Specifically, due to the asymmetrical source/drain design of TFET device, its source and drain are unexchangeable hence the layout of the TFET cell differs from that of the conventional MOSFET cell. As shown in Fig. 12(a) for MOSFET 8T cell, the source and drain of the stacked read transistors are exchangeable and can be shared. While in Fig. 12(b) and (c), for TFET and mixed TFET-MOSFET 8T cell, the stacked read transistors are TFET devices, and the vertical direction of the bit cells are expanded resulting from the unexchangeable source/drain, and the height of the bit cells is constrained by the minimum spacing rules between the diffusion layers. The area overhead of the TFET and mixed TFET-MOSFET 8T cell is about 27% compared with the MOSFET 8T cell.

TABLE II
LAYOUT DESIGN RULES

Parameters	Value(nm)
Leff	25
Minimum space between Metal	100
N/P Isolation	75
DIFF-DIFF	50
M1, M2 Pitch	80
Minimum Space Between M1	35
Minimum Space Between M2	35
Minimum Width of VIA	50

V. PERFORMANCE AND WRITE-ASSIST CIRCUIT TECHNIQUES

The performance of SRAM arrays with 16 cells per bit-line are assessed considering the worst case bit-line data pattern and bit-line loading estimated from the layout. As shown in Fig. 13(a), TFET 8T cell and mixed TFET-MOSFET 8T cell significantly outperform the MOSFET 8T cell in "cell" read access time (defined as the time from when selected read word-line (RWL) reaches half-V_{DD} to when the read bit-line (RBL) is pulled down to half-V_{DD}) for V_{DD} below 0.5 V, providing 4000x improvement at $V_{DD} = 0.2$ V. On the other hand, for V_{DD} above 0.6 V, MOSFET 8T cell provides better "cell" read performance with 10x improvement at $V_{DD} = 0.7$ V compared with TFET and mixed TFET-MOSFET 8T cell. This is

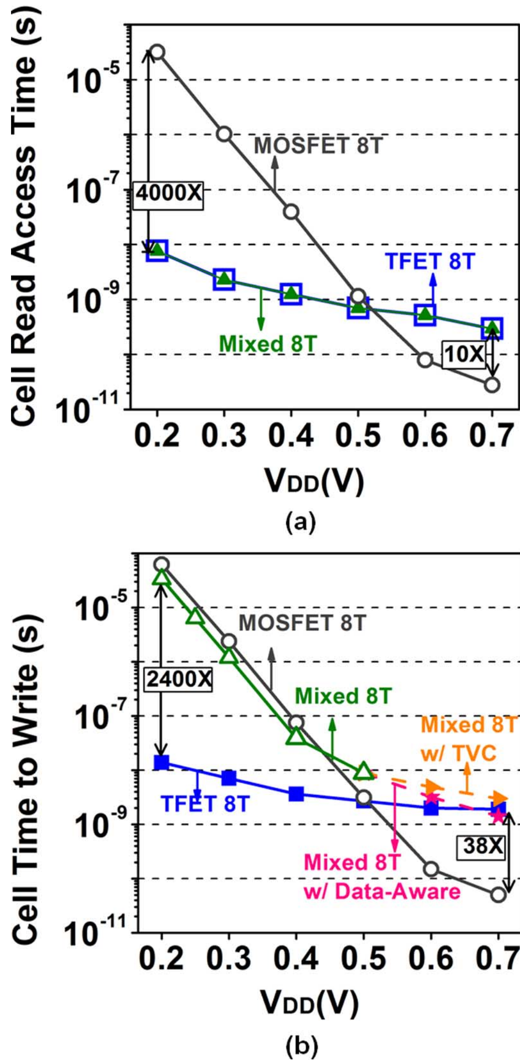

Fig. 13. Performance comparison of the MOSFET, TFET, and mixed TFET-MOSFET 8T SRAM cell for (a) cell read access time and (b) cell time-to-write.

because for V_{DD} below 0.5 V, TFET read transistors offer superior current drive and steep subthreshold swing compared with MOSFET devices, while for V_{DD} above 0.6 V, the current disparity reverses. Fig. 13(b) shows the "cell" time-to-write (defined as the time from the 50% activation of the Write Word-Line (WWL) to the time when the voltage of the cell storage node (pulling to "1") reaches 90% V_{DD}). For V_{DD} below 0.5 V, both MOSFET 8T cell and mixed TFET-MOSFET 8T cell exhibit substantial longer time-to-write than the TFET 8T cell. The "writing" process consists of two phases. In the initial phase of write operation, the write access transistor competes with the holding (pull-up) transistor to pull down the cell "1" storage node. In the second phase, the pull-up transistor of the opposite cell inverter pulls up the opposite cell "0" storage node to trigger the feedback/latching mechanism to complete the write operation. For mixed TFET-MOSFET 8T cell, the write access transistor pull down the cell "1" storage node quickly due to the superior current drive of TFET at low voltage. However, owing to lack of push-pull action and the low current drive of pull-up PMOSFET, the pull-up of the opposite cell "0" storage node (second phase of the write operation) is impeded, thus degrading the cell time-to-write of the proposed cell. For MOSFET 8T cell, due to the low current drive of MOSFET devices at low voltage, both the initial phase and the second phase of the write operation are impeded, thus exhibiting severely degraded cell time-to-write at low supply voltage. The cell time-to-write can be improved by write-assist circuit techniques and will be discussed in Section V-A. For V_{DD} above 0.6 V, since the current drive of MOSFET device outperforms that of TFET device, MOSFET 8T cell offers better "cell" time-to-write among the three cells. As discussed in the previous section, when V_{DD} is higher than 0.6 V, the current drive of the holding PMOSFET overwhelms that of the write access TFET in mixed TFET-MOSFET 8T cell, hence write failure occurs. For the proposed cell, write-assist circuit techniques would be necessary to extend the operation to higher voltage and will be discussed in Section V-B.

A. Low Voltage Operation

1) Negative Bit-Line Write-Assist: The cell time-to-write at low supply voltage can be improved by write-assist circuit techniques such as: 1) collapsing cell V_{DD} [19], 2) raising cell V_{SS} [20], 3) boosting write WL [21], and 4) negative write bit-line voltage [22]. Among these write-assist techniques, collapsing cell V_{DD} and raising cell V_{SS} will result in degradation of stability of unselected cells on the selected column, while the boosting write WL will aggravate half-select disturb. In this work, we consider the NBL write-assist (Fig. 14) to improve the cell write performance of the MOSFET and mixed TFET-MOSFET 8T cell. The transient waveforms during write operation of the proposed mixed TFET-MOSFET 8T SRAM cell with and without NBL write-assist circuit are shown in Fig. 16. The comparison of the improvement in cell time-to-write between the proposed mixed TFET-MOSFET and MOSFET 8T cell with the NBL write-assist technique is shown in Fig. 15. The results indicate that the proposed mixed TFET-MOSFET 8T cell using NBL write-assist shows larger improvement compared with the MOSFET 8T cell with NBL write-assist for V_{DD} below 0.5 V. This is because TFET access transistor with increased overdrive voltage due to NBL exhibits larger drive current improvement in both the initial and second phase of write operation compared with the MOSFET access transistor. Moreover, with the uni-directional conduction of TFET driver transistor, the current charging up the bit-line would be smaller compared with the MOSFET driver transistor, thus facilitating the cell time-to-write further.

B. High Voltage Operation

It is pointed out that the proposed mixed TFET-MOSFET 8T SRAM cell faces write failure for V_{DD} above 0.6 V due to the reverse of current drive disparity between the TFET access transistor and PMOSFET holding transistor. In this part, we consider write-assist circuit techniques including transient voltage collapse write-assist [23], [24] and the data-aware write-assist scheme [25] to enhance the write-ability of the proposed mixed TFET-MOSFET cell.

1) Transient Voltage Collapse Write-Assist: The schematic of the transient voltage collapse write-assist circuit is shown in Fig. 17. Transient voltage collapse write-assist dynamically pulls down the selected column cell supply V_{CS} below the

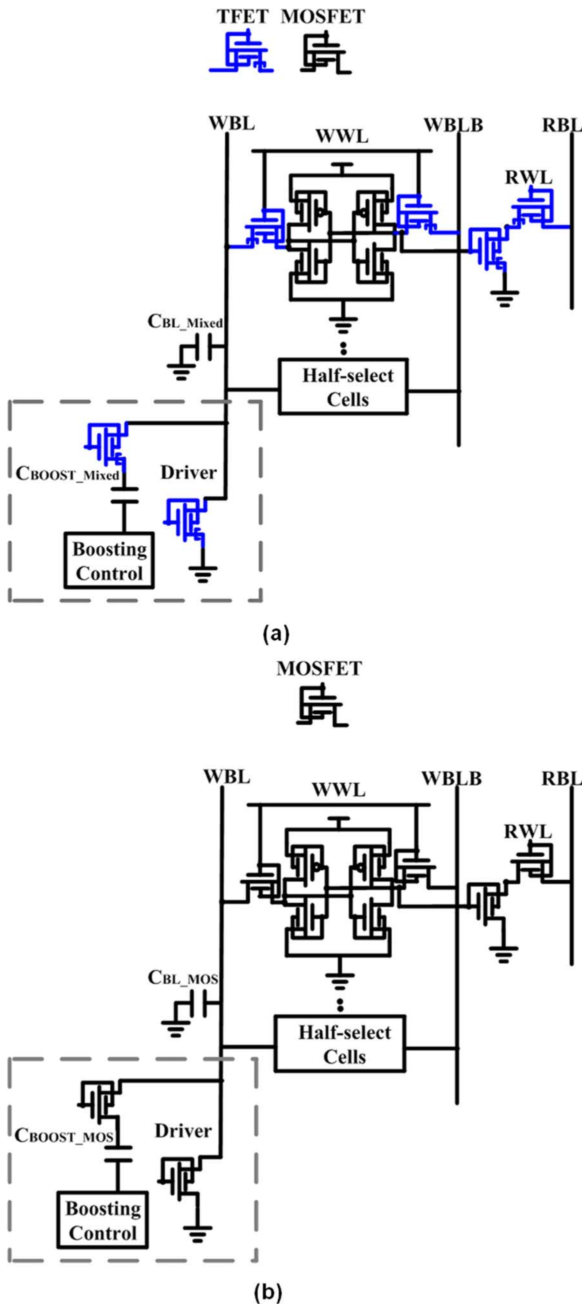

Fig. 14. Schematic of NBL write-assist for (a) the proposed mixed TFET-MOSFET 8T SRAM cell and (b) pure MOSFET 8T SRAM cell.

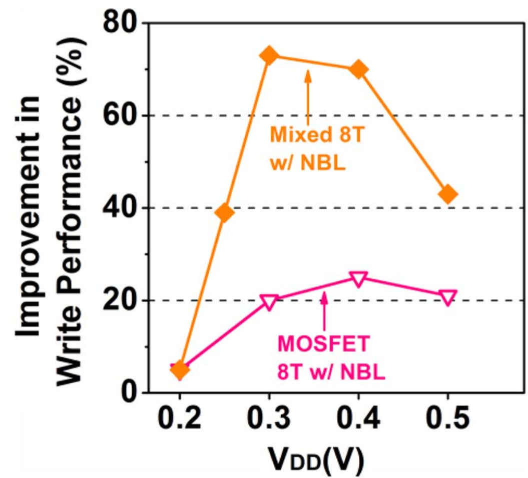

Fig. 15. Improvement in cell time-to-write of MOSFET and mixed TFET-MOSFET 8T cell with negative bit-line write-assist.

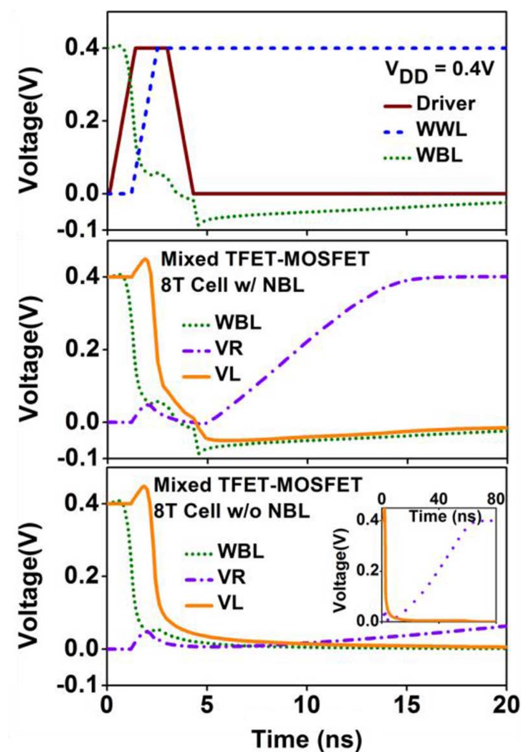

Fig. 16. Write transient waveforms of the proposed mixed TFET-MOSFET 8T SRAM cell with and without negative bit-line write-assist. Inset of the bottom figure shows the time when the write operation completes for the proposed mixed TFET-MOSFET 8T SRAM cell without negative bit-line write-assist.

data-retention voltage during write operation. The scheme offers fast cell supply collapse for effective write-assist. However, the TVC pulse width must be carefully controlled to ensure data retention of unselected cells in the selected column. The simulated transient waveforms during write operation at $V_{DD} = 0.6$ V are shown in Fig. 18. It is clearly seen that with the transient voltage collapse write-assist, the proposed mixed TFET-MOSFET 8T SRAM cell performs write successfully.

2) Data-Aware Write-Assist: The schematic of the data-aware write-assist circuit is shown in Fig. 19 where the virtual cell supply nodes V_{CSQ} and V_{CSQB} for the left- and right-half cells of a column are controlled by separate power-switch/keeper pairs. During write operation, the keepers are turned off, and the virtual cell supply node of the write "0" side (assuming V_{CSQ}) becomes floating due to the low-going WBL. The virtual cell supply node V_{CSQ} goes low due to write current and leakage of cells in the column, thus reducing V_{SG} of the holding PMOSFET and contention with the write access transistor. The pertinent transient waveforms during write are shown in Fig. 20. Compared with the transient voltage collapse write-assist in Fig. 19, the data-aware write-assist offers more significant write-ability and write performance improvement for the proposed mixed TFET-MOSFET 8T SRAM. This is because in the data-aware write-assist, the strength of pull-up

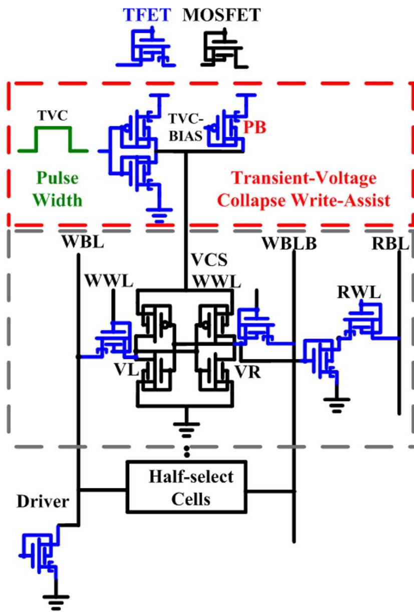

Fig. 17. Schematic of TVC write-assist scheme for the proposed mixed TFET-MOSFET 8T SRAM.

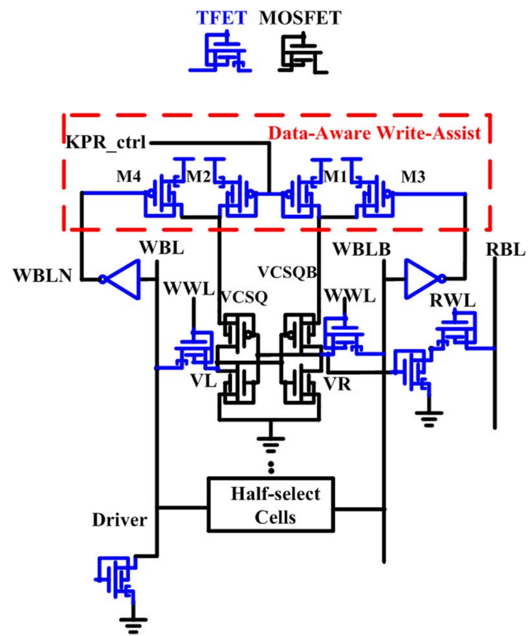

Fig. 19. Schematic of data-aware write-assist scheme for the proposed mixed TFET-MOSFET 8T SRAM.

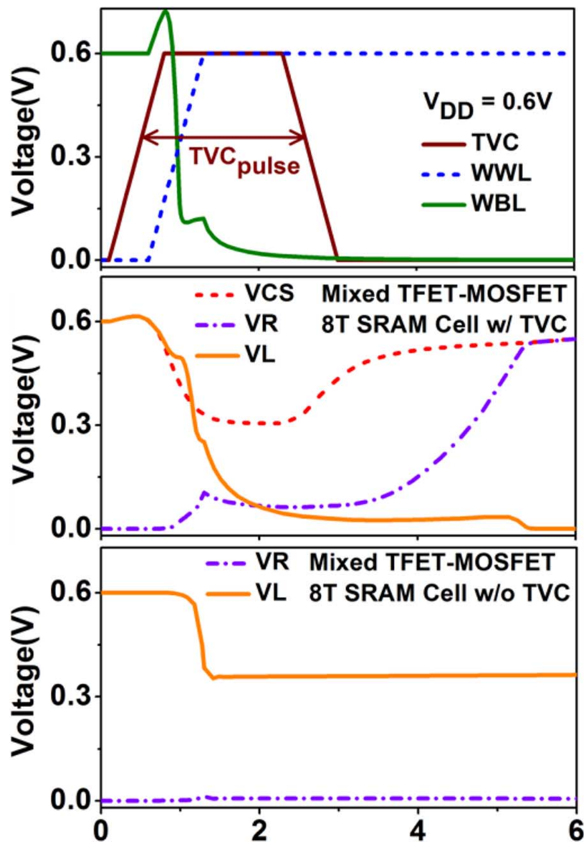

Fig. 18. Write transient waveforms of the proposed mixed TFET-MOSFET 8T SRAM cell with and without TVC write-assist.

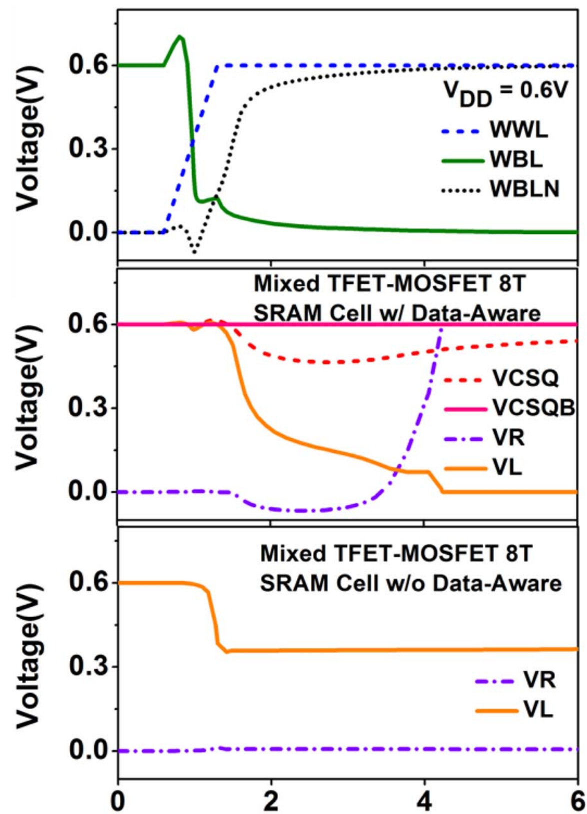

Fig. 20. Write transient waveforms of the proposed mixed TFET-MOSFET 8T SRAM cell with and without data-aware write-assist.

PMOSFET of the opposite half-cell and the latch feedback effect are not affected since V_{CSQB} for the opposite half cell remains at V_{DD}. On the other hand, in the transient voltage collapse write-assist, due to the lowering of the cell supply of the opposite half cell, the second phase of the write operation is retarded.

The cell time-to-write of the proposed mixed TFET-MOSFET 8T SRAM cell with transient voltage collapse write-assist and the data-aware write-assist are shown in Fig. 13(b) indicated by solid triangular and star symbol. With data-aware write-assist, the proposed mixed TFET-MOSFET 8T SRAM cell offers ∼40% improvement in cell time-to-write

compared with that using the transient voltage collapse write-assist at high supply voltages.

VI. Conclusion

We propose a mixed TFET-MOSFET 8T SRAM cell comprising MOSFET cross-coupled inverters, dedicated TFET read stack and TFET write access transistors suitable for ultra-low voltage operation. The use of MOSFET cross-coupled inverters improves hold static noise margin (SNM) over the pure TFET cell. The TFET read stack improves the "cell read access time" by 1.6x and 4000x at $V_{DD} = 0.5$ V and 0.2 V, respectively, compared with the MOSFET 8T cell due to the superior current drive and subthreshold slope of TFET at low supply voltages. The uni-directional TFET write access transistors eliminate the write half-select disturb to facilitate bit-interleaving architecture for improved soft error immunity with ECC compared with MOSFET 8T cell. The disparity in current drive between TFET write access transistor and MOSFET holding (pull-up) transistor greatly improves WSNM for supply voltage below 0.5 V. The proposed cell improves the cell hold/read stability, write stability, read performance, and eliminate half-select disturb for ultra low voltage operations. The layout and performance of the MOSFET, TFET, and proposed mixed TFET-MOSFET 8T cell are comparatively assessed. With negative bit-line write-assist, the cell time-to-write is significantly enhanced compared with the MOSFET 8T cell using NBL write-assist at low supply voltages. To operate at higher supply voltage for V_{DD} above 0.6 V, the proposed mixed TFET-MOSFET 8T cell adopting the transient voltage collapse write-assist or data-aware write-assist shows adequate write-ability. Among these SRAM cells, MOSFET 8T cell offers better cell stability and performance at higher supply voltage for V_{DD} above 0.6 V. With superior stability and read performance, the proposed mixed TFET-MOSFET cell provides merits for ultra-low voltage operation.

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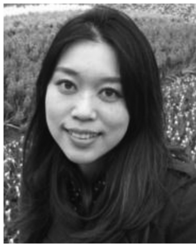

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