Active Guard Ring to Improve Latch-Up Immunity

Hui-Wen Tsai, *Student Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*— A new design concept named as active guard ring and related circuit implementation to improve the latch-up immunity of ICs are proposed. Using additional sensing circuit and active buffer to turn ON the electrostatic discharge (ESD) protection transistors, the large-dimensional ESD (or I/O) devices can provide or receive extra compensation current to the negative or positive current perturbation during the latch-up current test. The new proposed solution has been verified in 0.6-μm 5 V process to have much higher latch-up resistance compared with the conventional prevention method of guard ring in CMOS technology.**

***Index Terms*— Electrostatic discharge (ESD) protection, guard ring, latchup.**

I. Introduction

PARASITIC p-n-p-n paths are inherently existing in CMOS chips. It is needed to be aware of related short-circuit failure identified as latchup for IC designers in both development and layout stages. Such failure mechanism brings about huge abnormal current from VDD supply to ground if the unexpected conduction through the parasitic p-n-p-n structure is generated after voltage/current fluctuation is triggered at input/output (I/O) metal bonding pads (PADs). Damages or reliability problem are also caused if the abnormal current is over the limited value that metal lines or contacts can sustain or the parasitic p-n-p-n structure can afford [1], [2].

To examine the latch-up immunity, methods with positive and negative current tests (I-tests) had been defined in Joint Electron Device Engineering Council (JEDEC) standards [3]. Table I is the characterization of the force current for latch-up I-test specified in the up-to-date JEDEC standard. According to the newest standard, the highest latch-up level with I-test has been updated to be greater than 200 mA. Therefore, many companies promote their IC products with over 200-mA I-test as the target specification against latchup. To increase the latch-up immunity of CMOS chips, prevention with guard rings has been developed and implemented in the IC products. The related models on latch-up prevention with guard rings had been also studied in [4] and [5].

A depiction for the traditional latch-up prevention with guard rings in a typical CMOS IC is shown in Fig. 1. There is a parasitic p-n-p-n path (latch-up path) formed from the VDD-connected source (P+ diffusion) of p-type MOS (pMOS) to the VSS-connected source (N+ diffusion) of n-type MOS (nMOS) in the logic gates of internal circuits. Under the trigger of external current source, there is substrate current flew in or out of the internal circuits corresponding to positive or negative pulse applied at I/O PAD. Such substrate current is the main activator for the occurrence of latchup. With the guard ring surrounding the I/O buffer or electrostatic discharge (ESD) protection transistors, certain amount of the latch-up trigger current can be absorbed or released without causing latch-up occurrence at the internal circuits. Nevertheless, the tolerance toward the trigger current is related to the width of guard ring and the distance to the internal latch-up paths. To further enhance the tolerance for latch-up trigger current, methods with extra guard rings [6]–[8], isolating layers [9]–[11], or trench structure [12], [13] had been also proposed. Even if high latch-up immunity can be achieved by carefully implementing with special designs, saving the

TABLE I
TRIGGER CHARACTERIZATION IN LATCH-UP I-TEST [3]

Latchup I-test	Range of Stress	Force Current
Positive I-test	I	< 50 mA
	II	50 mA to < 100 mA
	III	100 to 150 mA
	IV	150 to 200 mA
	V	>= 200 mA
Negative I-test	I	> -50 mA
	II	-50 mA to > -100 mA
	III	-100 mA to > -150 mA
	IV	-150 mA to >-200 mA
	V	<= -200 mA

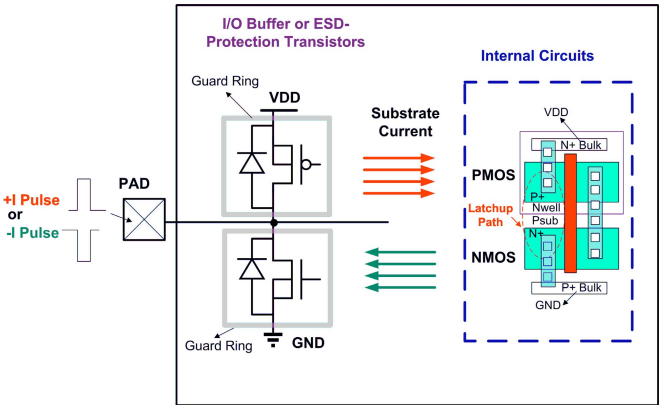


Fig. 1. Traditional latch-up prevention in CMOS IC with guard rings to surround the I/O and ESD protection transistors.

Manuscript received June 20, 2014; revised September 13, 2014; accepted October 7, 2014. Date of publication October 28, 2014; date of current version December 9, 2014. This work was supported by the Ministry of Science and Technology, Taiwan, under Contract 102-3113-P-110-010, Contract 103-2622-E-009-006, and Contract 103-2221-E-009-197-MY2. The review of this paper was arranged by Editor F. Udrea.

The authors are with the Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: miyu.ee98g@nctu.edu.tw; mdker@ieee.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2014.2363171

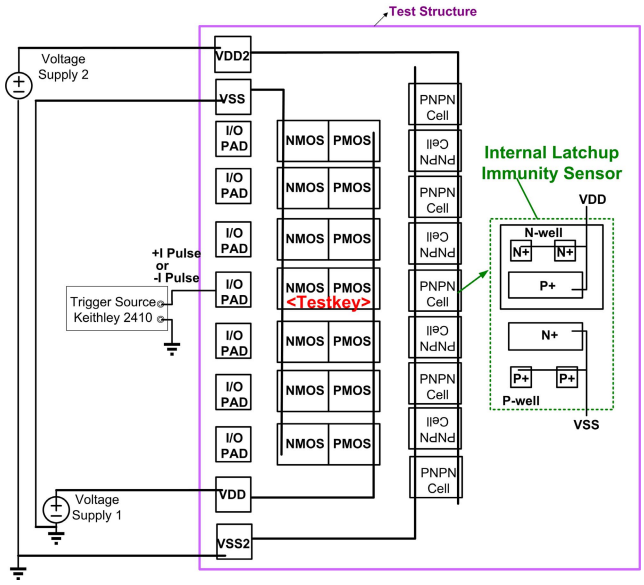


Fig. 2. Test structure to investigate the performance of latch-up prevention.

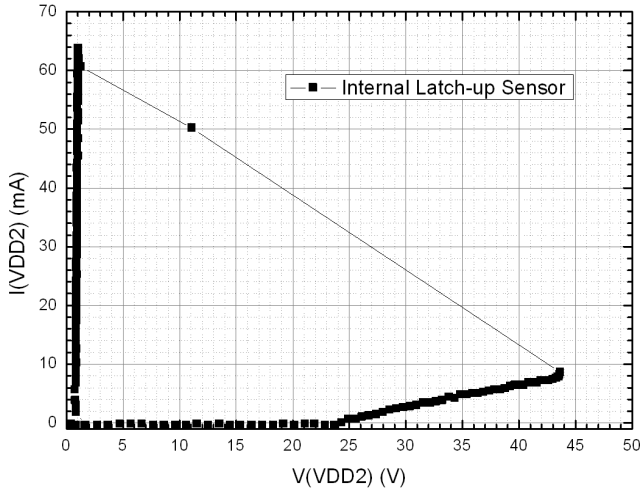


Fig. 3. Measured I–V curve of the internal sensor to show the latch-up characteristics, which has a holding voltage of 1.1 V.

fabrication cost without using extra layers or reducing the width of guard rings is still requested by IC industry.

In this paper, an active structure with existing ESD devices to increase the resistance against latchup is proposed and named as active guard ring. The ESD-protection nMOS and pMOS transistors work not only during ESD stress but also at the latch-up trigger conditions by the help of circuit technique. The concept of active guard ring and the novel circuit implementation has been proposed and successfully verified in silicon chip.

II. Test Structure and the Latch-Up Immunity of Traditional Design With Guard Ring

Fig. 2 shows the brief depiction of the test structure and the related setup with external equipments [7], [14]. For the test structure, it contains the testkeys and the p-n-p-n cells. The testkeys are composed of large-dimensional nMOS and pMOS with guard ring surrounding. The internal p-n-p-n cells work as latch-up immunity sensors to investigate the performance of

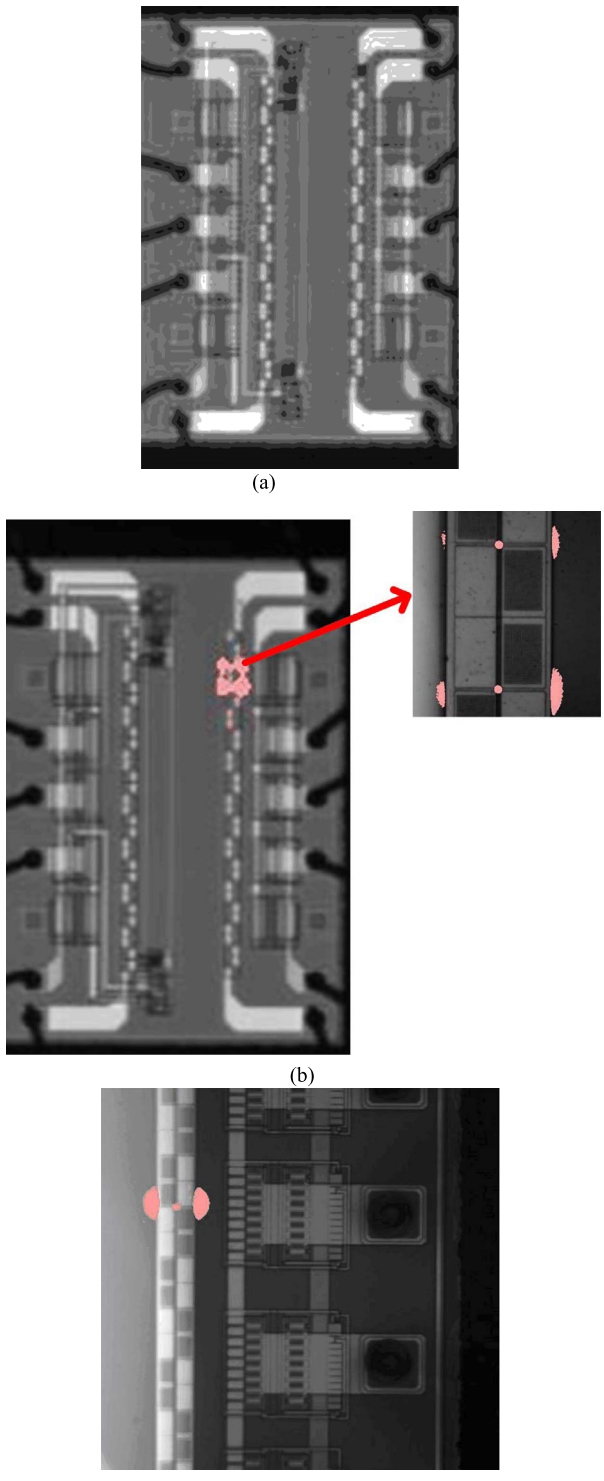


Fig. 4. (a) Chip photo of the latch-up test structure. (b) EMMI (Emission Microscope) picture on the damaged chip after 5-mA positive current pulse was applied. (c) EMMI picture on the damaged chip after 270-mA negative current pulse was applied.

the designed testkeys. The latch-up sensitivity of the internal p-n-p-n cells toward the external trigger source is affected by the structure of the testkeys as well as by the distance between the testkeys and the p-n-p-n cells. The I–V curve of the internal latch-up sensors are measured by the curve tracer (Tek 370B) from the VDD2 and VSS2 pads. The measured result is shown in Fig. 3. Since the holding voltage is near

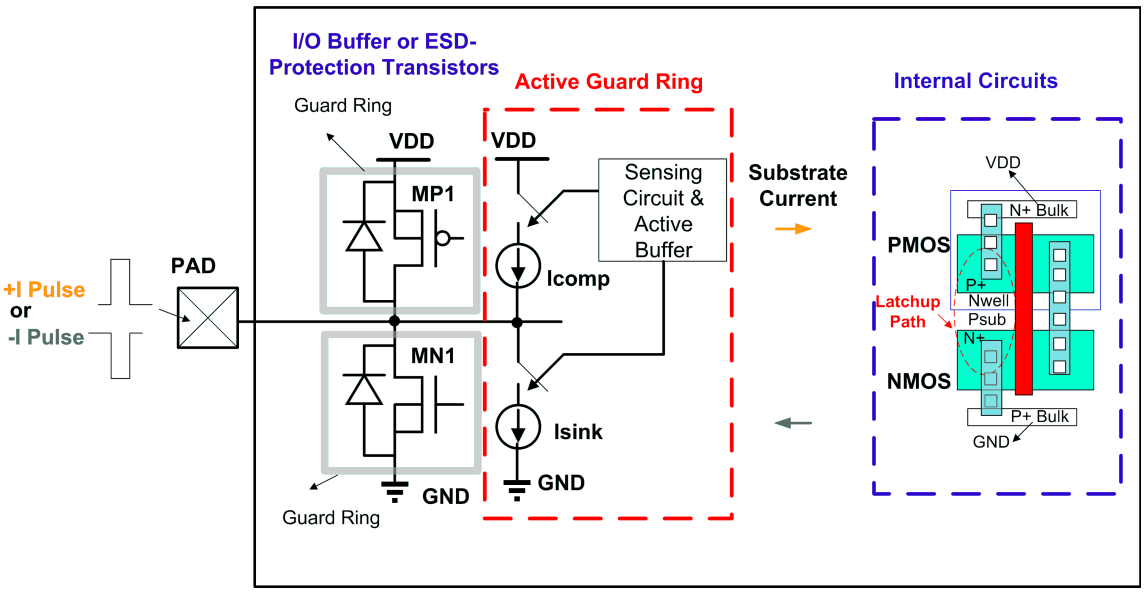


Fig. 5. Concept of active guard ring to reduce the injected substrate current at the latch-up path of internal circuits during latch-up I-tests.

1.1 V, large current is generated when latchup happens under 5 V power supply. Thus, the occurrence of latchup can be observed by monitoring the current or voltage condition at VDD2.

Some test chips had been fabricated in a 0.6-μm 5 V CMOS process to investigate the performance of the previous work with guard ring [7]. To examine the performance of the test chips, the I/O PAD of testkey under test is applied with trigger current pulse of $\sim$150 ms provided by Keithley 2410. In addition, the supply voltage (VDD) of the testkeys is given to 5 V and the supply voltage (VDD2) of the p-n-p-n cells is also connected to 5 V voltage source at room temperature, respectively. Emission Microscope (EMMI) analysis is taken, after the current pulse is applied to the I/O PAD to investigate the latch-up immunity level, to show the location of the abnormal current. Fig. 4(a)–(c) shows the EMMI pictures after positive or negative trigger current is applied to the I/O PAD. The normal chip photo without any hot spot, which also means no abnormal current, is shown in Fig. 4(a) after 4-mA positive current or 250-mA negative trigger current pulse was applied. The EMMI pictures for the damaged chip after experienced 5-mA current pulse or 270-mA negative current pulse are shown in Fig. 4(b) and (c), respectively. From the hot spots in Fig. 4(b) or (c), the abnormal current is attributed to the p-n-p-n path of the latch-up sensor. With the observed results, the traditional work with guard ring has weaker performance in the positive I-test. The tolerance level of the fabricated previous design is even less than 50 mA, which is clarified as the lowest level specified in the JEDEC standard [3].

III. Latch-Up Prevention by Active Guard Ring

A. Concept and Circuit Implementation

Fig. 5 shows the concept denominated as active guard ring proposed in this paper to reduce the injected current that triggers latchup at the internal circuits when latch-up I-test is applied at the I/O PAD. In addition to the traditional prevention method with guard ring to surround the I/O buffer and ESD-protection transistors at the I/O PAD, the proposed active guard ring design with the adopted circuits actively provides extra sink or compensation currents (Isink and Icomp) corresponding to positive or negative I-test, respectively. The structure for active guard ring is composed of a sensing circuit block and an active buffer. To generate sufficient sink or compensation current without paying the cost of extra silicon area, the existing large-dimensional ESD-protection nMOS and pMOS transistors are also adopted as major supporters to the mentioned sink or compensation current. The sensing circuit block is used to monitor whether the positive or negative current pulse is applied. Once the positive or negative trigger current is large enough, the sensing circuit will inform the active buffer about the strength of the applied current perturbation at PAD. The active buffer will then control the gate voltages of the large- dimensional ESD devices to generate the corresponding sink or compensation current.

The circuit implementation to realize the concept of active guard ring is presented in Fig. 6(a) and (b). In Fig. 6(a), the main embodiment includes the ESD devices (MP1 and MN1), a sensing circuit block, and an active buffer. The sensing circuit block is composed of MPS1, MNS1, RSN, and RSP to detect the information of the trigger current pulse. In addition, the MPS2, MN6, and MN7 are included in the block to mirror the detection results to the active buffer. The active buffer contains driving stages for MP1 and MN1, respectively. To control the gate voltage of MP1 (Vg_mp1), devices as MP2, MP3, MN2, and MN3 are adopted, as shown in Fig. 6(a). For the gate driver of MN1, it is made of MP4, MP5, MN4, and MN5.

For normal circuit operation without the external latch-up trigger source, the induced current by sensing circuit block is quite small to let MN2/MP4 has much weaker sink/source force compared with the designed reference source/sink force

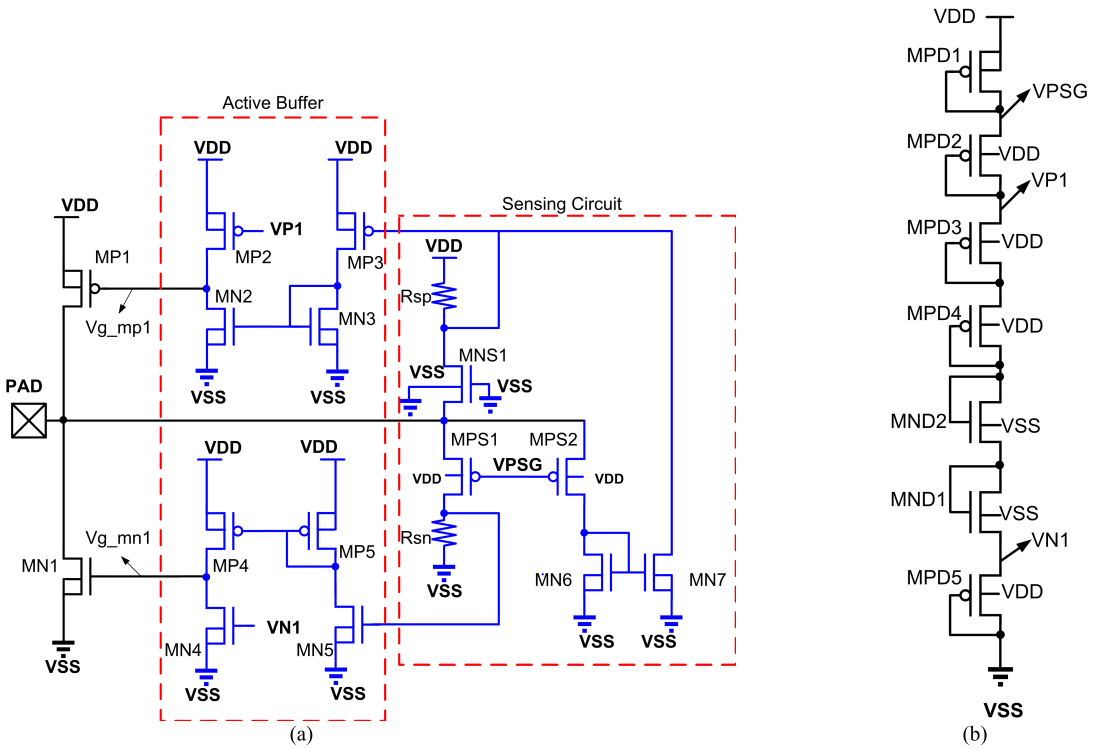


Fig. 6. (a) Circuit structure to implement the concept of active guard ring. (b) Diode-connected MOS string to generate the required voltage biases for VP1, VN1, and VPSG.

provided by MP2/MN4. Therefore, the gate voltage of MP1 (Vg_mp1) or MN1 (Vg_mn1) is pulled to high/low to OFF the MP1/MN1.

The reference current force at MP2/MN4 can be generated by connecting VP1/VN1 to a traditional bias current circuit if it exists in the internal circuits. However, instead of the need for a traditional bias current circuit, a series of diode-connected MOS transistors shown in Fig. 6(b), which is composed of MPD1 to MPD5 and MND1 to MND2, can provide the required voltages for VP1, VN1, and VPSG. Since the absolute threshold voltage of the designed pMOS MPD5 is much higher than the threshold voltage of nMOS MN1, even few quiescent currents in MPD5 can generate sufficient reference current force in MN4. With the device sizes used in the simulation, as described in Section III-B, the absolute threshold voltage for MPD5 ($|Vthp|$) is 0.964 V compared with 0.775 V for MN4 (Vthn). In addition, the summation of the threshold voltages of MPD1 and MPD2 is higher than MP2 so that small current in the diode-connected string makes enough reference current force in MP2. Moreover, the gate terminal of MPS1 (VPSG) is connected to the drain terminal of MPD1 to have a voltage slightly smaller than supply voltage VDD for quickly acting after the external trigger currents are applied. The number of stacked diode-connected MOS transistors is decided by the concern to have small quiescent standby current within the total quiescent current budget.

The detailed operations for the proposed active guard ring during positive and negative I-test are shown in Fig. 7(a) and (b), respectively. In Fig. 7(a), when sufficient positive current pulse is applied, the voltage at the PAD is raised up with the value over VDD. In such condition, there is current flow from the drain terminal to the bulk terminal of the MP1 (Idb_p), which is a normal path in traditional design. However, since the VPSG is slightly smaller than VDD, the source-to-gate voltages of MPS1 and MPS2 are also large enough to generate corresponding channel currents when PAD voltage is enough larger than VDD. The gate voltages of transistor MN5 and MP3 are thus pulled high and low, respectively. The current mirror, MN3 and MN2, then mirrors the current of MP3 to compare with the current sourced from transistor MP2. Once the mirrored current is larger, the gate voltage of MP1 (Vg_mp1) is pulled low to turn ON transistor MP1. Thus, the related source-to-drain current (Isd_mp1) is generated. Similarly, with the assistants of MP5 and MP4, there is also a mirrored current from MN5 to be compared with the drain current of MP4.

While the mirrored current is larger, the gate voltage ofMN1(Vg_mn1) is pulled high. Therefore, the transistor MN1 is turned ON and produces the related drain-to-source current (Ids_mn1). Due to the generation of Isd_mp1 and Ids_mn1, the amount of the drain-to-bulk current of MP1 (Idb_mp1) and the substrate current injected to the internal circuits is reduced, and thus improves the latch-up immunity against the positive I-test.

When sufficient negative current pulse is applied as shown in Fig. 7(b), the PAD voltage is pulled down to lower than Vss and induces certain current at drain terminal of MNS1. The related voltage difference across the resistor Rsp is thus pulled down the gate voltage of MP3 to generate the corresponding channel currents in transistor MP3 and MN3. The transistor MN3 then mirrors a current to transistor MN2. If the current

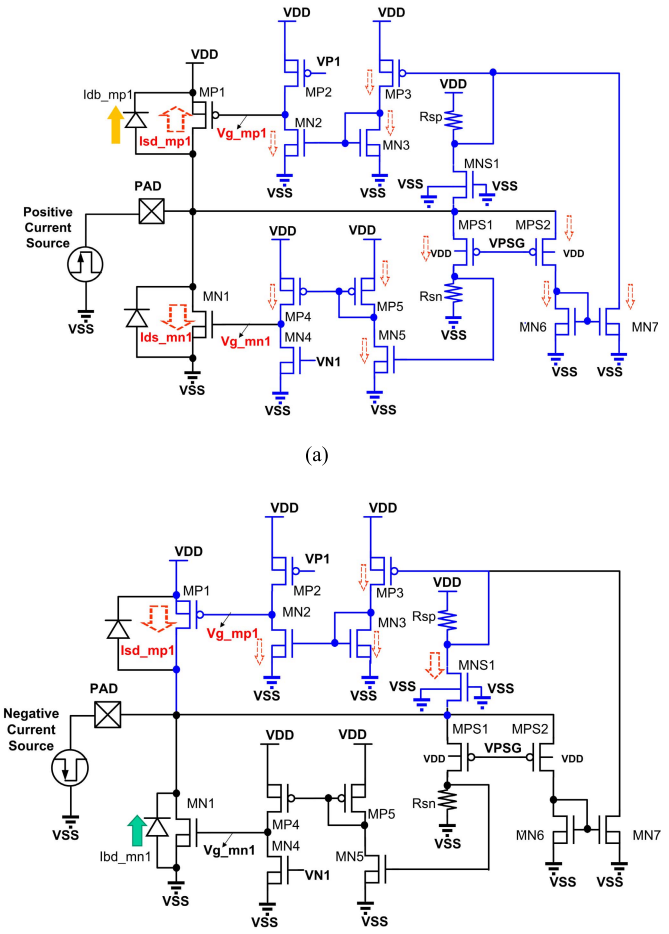


Fig. 7. Operations of the proposed work during (a) positive and (b) negative I-test.

flew in MN2 is larger than the current flew from MP2, Vg_mp1 is pulled low to turn ON the transistor MP1. Certain amount of current is generated and depicted as Isd_mp1 to compensate the negative I-test current at the PAD. Thus, the bulk-to-drain current of MN1 (Ibd_mn1) and the substrate current injected to the internal circuits are reduced. Since the latch-up immunity under negative I-test is intrinsically higher as presented in Section II, simpler structure to only turn ON transistor MP1 is enough.

The proposed work can be codesigned with the power-rail ESD clamp circuit [15] to achieve the whole-chip ESD protection. Once the ESD stress is applied under the positive-to-VSS (PS) [negative-to-VDD (ND)] modes, the parasitic drain-to-bulk diode or the channel of MP1 (MN1) can conduct the ESD current to the floating VDD (VSS) line and then to the grounded VSS (VDD) through the power-rail ESD clamp circuit. Thus, even adopted with the active guard ring structure, the ESD performance is not degraded with the help of the power-rail ESD clamp circuit.

B. Simulation

The simulated results in a given 0.6-μm 5 V CMOS process on the proposed active guard ring are done by doing a dc sweep at the PAD voltage from -1 to 6 V under room temperature. The device dimensions of the used transistors and resistors to verify this paper are listed in Tables II and III. The simulated waveforms for Vg_mp1, Vg_mn1, Isd_mp1, and Ids_mn1 are presented in Fig. 8. Since the Vg_mp1 is pulled low and the Vg_mn1 is pulled high while the PAD voltage is above 5.73 V, transistor mp1 and mn1 are verified to be turned ON. The mentioned sink currents are generated as Isd_mp1 of 65 mA and Ids_mn1 of 200 mA under the PAD voltage of 5.73 V, respectively. When the positive trigger current is applied to pull the PAD voltage high enough, those sink currents will help to hold back the increase of PAD voltage. Thus, less substrate injected current flows to the internal circuits.

When the PAD voltage pulls low to beneath -0.63 V, Isd_mp1 of 194 mA is induced, as shown in Fig. 8. The compensation current increases the PAD voltage against the increase of negative I-test current. The simulated curve of the current from supply voltage I(VDD) according to

TABLE II
DEVICE DIMENSIONS OF THE TRANSISTORS USED IN THE SILICON VERIFICATION

Circuit Block	Device	(Width*M)/Length
ESD Devices	MP1	(45 μm*18)/0.6 μm
	MN1	(30 μm*18)/0.6 μm
Active Buffer	MP2, MP3	(1.3 μm*1)/0.6 μm
	MN2, MN3	(1.3 μm*2)/0.6 μm
	MP4, MP5	(1.3 μm*3)/0.6 μm
	MN4, MN5	(1.3 μm*1)/0.6 μm
Sensing Circuit	MNS1	(30 μm*2)/1 μm
	MPS1, MPS2	(45 μm*2)/1 μm
	MN6	(5 μm*1)/5 μm
	MN7	(5 μm*1)/0.6 μm
Diode String	MPD1, MPD3	(1.6 μm*3)/1 μm
	MPD2, MPD4, MND1, MND2	(1.6 μm*1)/1 μm
	MPD5	(2 μm*2)/1 μm

TABLE III
RESISTORS USED IN THE SILICON VERIFICATION

Resistor in the Sensing Circuit	Resistance
Rsp	100 kohm
Rsn	100 kohm

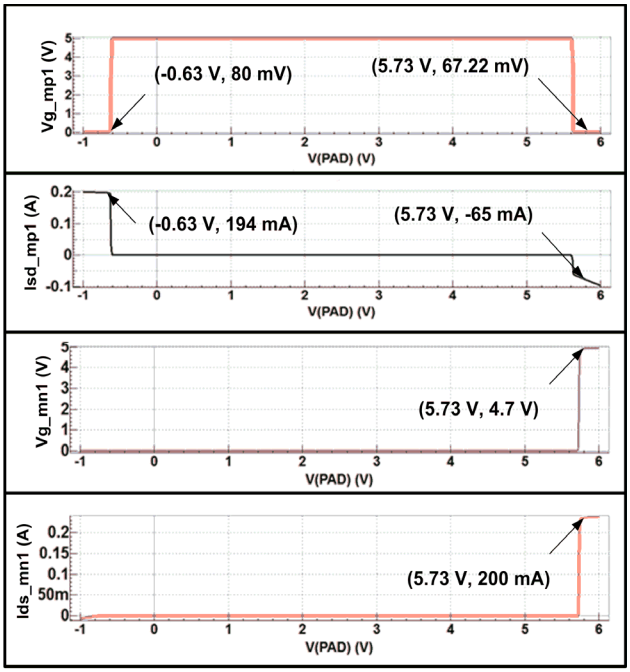


Fig. 8. Simulated waveforms of certain voltages and currents in this paper with dc sweep at the PAD voltage from −1 V to 6 V.

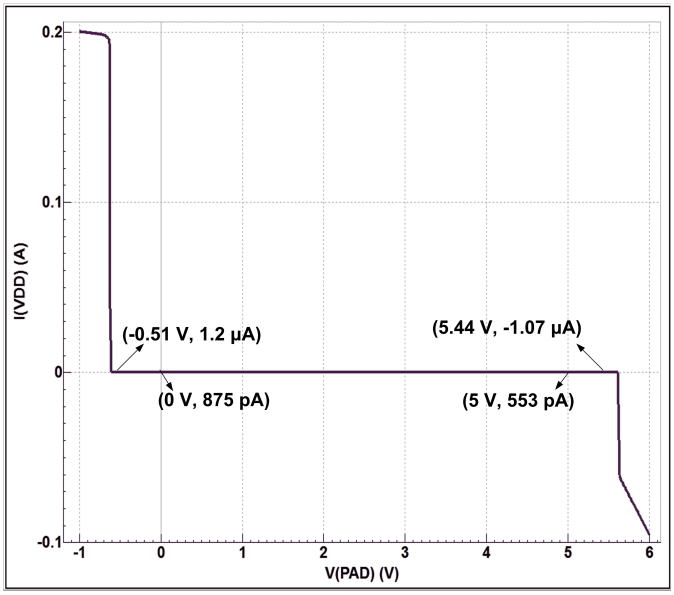


Fig. 9. Simulated waveforms for the current I(VDD) from supply voltage according to the variation of PAD voltage.

the variation of the PAD voltage is also shown in Fig. 9. From the result of Fig. 9, the current of supply voltage I(VDD) is below 1 nA with PAD voltage ranging from 0 to 5 V. Moreover, I(VDD) is less than −1.07 and 1.2 μA for PAD voltages ranging from 5 to 5.44 V and 0 to −0.51 V, respectively.

More detailed simulated supply currents I(VDD) under the different temperatures and PAD voltages for the design without or with the proposed active guard ring are summarized in Table IV. From the results of Table IV, the proposed design that is able to effectively enhance the latch-up immunity has been verified to only consume little quiescent standby current.

TABLE IV
SIMULATED RESULTS OF SUPPLY CURRENT I(VDD) AT DIFFERENT TEMPERATURES FOR THE WORK WITH AND WITHOUT THE PROPOSED ACTIVE GUARD RING PROTECTION

The design without the proposed active guard ring (only NMOS MN1 and PMOS MP1, kept in off state)				
I(VDD)	-20 °C	25 °C	85 °C	125 °C
V(PAD)=0V	362.3 pA	364.3 pA	481.7 pA	8.7 nA
V(PAD)=5V	176.7 pA	178.8 pA	183.2 pA	658.1 pA

The design with the proposed active guard ring				
I(VDD)	-20 °C	25 °C	85 °C	125 °C
V(PAD)=0V	660.8 pA	874.3 pA	1 nA	25 nA
V(PAD)=5V	526 pA	553.4 pA	1.5 nA	15.4 nA

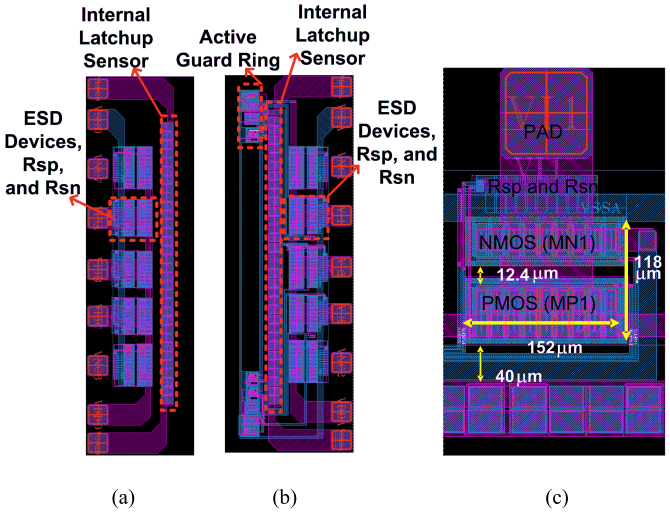


Fig. 10. Layout top view of the (a) testkeys with only single guard ring, (b) testkeys with proposed active guard ring, and (c) enlarged graph for the ESD devices and related resistors (Rsp and Rsn) of the testkey.

IV. EXPERIMENTAL RESULTS

The test chip to verify the proposed design with active guard ring and the related test structure has been fabricated in a 0.6-μm 5 V CMOS process. The layout top view of the test chip for the testkeys with only guard ring, the testkeys with active guard ring, and the enlarged graph for the ESD devices and resistors (Rsp and Rsn) is shown in Fig. 10(a)–(c), respectively. The dimensions of the ESD devices in the new proposed work in Fig. 10(b) are the same as that of the previous work in (a) with 152 μm×118 μm area consumption. The distances of the oxide diffusion (OD) junctions between the bulk terminals of MP1 and MN1 is 12.4 μm. The enlarged layout graphs for the single p-n-p-n

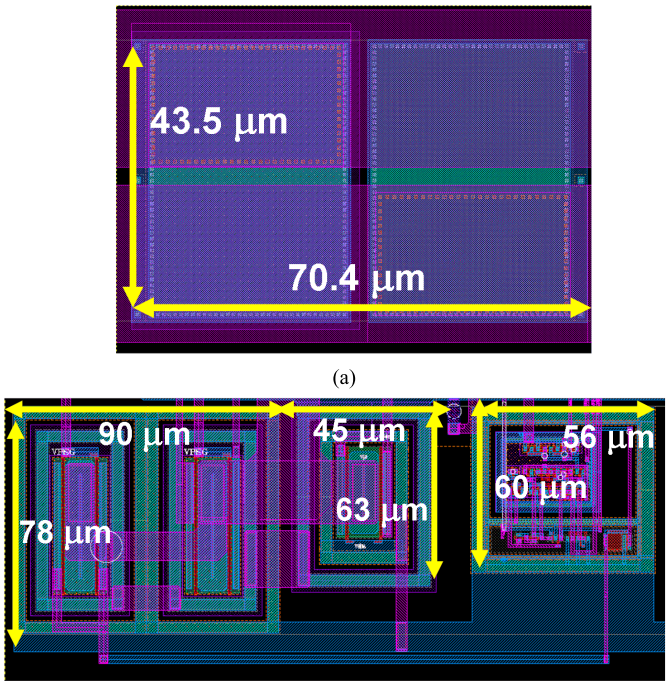


Fig. 11. Enlarged layout graph for (a) single p-n-p-n cell and (b) active guard ring.

cell to detect latch-up occurrence and the circuit to realize the active guard ring are shown in Fig. 11(a) and (b). The area draught for one p-n-p-n cell is about 70.4 μm $\times$ 43.5 μm and 0.0132 mm^2 (90 μm $\times$ 78 μm + 45 μm $\times$ 63 μm + 56 μm $\times$ 60 μm) for the implemented active guard ring. Though some additional area is required in this paper, the placement can be flexible and can be merged with other internal circuits together. Since there is no need to put the active guard ring beside the PAD, it is also able to arrange the extra area brought by additional circuits to the dummy or redundant layout area. Thus, the required area near the PAD can be similar to the traditional design for the PAD-limited application.

The measurement setup is similar as that shown in Fig. 2 with 5 V supply at VDD and an external current source applied to the PAD. However, the VDD2 is connected in series with a 100-Ω resistor to the 5 V voltage source instead of directly connected the PAD to the voltage source. The occurrence of latchup can be easily caught by observing the voltage change of VDD2 due to the large abnormal current induced by latchup. The measured waveforms under the positive I-test to the test chip with 250 and 280-mA trigger currents are shown in Fig. 12(a) and (b), respectively. The voltage of VDD2 is captured as CH1 and the trigger current applied at PAD is recorded as CH4 in the figure. If the trigger current is not over the tolerance of the testkey, the voltage at VDD2 is kept at 5 V, as shown in Fig. 12(a). While latchup is triggered at the p-n-p-n cells, the voltage at VDD2 is dropped to ~1 V, as shown in Fig. 12(b). Thus, the proposed work is verified to pass the 250-mA but not 280-mA positive I-test from the experimented results. Under the negative I-test, the measured waveforms of the

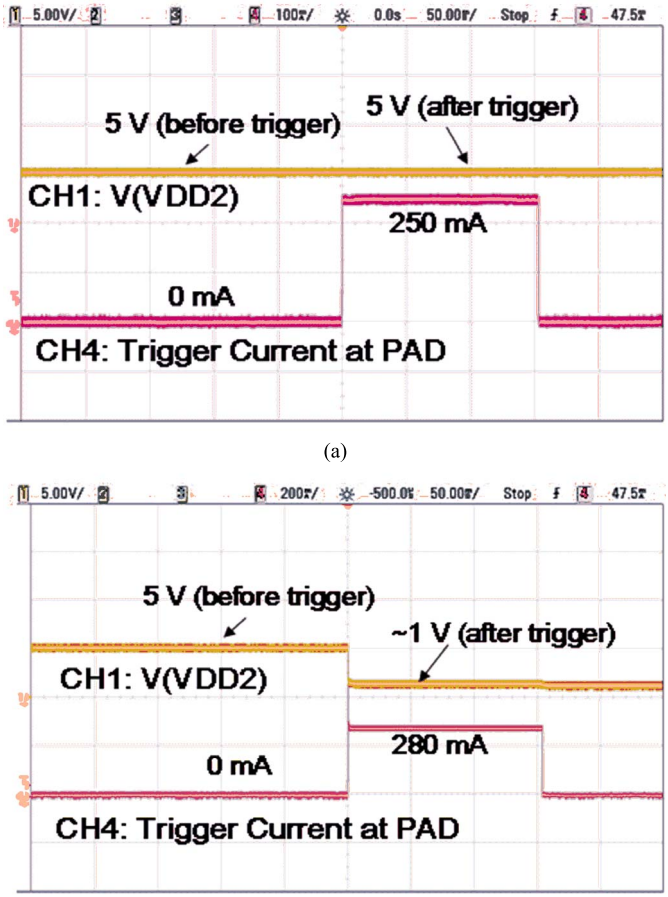
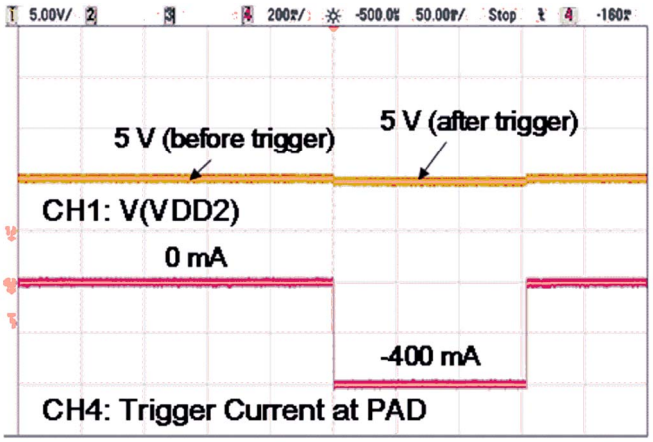
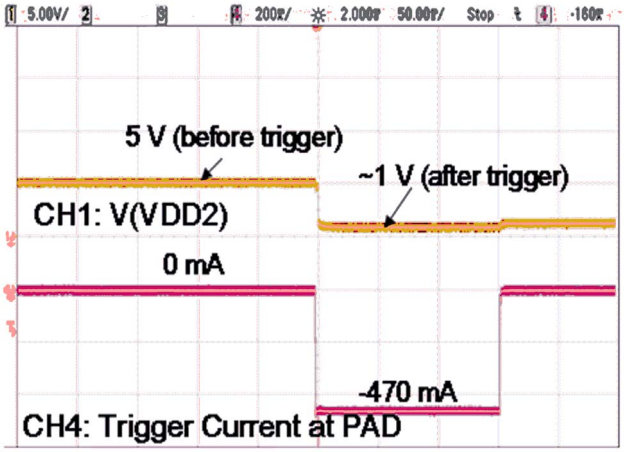


Fig. 12. Measured waveforms of proposed design with active guard ring under positive I-test with (a) 250-mA and (b) 280-mA trigger currents applied at the input PAD.

proposed design are shown in Fig. 13(a) and (b) under −400 and −470-mA trigger currents, respectively. Since the VDD2 is kept at 5 V in Fig. 13(a), no latchup occurrence at the p-n-p-n cells when the negative I-test current of −400 mA is applied. While the VDD2 is dropped to ~1 V after the negative trigger current of −470 mA is applied in Fig. 13(b), the waveforms show that the proposed design has −400-mA latch-up immunity but is failed in the −470-mA I-test. Moreover, more detailed examinations to investigate the latch-up immunity are done by the latch-up tester with 10-ms pulse width and follow the JEDEC standards. The latchup test results for the testkeys with the traditional prevention of guard ring and the new proposed design of active guard ring are listed in Table V. The tolerance in positive I-test for the proposed design is 260 mA that is much higher than the 5-mA performance of the traditional design. In addition, the immunity in the negative I-test of the work with active guard ring is also increased to −430 mA compared with −190 mA for the traditional prevention with guard ring. From the experiment results, the proposed work of active guard ring has been verified to reach the highest level (200 mA for positive I-test and −200 mA for negative I-test) defined in JEDEC standards, which is helpful for IC products with qualified latch-up prevention.



(a)



(b)

Fig. 13. Measured waveforms of proposed design with active guard ring under negative I-test with (a) 400-mA and (b) 470-mA trigger currents applied at the input PAD.

TABLE V
LATCH-UP TEST RESULTS

Latchup I-test	Test Cell with the Traditional Guard Ring		Test Cell with the Proposed Active Guard Ring	
	Pass	Fail	Pass	Fail
Positive I-test	5 mA	10 mA	260 mA	270 mA
Negative I-test	-190 mA	-200 mA	-430 mA	-440 mA

V. CONCLUSION

The proposed design of active guard ring concept and the practical circuit implementation has been fabricated and successfully verified in a 0.6-μm 5 V CMOS process. The additional sensing and active buffers are developed to activate the existing ESD devices while the external trigger current is applied under the latch-up I-test. From the silicon verification, the testkey with the proposed design can achieve 260 and −430-mA immunities for positive and negative I-tests, respectively. The proposed active guard ring can significantly enhance the latch-up immunity of CMOS ICs with the cost of very small quiescent standby current during the normal circuit operation.

ACKNOWLEDGMENT

The authors would like to thank Leadtrend Technology Corporation for the support with chip fabrication and latch-up test.

REFERENCES

[1] S. H. Voldman, *Latchup*. New York, NY, USA: Wiley, 2007.
[2] M.-D. Ker and S.-F. Hsu, *Transient-Induced Latchup in CMOS Integrated Circuits*. New York, NY, USA: Wiley, 2009.
[3] *IC Latch-Up Test*, JEDEC Solid State Technology Association, JEDEC Standard JESD78D, 2011.
[4] F. Farbiz and E. Rosenbaum, "Modeling and understanding of external latchup in CMOS technologies—Part I: Modeling latch-up trigger current," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 3, pp. 417–425, Sep. 2011.
[5] F. Farbiz and E. Rosenbaum, "Modeling and understanding of external latchup in CMOS technologies—Part II: Minority carrier collection efficiency," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 3, pp. 426–432, Sep. 2011.
[6] T.-L. Hsu, Y.-C. Chen, H.-C. Tseng, V. Liang, and J.-S. Jan, "psub guard ring design and modeling for the purpose of substrate noise isolation in the SOC era," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 693–695, Sep. 2005.
[7] M.-D. Ker and W.-Y. Lo, "Methodology on extracting compact layout rules for latchup prevention in deep-submicron bulk CMOS technology," *IEEE Trans. Semicond. Manuf.*, vol. 16, no. 2, pp. 319–334, May 2003.
[8] M. A. Halfacre, D. S. Pan, and W. K. Huie, "N- well CMOS process on a P substrate with double field guard rings and a PMOS buried channel," U.S. Patent 4 574 467, Mar. 11, 1986.
[9] T. Aoki, "A practical high-latchup immunity design methodology for internal circuits in the standard cell-based CMOS/BiCMOS LSIs," *IEEE Trans. Electron Devices*, vol. 40, no. 8, pp. 1432–1436, Aug. 1993.
[10] S.-F. Hsu and M.-D. Ker, "Dependence of device structures on latchup immunity in a high-voltage 40-V CMOS process with drain-extended MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 840–851, Apr. 2007.
[11] M. Pfost, P. Brenner, T. Huttner, and A. Romanyuk, "An experimental study on substrate coupling in bipolar/BiCMOS technologies," *IEEE J. Solid-State Circuits*, vol. 39, no. 10, pp. 1755–1763, Oct. 2004.
[12] S. Voldman *et al.*, "The influence of a silicon dioxide-filled trench isolation structure and implanted sub-collector on latchup robustness," in *Proc. 43rd Annu. IEEE IRPS*, Apr. 2005, pp. 112–120.
[13] S. H. Voldman, "The influence of a novel contacted polysilicon-filled deep trench (DT) biased structure and its voltage bias state on CMOS latchup," in *Proc. 44th Annu. IEEE IRPS*, Mar. 2006, pp. 151–158.
[14] J. Quincke, "Novel test structures for the investigation of the efficiency of guard rings used for I/O-latch-up prevention," in *Proc. IEEE Int. Conf. Microelectron. Test Struct.*, Mar. 1990, pp. 35–39.
[15] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173–183, Jan. 1999.

Hui-Wen Tsai (S'07) received the M.S. degree in electrical engineering from National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 2007. She is currently pursuing the Ph.D. degree with the Institute of Electronics, NCTU.

Ming-Dou Ker (F'08) received the Ph.D. degree from the Institute of Electronics, National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 1993.

He is currently the Dean of the College of Photonics with NCTU.

Prof. Ker is an Editor of the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY.