



# Abnormal temperature-dependent floating-body effect on Hot-Carrier Degradation in PDSOI n-MOSFETs

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## ABSTRACT

This letter investigates abnormal degradation behavior after hot-carrier stress in partially-depleted silicon-on-insulator n-channel metal-oxide-semiconductor field effect transistors. It is found that the hot-carrier-induced degradation under floating body (FB) operation is more serious than that under grounded body (GB) operation due to the floating body effect (FBE). Furthermore, the degradation is independent on temperature under GB operation, because impact ionization is virtually independent on temperature under large  $V_D$ . However, the degradation under FB operation becomes less serious with increasing temperature. This is due to a smaller source/body PN junction band offset at a high temperature, which causes fewer accumulated holes at the body terminal and reduces the FBE.

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## 1. Introduction

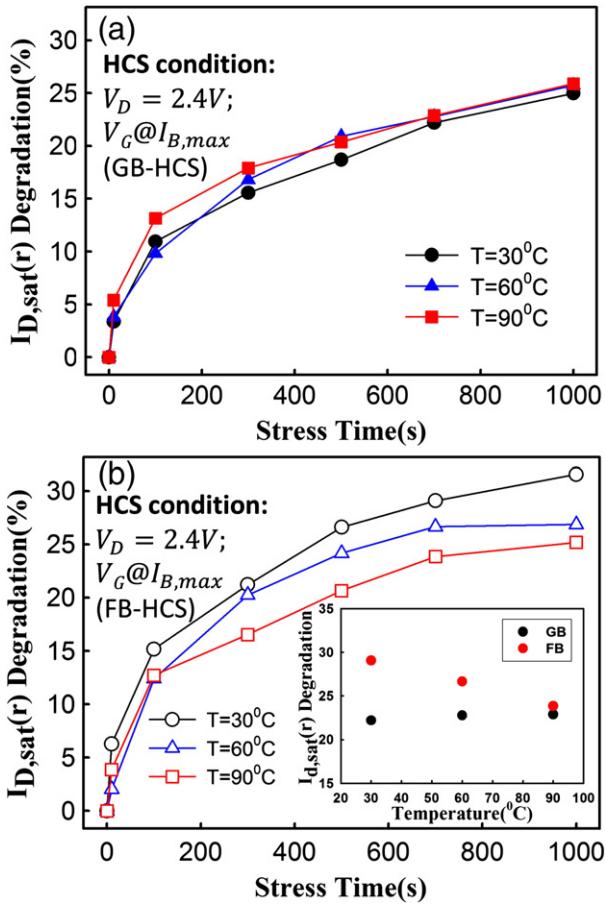
Recently, electronic products combining display panels [1–6], memory devices [7–34], and portable devices have become more popular for consumers. These electronic products are mostly composed of MOSFETs. However, there are many problems in conventional bulk-Si MOSFETs, such as latch-up, parasitic junction capacitances, short channel leakage and punch-through. The silicon-on-insulator (SOI) structure is a valid solution to these problems. The main advantages of SOI are related to the improved isolation and reduced parasitic junction capacitance, resulting in a reduced subthreshold swing, low leakage current, high operation speed, and low power consumption. Nevertheless, there are some drawbacks of the SOI structure, such as self-heating and the floating body effect (FBE) [35–37]. In addition, as the devices are scaled down, the SOI structure also suffers from severe hot-carrier effects (HCE). HCE in SOI MOSFETs has been extensively researched under grounded body (GB) operation [38,39]. Since the floating body potential may interact with the impact-ionization phenomenon, HCE is even more complicated in SOI MOSFETs [40–43]. Consequently, it is essential to clarify the mechanism of hot-carrier-induced degradation under FB operation.

In this letter, to investigate the influence of FB potential, hot-carrier-induced degradations under GB and FB operations are compared in partially depleted (PD) SOI MOSFETs. Experimental data show that the hot-carrier-induced degradation has different temperature dependence under FB and GB operations, indicating that a different mechanism dominates the degradation under FB and GB operations. The mechanism of FBE on hot-carrier-induced degradation is proposed and verified in this paper.

## 2. Experiment

Using 65-nm SOI CMOS technology, PD SOI n-type MOSFETs are employed with a T-gate structure to investigate the hot-carrier degradation at different temperatures under GB and FB operations. The silicon film and buried oxide thicknesses for the devices are 75 and 145 nm, respectively. The gate oxide with a thickness of 1.2 nm was grown by *in situ* steam generation, with the channel doping concentration being about  $3 \times 10^{18} \text{ cm}^{-3}$ . The channel currents follow in the <110> direction on (100) substrates. In this letter, devices with a channel width of 1  $\mu\text{m}$  and a length of 0.15  $\mu\text{m}$  were selected. Hot-carrier stress was carried out with either GB or FB operation to study the hot-carrier-induced degradation. To further investigate the impacts of FB operation,  $I_D-V_D$  output curves and the PN junction across the source and body terminals are characterized at temperatures ranging from 140 K to 385 K. All I-V curves were measured during an Agilent B1500 semiconductor parameter analyzer.

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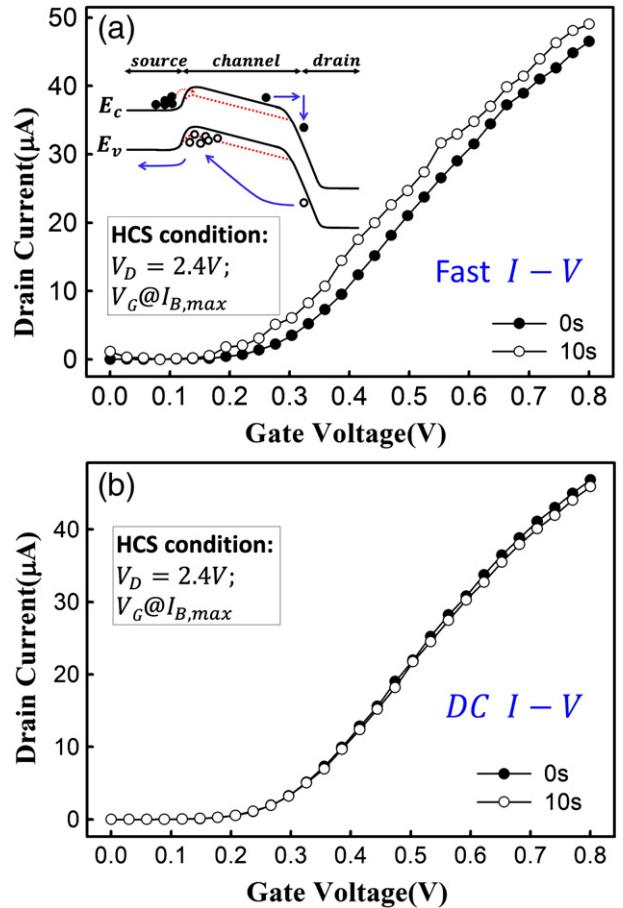


**Fig. 1.** Hot-carrier-induced degradation of saturation  $I_D$  measured with  $V_D = 1$  V under reverse-operation mode (source/drain interchanged) versus stress time at different temperatures under (a) GB and (b) FB operations. The inset of (b) shows the comparison of saturation  $I_D$  degradation between GB and FB operations under reverse-operation as a function of temperature.

### 3. Results and discussion

Hot carrier stress (HCS) is carried out with  $V_G$  at the maximum of body current and  $V_D = 2.4$  V. Fig. 1 shows hot-carrier-induced degradation of saturation  $I_D$  measured with  $V_D = 1$  V under reverse-operation mode (source/drain interchanged) ( $I_{D,sat}(r)$ ) versus stress time at different temperatures for the PD SOI MOSFETs. Fig. 1(a) shows that  $I_{D,sat}(r)$  degradation after GB-HCS is independent of temperature, whereas Fig. 1(b) shows that the degradation after FB-HCS becomes less significant with increasing temperature. It can be clearly observed that the  $I_{D,sat}(r)$  degradation under FB-HCS is more serious than that under GB-HCS at lower temperatures, becoming insignificant at high temperature, shown in the inset of Fig. 1(b).

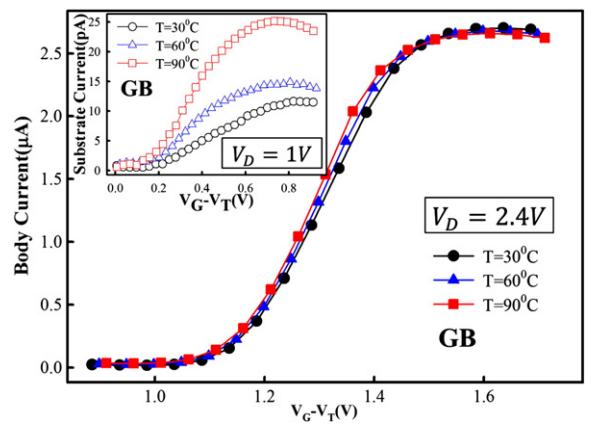
To further verify the mechanism of greater degradation under FB than that of GB, fast I-V measurement is performed. Compared with DC I-V, fast I-V measurement can shorten the measurement period from a few milliseconds to a few microseconds. Before stress, DC I-V and fast I-V measurements are both carried out under FB operation, and the initial characteristics are found to be identical. After 10 s of stress, fast I-V is performed instantaneously at the end of stress to investigate the transient phenomenon right after HCS, and then followed by a DC I-V measurement. Fig. 2 shows these fast I-V and DC I-V measurements before and after stress under FB operation. Unlike the conventional DC I-V that reveals a drain current deterioration after stress, as shown in Fig. 2(b), fast I-V shows a drain current rise after FB-HCS, shown in Fig. 2(a). This can be attributed to the fact that impact-ionization-generated holes are injected into the floating



**Fig. 2.**  $I_D$ - $V_G$  transfer characteristic curves by fast I-V measurement with drain voltage of 50 mV under hot carrier stress for 0 s and 10 s at  $30^\circ\text{C}$  under (a) fast I-V and (b) DC I-V measurements.

substrate, and the increase of substrate potential gives rise to a reduction of threshold voltage which leads to transient drain current increase in fast I-V measurement. Since the measurement is fast enough, the increase of drain current due to the FBE can be detected via fast I-V, as in Fig. 2(a). Because the accumulation of holes in the body reduces threshold voltage and results in the extra injection of electrons into the channel for impact ionization, degradation under FB is more serious than that under GB operation.

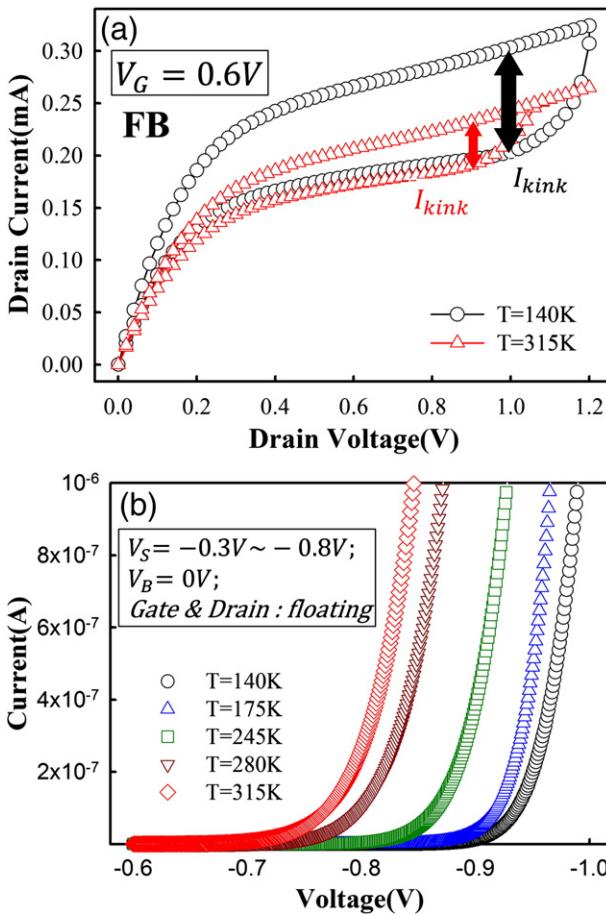
To further verify the effects of temperature on HCE under GB operation, body current with  $V_D = 2.4$  V (stress condition) is measured and



**Fig. 3.**  $I_B$ - $V_G$  at different temperatures with  $V_D = 2.4$  V under GB operation. Inset shows the  $I_B$ - $V_G$  curves with  $V_D = 1$  V under GB operation.

shown in Fig. 3. Corresponding to the  $I_D$  degradation which is independent on temperature, it can be clearly observed that body current with  $V_D = 2.4$  V is also independent on temperature. Accordingly, the degree of hot-carrier-induced degradation is dominated by impact-ionization rate. On the contrary,  $I_B$  measured with  $V_D = 1$  V increases with increasing temperature, shown in the inset of Fig. 3. This is because channel electrons do not have sufficient energy for impact ionization, and temperature significantly enhances impact-ionization at low  $V_D$  [44]. Therefore, at high temperature, even though carrier mobility and  $I_D$  are degraded,  $I_B$  still increases. Nevertheless, since channel electrons have sufficient energy for impact-ionization under high  $V_D$ , the impact ionization rate is insensitive to temperature. As a result, it is clear that hot-carrier-induced degradation under GB operation at different temperatures is dominated by the degree of impact ionization. However the origin of the temperature dependence of hot-carrier-induced degradation under FB operation is not yet clear.

Fig. 4(a) shows dual sweep of the  $I_D$ - $V_D$  output curves at low and high temperatures under FB operation. Because of the FBE,  $I_D$  suddenly rises in the saturation region [45]. Since the holes generated due to impact ionization at the body terminal cannot be recombined instantaneously, there is a drain current difference between the forward- and reverse-sweep, which is defined as  $I_{kink}$ . In order to understand the impact of temperature on FBE,  $I_{kink}$  is investigated at different temperatures. Obviously,  $I_{kink}$  is large at low temperature and is small at high temperature. It can be inferred that there are more holes at the body terminal at low temperature. However, the smaller  $I_B$  at low temperature, shown in Fig. 3, contradicts with this inference of more generated holes at low temperature in Fig. 4(a), since a smaller  $I_B$  should theoretically



**Fig. 4.** (a) Dual  $I_D$ - $V_D$  sweeps at low and high temperatures under FB operation, and (b) source/body PN junction with  $V_S = -0.3$  to  $-0.8$  V,  $V_B = 0$  V and floating gate and drain at different temperatures.

result in fewer holes. Fig. 4(b) shows the I-V characteristics of the PN junction across the source (N) and body (P) terminals at different temperatures with  $V_S = -0.3$  to  $0.8$  V,  $V_B = 0$  V and floating gate and drain. The  $V_{on}$  is defined as the source voltage when the forward-bias junction current equals 1 nA, and  $V_{on}$  difference at different temperatures is defined as  $\phi_B$ .

The equation of drain current in the saturation region can be simplified and expressed as:

$$I_D = \frac{W}{2L} \mu C_{ox} (V_G - V_T)^2 \quad (1)$$

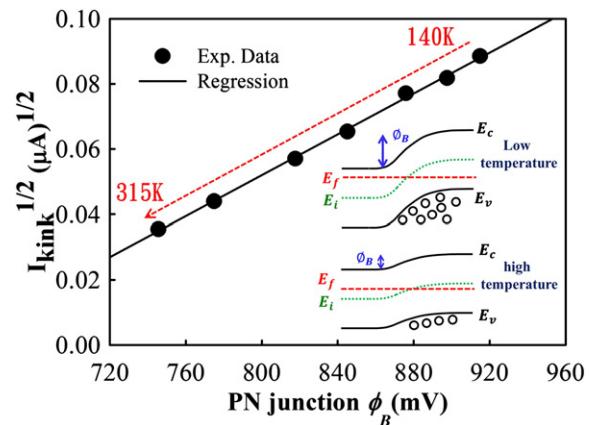
$$\sqrt{I_D} \propto V_G - V_T \quad (2)$$

$$\sqrt{I_{kink}} \propto \phi_B, \quad (3)$$

where  $W$  and  $L$  is the channel width and length, respectively,  $\mu$  is the carrier mobility,  $C_{ox}$  is the gate oxide capacitance per unit area, and  $V_T$  is the threshold voltage. Eq. 3 shows that  $I_{kink}$  is proportional to  $\phi_B$ , and the relationship between  $I_{kink}$  and  $\phi_B$  is plotted, as shown in Fig. 5. Fig. 5 shows the  $I_{kink} - \phi_B$  plot at different temperatures ranging from 140 K to 385 K, and the result exhibits an obvious linear dependence. Thus, based on the aforementioned investigation, the anomalous temperature dependence of FB-HCS-induced degradation can be elucidated as follows. The Fermi-levels both in the source and body are far from the intrinsic Fermi-level at low temperature, and approaches the intrinsic Fermi-level with increasing temperature, as in the inset of Fig. 5. Therefore, the PN junction is wider and  $\phi_B$  is large at low temperature and vice versa at high temperature. Furthermore, because of small  $\phi_B$  at high temperature, the ability of the PN junction to retain holes is poor and therefore the kink effect is less significant. As a result, the degree of hot-carrier-induced degradation under FB operation at different temperatures is dominated by the ability to retain holes at the source/body PN junction.

#### 4. Conclusion

This paper investigates the behavior of hot carrier-induced-degradation at different temperatures under GB and FB operations in PD SOI n-MOSFETs, and finds that the degradation under FB is more serious than that under GB operation due to the floating body effect. The hot-carrier-induced degradation is independent on temperature under GB operation, whereas the degradation under FB operation becomes less significant with increasing temperature. This is due to the



**Fig. 5.**  $\sqrt{I_{kink}}$  versus PN junction  $\phi_B$  with temperature ranging from 140 K to 315 K at increments of 35 K. The inset shows the band diagram of PN junction at low and high temperatures.

lessened ability to retain holes at the source/body PN junction at high temperature and the resultant insignificant FBE. According to this study, hot-carrier-induced degradation under GB operation at different temperatures is dominated by the impact ionization rate, while the degree of degradation under FB operation is dominated by the ability to retain holes at the source/body PN junction.

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## References

- [1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors, *Nature (London)* 432 (2004) 488.
- [2] C.T. Tsai, T.C. Chang, S.C. Chen, I. Lo, S.W. Tsao, M.C. Hung, J.J. Chang, C.Y. Wu, C.Y. Huang, Influence of positive bias stress on N<sub>2</sub>O plasma improved InGaZnO thin film transistor, *Appl. Phys. Lett.* 96 (2010) 242105.
- [3] T.C. Chen, T.C. Chang, C.T. Tsai, T.Y. Hsieh, S.C. Chen, C.S. Lin, M.C. Hung, C.H. Tu, J.J. Chang, P.L. Chen, Behaviors of InGaZnO thin film transistor under illuminated positive gate-bias stress, *Appl. Phys. Lett.* 97 (2010) 112104.
- [4] W.F. Chung, T.C. Chang, H.W. Li, C.W. Chen, Y.C. Chen, S.C. Chen, T.Y. Tseng, Y.H. Tai, Influence of H<sub>2</sub>O dipole on subthreshold swing of amorphous Indium-Gallium-Zinc-Oxide thin film transistors, *Electrochem. Solid-State Lett.* 14 (3) (2011) H114.
- [5] H.Y. Lu, P.T. Liu, T.C. Chang, S. Chi, Enhancement of brightness uniformity by a new voltage-modulated pixel design for AMOLED displays, *IEEE Electron. Device Lett.* 27 (9) (2006) 743.
- [6] S.C. Chen, T.C. Chang, P.T. Liu, Y.C. Wu, P.S. Lin, B.H. Tseng, J.H. Shy, S.M. Sze, C.Y. Chang, C.H. Lien, A novel nanowire channel poly-Si TFT functioning as transistor and nonvolatile SONOS memory, *IEEE Electron. Device Lett.* 28 (9) (2007) 809.
- [7] K.C. Chang, T.M. Tsai, T.C. Chang, K.H. Chen, R. Zhang, Z.Y. Wang, J.H. Chen, T.F. Young, M.C. Chen, T.J. Chu, S.Y. Huang, Y.E. Syu, D.H. Bao, S.M. Sze, Dual ion effect of the lithium silicate resistance random access memory, *IEEE Electron. Device Lett.* 35 (5) (2014) 530.
- [8] R. Zhang, K.C. Chang, T.C. Chang, T.M. Tsai, S.Y. Huang, W.J. Chen, K.H. Chen, J.C. Lou, J.H. Chen, T.F. Young, M.C. Chen, H.L. Chen, S.P. Liang, Y.E. Syu, S.M. Sze, Characterization of oxygen accumulation in Indium-Tin-Oxide for resistance random access memory, *IEEE Electron. Device Lett.* 35 (6) (2014) 630.
- [9] C.C. Shih, K.C. Chang, T.C. Chang, T.M. Tsai, R. Zhang, J.H. Chen, K.H. Chen, T.F. Young, H.L. Chen, J.C. Lou, T.J. Chu, S.Y. Huang, D.H. Bao, S.M. Sze, Resistive switching modification by ultraviolet illumination in transparent electrode resistive random access memory, *IEEE Electron. Device Lett.* 35 (5) (2014) 633.
- [10] T.J. Chu, T.M. Tsai, T.C. Chang, K.C. Chang, R. Zhang, K.H. Chen, J.H. Chen, T.F. Young, J. W. Huang, J.C. Lou, M.C. Chen, S.Y. Huang, H.L. Chen, Y.E. Syu, D.H. Bao, S.M. Sze, Tri-resistive switching behavior of hydrogen induced resistance random access memory, *IEEE Electron. Device Lett.* 35 (2) (2014) 217.
- [11] K.C. Chang, J.H. Chen, T.M. Tsai, T.C. Chang, S.Y. Huang, R. Zhang, K.H. Chen, Y.E. Syu, G.W. Chang, T.J. Chu, G.R. Liu, Y.T. Su, M.C. Chen, J.H. Pan, K.H. Liao, Y.H. Tai, T.F. Young, S.M. Sze, C.F. Ai, M.C. Wang, J.W. Huang, Improvement mechanism of resistance random access memory with supercritical CO<sub>2</sub> fluid treatment, *J. Supercrit. Fluids* 85 (2014) 183.
- [12] K.C. Chang, J.W. Huang, T.C. Chang, T.M. Tsai, K.H. Chen, T.F. Young, J.H. Chen, R. Zhang, J.C. Lou, S.Y. Huang, Y.C. Pan, H.C. Huang, Y.E. Syu, D.S. Gan, D.H. Bao, S.M. Sze, Space electric field concentrated effect for Zr:SiO<sub>2</sub> RRAM devices using porous SiO<sub>2</sub> buffer layer, *Nanoscale Res. Lett.* 8 (2013) 523.
- [13] R. Zhang, T.M. Tsai, T.C. Chang, K.C. Chang, K.H. Chen, J.C. Lou, T.F. Young, J.H. Chen, S. Y. Huang, M.C. Chen, C.C. Shih, H.L. Chen, J.H. Pan, C.W. Tung, Y.E. Syu, S.M. Sze, Mechanism of power consumption inhibitive multi-layer Zn:SiO<sub>2</sub>/SiO<sub>2</sub> structure resistance random access memory, *J. Appl. Phys.* 114 (2013) 234501.
- [14] Y.T. Su, K.C. Chang, T.C. Chang, T.M. Tsai, R. Zhang, J.C. Lou, J.H. Chen, T.F. Young, K.H. Chen, B.H. Tseng, C.C. Shih, Y.L. Yang, M.C. Chen, T.J. Chu, C.H. Pan, Y.E. Syu, S.M. Sze, *Appl. Phys. Lett.* 103 (2013) 163502.
- [15] K.C. Chang, T.M. Tsai, R. Zhang, T.C. Chang, K.H. Chen, J.H. Chen, T.F. Young, J.C. Lou, T.J. Chu, C.C. Shih, J.H. Pan, Y.T. Su, Y.E. Syu, C.W. Tung, M.C. Chen, J.J. Wu, Y. Hu, S.M. Sze, Electrical conduction mechanism of Zn:SiO<sub>2</sub> resistance random access memory with supercritical CO<sub>2</sub> fluid process, *Appl. Phys. Lett.* 103 (2013) 083509.
- [16] T.M. Tsai, K.C. Chang, R. Zhang, T.C. Chang, J.C. Lou, J.H. Chen, T.F. Young, B.H. Tseng, C.C. Shih, Y.C. Pan, M.C. Chen, J.H. Pan, Y.E. Syu, S.M. Sze, Performance and characteristics of double layer porous silicon oxide resistance random access memory, *Appl. Phys. Lett.* 102 (2013) 253509.
- [17] K.C. Chang, R. Zhang, T.C. Chang, T.M. Tsai, J.C. Lou, J.H. Chen, T.F. Young, M.C. Chen, Y.L. Yang, Y.C. Pan, G.W. Chang, T.J. Chu, C.C. Shih, J.Y. Chen, C.H. Pan, Y.T. Su, Y.E. Syu, Y.H. Tai, S.M. Sze, Origin of hopping conduction in Graphene-Oxide-Doped silicon oxide resistance random access memory devices, *IEEE Electron. Device Lett.* 34 (5) (2013) 677.
- [18] K.C. Chang, C.H. Pan, T.C. Chang, T.M. Tsai, R. Zhang, J.C. Lou, T.F. Young, J.H. Chen, C.C. Shih, T.J. Chu, J.Y. Chen, Y.T. Su, J.P. Jiang, K.H. Chen, H.C. Huang, Y.E. Syu, D.S. Gan, S.M. Sze, Hopping effect of hydrogen-doped silicon oxide insert RRAM by supercritical CO<sub>2</sub> fluid treatment, *IEEE Electron. Device Lett.* 34 (5) (2013) 617.
- [19] K.C. Chang, T.M. Tsai, T.C. Chang, Senior Member, H.H. Wu IEEE, K.H. Chen, J.H. Chen, T.F. Young, T.J. Chu, J.Y. Chen, C.H. Pan, Y.T. Su, Y.E. Syu, C.W. Tung, G.W. Chang, M.C. Chen, H.C. Huang, Y.H. Tai, D.S. Gan, J.J. Wu, Y. Hu, S.M. Sze, Low temperature improvement method on Zn:SiO<sub>2</sub> resistive random access memory devices, *IEEE Electron. Device Lett.* 34 (4) (2013) 511.
- [20] K.C. Chang, T.M. Tsai, T.C. Chang, H.H. Wu, J.H. Chen, Y.E. Syu, G.W. Chang, T.J. Chu, G. R. Liu, Y.T. Su, M.C. Chen, J.H. Pan, J.Y. Chen, C.W. Tung, H.C. Huang, Y.H. Tai, D.S. Gan, S.M. Sze, Characteristics and mechanisms of silicon oxide based resistance random access memory, *IEEE Electron. Device Lett.* 34 (3) (2013) 399.
- [21] T.M. Tsai, K.C. Chang, T.C. Chang, G.W. Chang, Y.E. Syu, Y.T. Su, G.R. Liu, K.H. Liao, M.C. Chen, H.C. Huang, Y.H. Tai, D.S. Gan, S.M. Sze, Origin of hopping conduction in Sn-doped silicon oxide RRAM with supercritical CO<sub>2</sub> fluid treatment, *IEEE Electron. Device Lett.* 33 (12) (2012) 1693.
- [22] T.M. Tsai, K.C. Chang, T.C. Chang, Y.E. Syu, S.L. Chuang, G.W. Chang, G.R. Liu, M.C. Chen, H.C. Huang, S.K. Liu, Y.H. Tai, D.S. Gan, Y.L. Yang, T.F. Young, B.H. Tseng, K.H. Chen, M.J. Tsai, C. Ye, H. Wang, S.M. Sze, Bipolar resistive RAM characteristics induced by Nickel Incorporated into Silicon Oxide Dielectrics for IC Applications, *IEEE Electron. Device Lett.* 33 (12) (2012) 1696.
- [23] T.M. Tsai, K.C. Chang, T.C. Chang, Y.E. Syu, K.H. Liao, B.H. Tseng, S.M. Sze, Dehydroxyl effect of Sn-doped silicon oxide resistance random access memory with supercritical CO<sub>2</sub> fluid treatment, *Appl. Phys. Lett.* 101 (2012) 112906.
- [24] K.C. Chang, T.M. Tsai, T.C. Chang, Y.E. Syu, K.H. Liao, S.L. Chuang, C.H. Li, D.S. Gan, S.M. Sze, The effect of silicon oxide based RRAM with Tin Doping, *Electrochem. Solid-State Lett.* 15 (3) (2012) H65.
- [25] K.C. Chang, T.M. Tsai, T.C. Chang, Y.E. Syu, C.-C. Wang, S.K. Liu, S.L. Chuang, C.H. Li, D. S. Gan, S.M. Sze, Reducing operation current of Ni-doped silicon oxide resistance random access memory by supercritical CO(2) fluid treatment, *Appl. Phys. Lett.* 99 (26) (2011) 263501.
- [26] K.C. Chang, T.M. Tsai, T.C. Chang, Y.E. Syu, H.C. Huang, Y.C. Hung, T.F. Young, D.S. Gan, N.J. Ho, Low-Temperature synthesis of ZnO nanotubes by supercritical CO<sub>2</sub> fluid treatment, *Electrochem. Solid-State Lett.* 14 (9) (2011) K47.
- [27] Y.E. Syu, T.C. Chang, J.H. Lou, T.M. Tsai, K.C. Chang, M.J. Tsai, Y.L. Wang, M. Liu, S.M. Sze, Atomic-level quantized reaction of HfO<sub>x</sub> memristor, *Appl. Phys. Lett.* 102 (2013) 172903.
- [28] Y.E. Syu, T.C. Chang, T.M. Tsai, G.W. Chang, K.C. Chang, Y.H. Tai, M.J. Tsai, Y.L. Wang, S. M. Sze, Silicon introduced effect on resistive switching characteristics of WO(X) thin films, *Appl. Phys. Lett.* 100 (2) (2012) 022904.
- [29] T.J. Chu, T.C. Chang, T.M. Tsai, H.H. Wu, J.H. Chen, K.C. Chang, T.F. Young, K.H. Chen, Y.E. Syu, G.W. Chang, Y.F. Chang, M.C. Chen, J.H. Lou, J.H. Pan, J.Y. Chen, Y.H. Tai, C. Ye, H. Wang, S.M. Sze, Charge quantity influence on resistance switching characteristic during forming process, *IEEE Electron. Device Lett.* 34 (4) (2013) 502.
- [30] Y.E. Syu, R. Zhang, T.C. Chang, T.M. Tsai, K.C. Chang, J.C. Lou, T.F. Young, J.H. Chen, M. C. Chen, Y.L. Yang, C.C. Shih, T.J. Chu, J.Y. Chen, C.H. Pan, Y.T. Su, H.C. Huang, D.S. Gan, S.M. Sze, Endurance improvement technology with nitrogen implanted in the interface of WSiO<sub>x</sub> resistance switching device, *IEEE Electron. Device Lett.* 34 (7) (2013) 864.
- [31] T.C. Chang, F.Y. Jian, S.C. Chen, Y.T. Tsai, Developments in nanocrystal memory, *Mater. Today* 14 (2011) 608.
- [32] M.C. Chen, T.C. Chang, C.T. Tsai, S.Y. Huang, S.C. Chen, C.W. Hu, S.M. Sze, M.J. Tsai, Influence of electrode material on the resistive memory switching property of indium gallium zinc oxide thin films, *Appl. Phys. Lett.* 96 (2010) 262110.
- [33] Y.E. Syu, T.C. Chang, T.M. Tsai, Y.C. Hung, K.C. Chang, M.J. Tsai, M.J. Kao, S.M. Sze, Redox reaction switching mechanism in RRAM device with Pt/CoSiO<sub>x</sub>/TiN structure, *IEEE Electron. Device Lett.* 32 (2011) 545.
- [34] J. Jomah, G. Ghibaudo, F. Balestra, Analysis and modeling of self-heating effects in thin-film SOI MOSFETs as a function of temperature, *Solid State Electron.* 38 (1995) 615.
- [35] C.H. Dai, T.C. Chang, A.K. Chu, Y.J. Kuo, S.C. Chen, C.C. Tsai, S.H. Ho, W.H. Lo, G. Xia, O. Cheng, C.T. Huang, On the origin of hole valence band injection on GfBE in PD SOI n-MOSFETs, *IEEE Electron. Device Lett.* 31 (2010) 540.
- [36] W.H. Lo, T.C. Chang, C.H. Dai, W.L. Chung, C.E. Chen, S.H. Ho, O. Cheng, C.T. Huang, Impact of mechanical strain on GfBE in PD SOI p-MOSFETs as indicated from NBTT degradation, *IEEE Electron. Device Lett.* 33 (2012) 303.
- [37] C. Hu, S.C. Tam, F.C. Hsu, P.K. Ko, T.Y. Chan, K.W. Terrill, Hot-electron-induced MOSFET degradation-model, monitor, and improvement, *IEEE Electron. Device Lett.* ED32 (1985) 375.
- [38] P. Heremans, R. Bellens, G. Groeseneken, H.E. Maes, Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFETs, *IEEE Electron. Device Lett.* 35 (1988) 2194.
- [39] D. Munteanu, A.M. Ionescu, Modeling of drain current overshoot and recombination lifetime extraction in floating-body submicron SOI MOSFETs, *IEEE Electron. Device Lett.* 49 (2002) 1198.
- [40] Y.C. Tseng, W.M. Huang, C. Hwang, J.C.S. Woo, AC floating body effects in partially depleted floating body SOI nMOS operated at elevated temperature: an analog circuit prospective, *IEEE Electron. Device Lett.* 21 (2000) 494.
- [41] M. Emam, J.C. Tinoco, D.V. Janvier, J.P. Raskin, High-temperature DC and RF behaviors of partially-depleted SOI MOSFET transistors, *Solid State Electron.* 52 (2008) 1924.

- [42] M. Emam, J.P. Raskin, Partially depleted SOI versus deep n-well protected bulk-Si MOSFETs: a high-temperature RF study for low-voltage low-power applications, *IEEE Microw. Theory Tech. Soc.* 61 (2013) 1496.
- [43] D.S. Jeon, D.E. Burk, A temperature-dependent SOI MOSFET model for high-temperature application (27 °C–300 °C), *IEEE Trans. Electron. Devices* 38 (1991) 2101.
- [44] P. Aminzadeh, M. Alavi, D. Scharfetter, Temperature dependence of substrate current and hot carrier-induced degradation at low drain bias, *IEEE Symp. VLSI Technol.* (1998) 178.
- [45] S.C. Lin, J.B. Kuo, Temperature-dependent Kink effect model for partially depleted SOI NMOS devices, *IEEE Trans. Electron. Devices* 46 (1999) 254.