Analog Integr Circ Sig Process (2014) 81:645–655
DOI 10.1007/s10470-014-0421-y

Background calibration of integrator leakage in discrete-time delta-sigma modulators

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Received: 26 March 2014 / Revised: 31 August 2014 / Accepted: 30 September 2014 / Published online: 16 October 2014

Abstract This paper presents an integration-leakage calibration technique for the switched-capacitor integrators in a delta-sigma modulator (DSM). Integrators realized with low-gain opamps are lossy. A DSM that uses lossy integrators exhibits a degraded signal-to-quantization-noise ratio. To calibrate an integrator, its integration leakage is detected in the digital domain, and the leakage compensation is applied to the same integrator in the analog domain. The proposed scheme can calibrate all integrators in a discrete-time DSM of any form. It can be proceed in the background without interrupting the normal DSM operation. The design considerations for the proposed calibration scheme are discussed. Design cases of a 1st-order, a 2nd-order, and a 3rd-order DSM are demonstrated and simulated.

1 Introduction

Delta-sigma modulators (DSMs) are widely used in high-resolution analog-to-digital converters (ADCs). A DSM can effectively suppress the quantization noises arising from its internal quantizer by combining its noise-shaping function with the oversampling operation. Comparing to Nyquist-rate ADCs of similar performance, DSMs require analog circuits of higher speed. Consider a discrete-time single-loop DSM that comprises a cascade of switched-capacitor (SC) integrators. Each integrator contains an opamp. The open-loop unity-gain frequency and slew rate of the opamp determine the speed of the integrator, while the dc voltage gain of the opamp dictates the quality of the integration function. An SC integrator realized with a low-gain opamp is lossy, i.e., it exhibits integration leakage. If the integrators in a DSM are lossy, the noise-shaping capability of the DSM is weakened, resulting in degraded signal-to-quantization-noise ratio (SQNR).

As CMOS technologies advances, MOSFETs become smaller and faster, but their intrinsic voltage gain, g_m/g_{ds}, also decreases. Consider a standard 32 nm CMOS. A minimum-channel-length MOSFET has a maximum transit frequency f_T of over 400 GHz, but it has an intrinsic gain of only about six [1]. Furthermore advanced CMOS technologies have lower supply voltage, it is difficult to design high-speed opamps that also have a good dc gain. Although correlated double sampling [2], correlated level shifting [3], and multiple-stage configuration [4] can be used to raise the dc gain of opamps, all sacrifice the speed.

To take advantage of the advanced nano-scale CMOS technologies, we propose using opamps with simple circuit configuration and MOSFETs of minimum channel length. The resulting SC integrators are high-speed and low-power but also lossy. We then employ calibration to compensate the integration leakage of the integrator and recover the noise-shaping capability of the DSM. There are calibration techniques that can improve the frequency accuracy of the noise-shaping functions of the DSMs [5–8]. They all assume the opamps have sufficiently large dc gain. A calibration technique has been proposed to correct both the integration leakage and the distortion of the integrators in a cascade DSM [9]. However, it is difficult to obtain the required modeling parameters from the DSM digital output alone.

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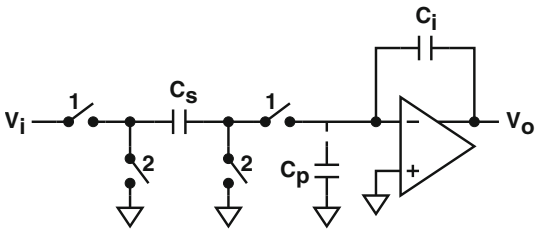


Fig. 1 A conventional switched-capacitor (SC) integrator

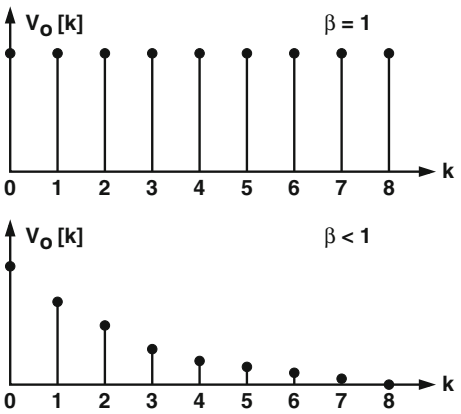


Fig. 2 Integrator time-domain output response. $V_i[k] = 0$ for $k > 0$

This paper proposes an integration-leakage calibration technique for the integrators in an SC DSM. To calibrate an integrator, its integration leakage is detected in the digital domain, while the leakage compensation is added to the same integrator in the analog domain. Once all integrators are calibrated, the SQNR performance of the DSM is restored. The proposed scheme can calibrate all integrators in a DSM of any form. It calibrates one integrator at a time. It can proceed in the background without interrupting the normal DSM operation.

The rest of this paper is organized as follows. Section 2 discusses the effect of integration leakage on the SQNR performance of DSMs. Section 3 introduces the SC integrators with leakage compensation. Section 4 introduces the proposed calibration technique with a 1st-order DSM design case. Design considerations are outlined. Section 5 applies the calibration technique to a 2nd-order DSM design case. Section 6 applied the techniques to high-order DSMs. Section 7 demonstrates a 3rd-order DSM design case. Finally, Sect. 8 draws conclusions.

2 Integration leakage and its effect

Figure 1 presents a conventional SC integrator, its z-domain transfer function is

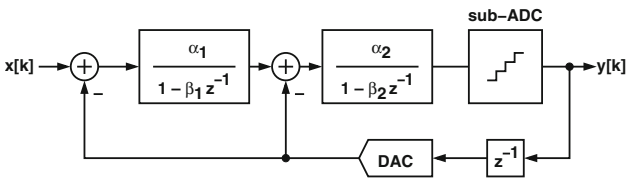


Fig. 3 A delta-sigma modulator with lossy integrators

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{\alpha}{1 - \beta z^{-1}} \tag{1}$$

with

$$\alpha = \frac{-\frac{C_s}{C_i}}{1 + \frac{1}{A_0} \cdot \frac{C_i + C_s + C_p}{C_i}} \qquad \beta = \frac{1 + \frac{1}{A_0} \cdot \frac{C_i + C_p}{C_i}}{1 + \frac{1}{A_0} \cdot \frac{C_i + C_s + C_p}{C_i}} \tag{2}$$

where A_0 is the dc voltage gain of the opamp and C_p is the total parasitic capacitance associated with the negative terminal of the opamp. If the opamp is ideal with $A_0 = \infty$, then $\alpha = -C_s/C_i$ and $\beta = 1$. Figure 2 illustrates the integrator time-domain output response, in which $V_i[k] = 0$ for $k > 0$. If $\beta = 1$, $V_o[k]$ maintains its $V_o[0]$ value for $k > 0$. If $\beta < 1$, then the charge on capacitor C_i leaks and $V_o[k]$ decreases as k progresses. An integrator with $\beta < 1$ is a lossy integrator.

Figure 3 shows a DSM that uses the lossy integrators. Although the coefficient α for the integrator of Fig. 1 is negative, the coefficients α_1 and α_2 in Fig. 3 are positive for simplicity. Their polarities can be easily changed in a fully differential circuit configuration. Assume the digital-to-analog converter (DAC) is ideal. The difference between the sampled analog input $x[k]$ and the DAC output is integrated by two lossy integrators and then quantized by a sub-ADC. The sub-ADC introduces quantization errors $e[k]$. The sub-ADC digital output $y[k]$ can be expressed as $Y(z) = \mathrm{STF(z)} \cdot \mathrm{X(z)} + \mathrm{NTF(z)} \cdot \mathrm{E(z)}$. Where STF(z) is the signal transfer function and NTF(z) is the noise transfer function. If the integrators are lossy, i.e., $\beta_1 < 1$ and $\beta_2 < 1$, then the zeros of the NTF deviate from the unit circle in the z-plane, diminishing the the DSM's ability of suppressing the sub-ADC quantization errors. Consider an M-th order DSM with M lossy integrators. Its NTF is expressed as

$$\mathrm{NTF(z)} = \left(1 - \beta z^{-1}\right)^{\mathrm{M}} \tag{3}$$

The β coefficients are assumed to be identical for simplicity. If the sub-ADC in the DSM has B-bit resolution, then the DSM's maximum SQNR is

$$\mathrm{SQNR} = 2^{\mathrm{B}} \times \sqrt{3/2} \times \mathrm{SQNR_{NTF}} \tag{4}$$

where $\mathrm{SQNR_{NTF}}$ is the SQNR enhancement by the NTF. It can be expressed as

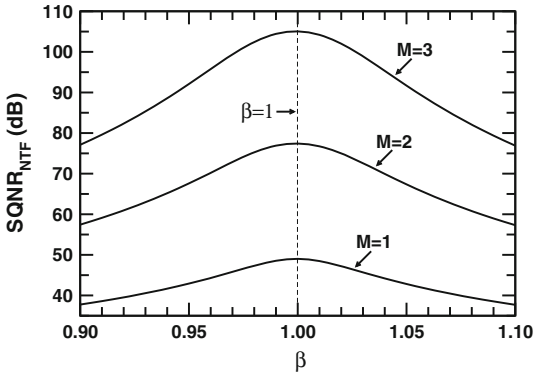


Fig. 4 DSM SQNR enhancement versus β. Assume OSR = 64. For a 1st-order DSM, $M = 1$. For a 2nd-order DSM, $M = 2$. For a 3rd-order DSM, $M = 3$

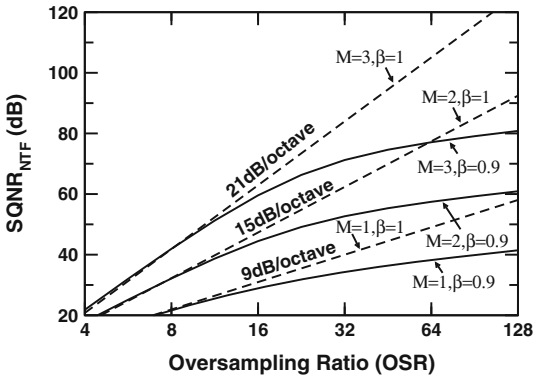


Fig. 5 DSM SQNR enhancement versus oversampling ratio (OSR)

$$\mathrm{SQNR_{NTF}} = \frac{\mathrm{P_e}}{\mathrm{P_{e,sh}}} = \frac{2\mathrm{M}+1}{\theta \cdot \pi^{2\mathrm{M}}} \times \mathrm{OSR}^{2\mathrm{M}+1} \tag{5}$$

with

$$\theta = \sum_{n=0}^{M} \frac{M!}{n!(M-n)!} \frac{(2M+1)\beta^{M-n}}{2M-2n+1} \left[\frac{\mathrm{OSR}(1-\beta)}{\pi}\right]^{2n} \tag{6}$$

where OSR is the oversampling ratio. If $\beta = 1$, then each term of (6) is zero except $n = 0$, and $\theta = 1$. If $\beta \neq 1$, then $\theta > 1$, yielding a larger in-band quantization noise power.

Figure 4 shows the effects of β on $\mathrm{SQNR_{NTF}}$ when OSR = 64. If $\beta = 1$, an ideal 3rd-order DSM can offer an $\mathrm{SQNR_{NTF}}$ of 105 dB. However, if $\beta = 0.9$, the resulting $\mathrm{SQNR_{NTF}}$ is degraded to 77 dB. Figure 5 shows the effects of β on $\mathrm{SQNR_{NTF}}$ when OSR increases. For an ideal M-order DSM, the $\mathrm{SQNR_{NTF}}$ is improved by $6M + 3$ dB when the OSR is doubled. If $\beta < 1$, it becomes less effective for the DSM to improve $\mathrm{SQNR_{NTF}}$ by increasing OSR. Although above conclusions are established on assuming that all NTF's zeros are located at β for simplicity, similar results are obtained even NTF's zeros are separated.

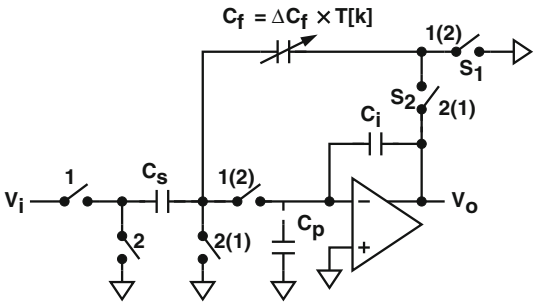


Fig. 6 A switched-capacitor integrator with leakage compensation. It is either an inverting integrator or a non-inverting integrator, depending the clock phases denoted on the switches

3 Integrator with leakage compensation

Consider the lossy integrator, its output falls by $(1-\beta)V_o[k-1]$ from cycle $k-1$ to cycle k. Figure 6 shows the proposed SC integrator to compensate this leakage. The capacitor C_f is added to sample V_o. The charge on C_f is added to the integrator in the next clock cycle. Similar integrators can be found in [10, 11]. The resulting β coefficient of the integrator is

$$\beta = \frac{1 + \frac{C_f}{C_i} + \frac{1}{A_0}\frac{C_i+C_p}{C_i}}{1 + \frac{1}{A_0}\frac{C_i+C_s+C_f+C_p}{C_i}} \tag{7}$$

If $C_f = C_s/(A_0 - 1)$, then $\beta = 1$ and the integrator becomes lossless. Since $C_f \ll C_s$, this C_f capacitor and its associated switches add minuscule loading and noise to the integrator. The required C_f is sensitive to process-voltage-temperature variations. Therefore, the integrator requires calibration to adjust C_f. In our design, a digital signal $T[k] \in \{0, 1, 2, \ldots\}$ controls C_f. A calibration processor (CP) continuously runs in the background to adjust C_f to ensure $\beta = 1$. The adjustable β can be expressed as

$$\beta = \beta_0 + \Delta\beta \times T[k] \tag{8}$$

where

$$\Delta\beta = \frac{1 + \frac{1}{A_0}\frac{C_s+C_p}{C_i}}{1 + \frac{2}{A_0}\frac{C_i+C_s+C_{f0}+C_p}{C_i}} \times \frac{\Delta C_f}{C_i} \tag{9}$$

and ΔC_f is the digital-control capacitance step size. A smaller ΔC_f makes β closer to 1 when calibration is applied to adjust C_f, resulting in a better $\mathrm{SQNR_{NTF}}$.

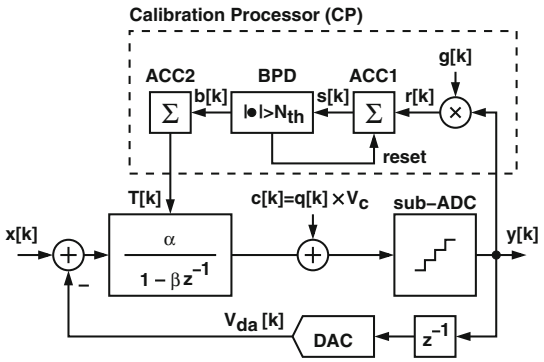


Fig. 7 A 1st-order DSM with the proposed calibration scheme

4 First-order DSM design case

4.1 Architecture

Figure 7 shows a 1st-order DSM using the integrator of Fig. 6. If $C_s = C_i$ and $A_0 = 8$, then $\alpha = 0.8$ and $\beta = 0.9$. This DSM includes a background calibration that automatically adjusts the C_f capacitor in the integrator to maximize the DSM's SQNR. The sub-DAC has N levels and covers an output range of ± 1. The least-significant-bit (LSB) size is $\Delta = 2/(N-1)$. The DSM output is $y[k]$. If N is odd, $y[k]$ has its value among $\{0, \pm 1, \pm 2, \ldots, \pm (N-1)/2\}$. If N is even, $y[k]$ has its value among $\{\pm 0.5, \pm 1.5, \ldots, \pm (N/2 - 0.5)\}$, The DAC output is $V_{da}[k] = \Delta \times y[k-1]$. The input thresholds of sub-ADC correspond to the middle of adjacent DAC outputs, its LSB size is also Δ. The DSM has a sampling rate of f_s. The modulator digital output $y[k]$ is

$$\Delta \times Y = \mathrm{STF}_1 \cdot \mathrm{X} + \mathrm{NTF}_1 \cdot \mathrm{E} \tag{10}$$

where

$$\mathrm{STF}_1 = \frac{\mathrm{H}}{1 + \mathrm{z}^{-1}\mathrm{H}} \quad \mathrm{NTF}_1 = \frac{1}{1 + \mathrm{z}^{-1}\mathrm{H}} \tag{11}$$

and H is the transfer function of the integrator expressed in (1). As proposed in Sect. 3, the β of the integrator is adjustable. It is adjusted automatically by the calibration processor (CP) shown in Fig. 7. To facilitate calibration, a periodic square wave $c[k] = q[k] \times V_c$ is added to the sub-ADC input. The CP detects the calibrating signal embedded in $y[k]$, generates a control signal $T[k]$, and adjusts β to make $\beta = 1$.

Figure 8 shows a signal flow diagram of the calibration. The modulator input $x[k]$ and sub-ADC quantization errors $e[k]$ are shaped by STF_1 and NTF_1 respectively. The calibrating signal $c[k]$ is shaped by NTF_1, yielding $d[k]$. The summation of the above three signals is converted to $y[k]$

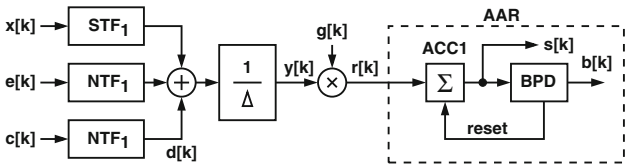


Fig. 8 Calibration signal flow diagram

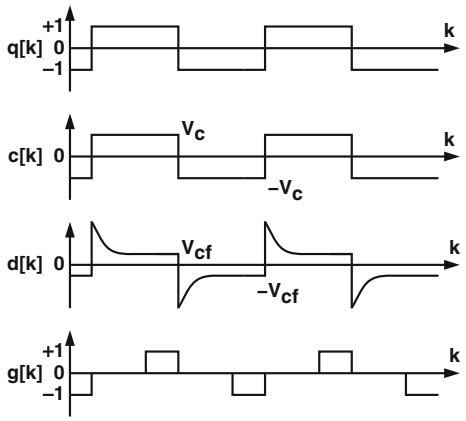


Fig. 9 Calibration signal waveforms

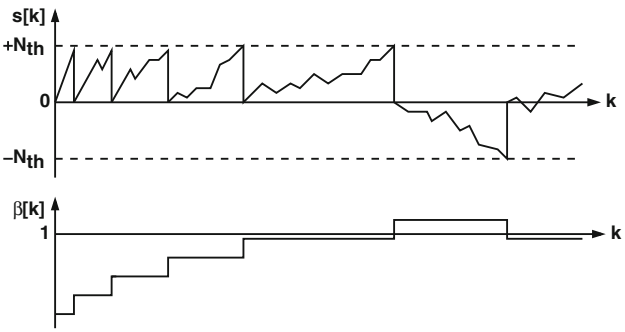


Fig. 10 Accumulation-and-reset (AAR) operation

with a conversion gain of $1/\Delta$. The calibrating signal $c[k]$ is expressed as a periodic binary square wave $q[k] \in \{-1, +1\}$ multiplied by an amplitude of V_c. Thus, embedded in $y[k]$, $d[k]$ is the step response of NTF_1 triggered by $c[k]$. Figure 9 shows the $d[k]$ waveform. The step response has an initial value of

$$V_{ci} = V_c \times \frac{2\alpha + 1 - \beta}{\alpha + 1 - \beta} \tag{12}$$

and settles toward a final value of

$$V_{cf} = V_c \times \frac{1 - \beta}{\alpha + 1 - \beta} \tag{13}$$

Since V_{cf} depends on $1 - \beta$, it can be used to detect β.

Figure 8 shows the CP operation. The CP correlates the DSM output $y[k]$ with a triple-valued sequence $g[k] \in \{-1, 0, +1\}$. The $g[k]$ waveform is illustrated in Fig. 9. It has the same polarity as $q[k]$, but its value is set to 0 during the initial transition phase of $d[k]$. Thus, the resulting product $r[k]$ contains only the valid V_{cf} information. Following $r[k]$ is an accumulator (ACC1). It is followed by a binary peak detector (BPD). Together they perform the accumulation-and-reset (AAR) operation [12] to extract V_{cf} from $r[k]$ while removing the perturbations caused by $x[k]$ and $e[k]$. The AAR operation is described as follows. Accumulator ACC1 accumulates the $r[k]$ sequence. Its output $s[k]$ is monitored by a BPD with a threshold $N\text{th} > 0$. Whenever $s[k]$ reaches either $+N\text{th}$ or $-N\text{th}$, the BPD issues an output $b[k] = +1$ or $b[k] = -1$ for one clock cycle respectively and reset $s[k]$ to 0. The BPD output $b[k]$ remains at 0 when no reset occurs. The BPD output $b[k]$ is an estimate of the $(1 - \beta)$ polarity. The CP uses it to adjust the β of the integrator. As shown in Fig. 7, following $b[k]$ is another accumulator, ACC2, that accumulates the $b[k]$ sequence. Its output $T[k]$ controls the β according to (8). Figure 10 illustrates the time-domain waveform of the ACC1 output s, and the waveform of the resulting β. When β approaches 1, both $|1 - \beta|$ and V_{cf} become smaller, and it takes a longer time to activate the BPD.

4.2 Calibration parameters

This calibration has five design parameters, including the $c[k]$ amplitude V_c, the $c[k]$ frequency f_q, the $g[k]$ duty ratio D_g, the BPD threshold $N\text{th}$, and the $T[k]$ control step size $\Delta\beta$. Referring to Fig. 9, the duty ratio D_g is defined as the ratio of the time for $g[k] = +1$ to the time for $q[k] = +1$. The duty ratio for $g[k] = -1$ and $q[k] = -1$ is assumed to be the same as D_g.

We use the aforementioned 1st-order DSM design case to illustrate the design considerations for the proposed calibration scheme. The DSM block diagram is shown in Fig. 7. Its sub-ADC and DAC have $N = 16$ quantization steps. The corresponding quantization step size is $\Delta = 2/15$. It has a sampling frequency of f_s and a corresponding sampling period of $T_s = 1/f_s$. The integrator in Fig. 7 is realized using the SC integrator of Fig. 6 with a transfer function of (1). If the opamp has a dc gain of $A_0 = 8$, then $\alpha = 0.8$ and $\beta = 0.9$. Assume the OSR of the DSM is 64. Its theoretical maximum SQNR is 74 dB when $A_0 = \infty$. We will apply the proposed calibration to recover SQNR.

As shown in Fig. 7, the calibration square wave $c[k] = q[k] \times V_c$ is added to the sub-ADC input. Let $c[k]$ have a frequency of f_q, a corresponding period of $T_q = 1/f_q$, and a duty cycle of 50 %. The resulting $d[k]$, as shown in Fig. 9, is embedded in the sub-ADC output $y[k]$. In each f_q cycle, the transient response of $d[k]$ is a step response of NTF_1 triggered by $c[k]$. It can be expressed as

$$d[k] = V_c \times \frac{2\alpha(\beta - \alpha)^k + (1 - \beta)}{\alpha + 1 - \beta} \tag{14}$$

This step response has an initial value of V_{ci} of Fig. (12) and then settles toward the V_{cf} of (13). Figure 11 shows several $d[k]$ waveforms with different β.

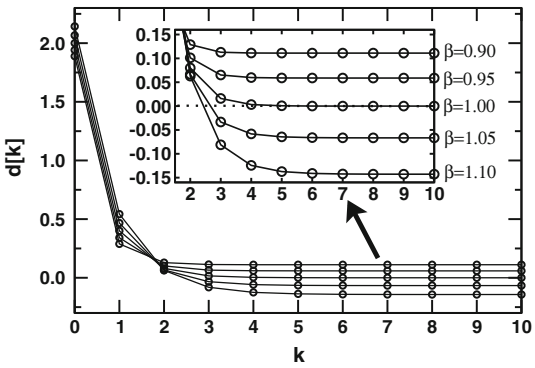


Fig. 11 The transient response of $d[k]$ with different β

The $d[k]$ waveforms have settled near V_{cf} for $k > 5$. We choose $T_q = 16T_s$ and $D_g = 1/4$, so that, in each $d[k]$ transient, $d[k]$ has a period of 6 clock cycles to settle before $g[k]$ is activated for 2 clock cycles. The frequency of the injected signal $c[k]$ is $f_q = f_s/16$. As long as OSR > 8, the frequency components of $d[k]$ in $y[k]$ is outside the signal band. It can be easily removed by the decimation filter following the DSM.

The injection of the calibration signal $c[k]$ degrades the DSM's maximum SQNR, since $c[k]$ increases the input signal range of the sub-ADC input. The SQNR degradation is a function of the $c[k]$ amplitude V_c. Figure 12 shows the simulated SQNR of the DSM design case. The injected $c[k]$ has a frequency $f_q = f_s/16$. In Fig. 12, SQNR is plotted against $x[k]$ input amplitude with different V_c. The $x[k]$ frequency is $f_{in} = (41/2^{16})f_s$. If $V_c = 1\Delta = 2/15$, the maximum SQNR is 71 dB at -1.5 dBFS. If $V_c = 3\Delta = 6/15$, the maximum SQNR is 67 dB at -3.0 dBFS. If $V_c = 5\Delta = 10/15$, the maximum SQNR is 66 dB at -4.5 dBFS. In this design example, we choose $V_c = 1\Delta$.

Figure 10 illustrates the transient response of β during the calibration. Consider the DSM shown in Fig. 7. The averaged variation of $s[k]$ for one clock cycle is $\Delta s = D_g V_{cf}/\Delta$. It takes $N\text{th}/\Delta\text{s}$ cycles for $s[k]$ to accumulate from 0 to $+N\text{th}$ (or $-N\text{th}$) so that $T[k]$ is changed by 1 and β is changed by $\Delta\beta$. Thus, we have

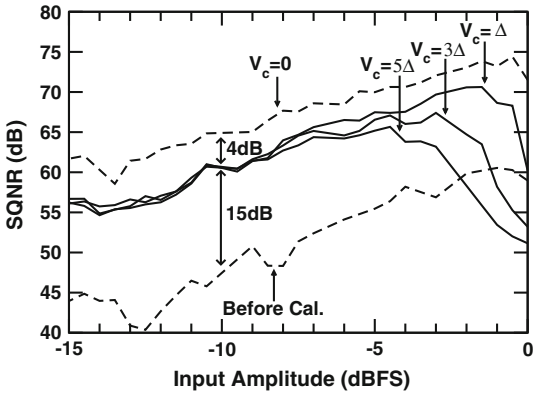


Fig. 12 SQNR of the 1st-order DSM design case with different V_c. The opamp in the DSM is ideal

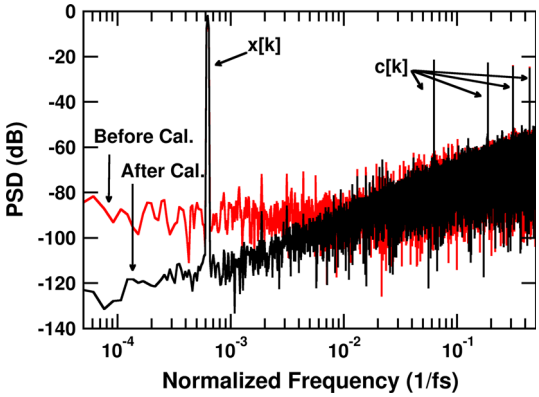


Fig. 14 Output spectra of the 1st-order DSM design case

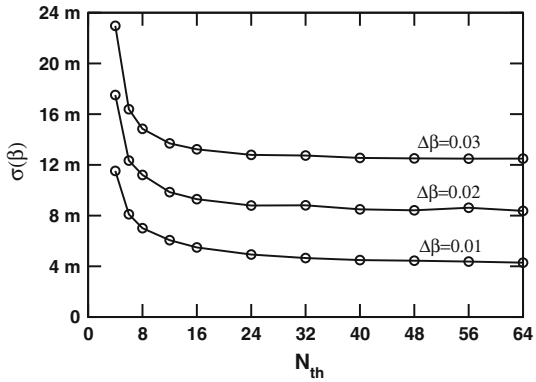


Fig. 13 $\sigma(\beta)$ versus Nth with different $\Delta\beta$

$$\frac{d\beta}{dk} = \frac{\Delta\beta}{N\text{th}/\Delta\text{s}} \approx \frac{\Delta\beta D_g V_c}{\alpha N\text{th}\Delta}(1-\beta) \tag{15}$$

This calibration loop can be modeled as a single-pole feedback system. The transient response of β can be expressed as

$$\beta[k] = 1 - (1-\beta[0]) \times e^{-k/\tau} \tag{16}$$

The time constant τ is

$$\tau = \frac{N\text{th}}{D_g} \cdot \frac{\Delta}{V_c} \cdot \frac{\alpha}{\Delta\beta} \tag{17}$$

From (17), a smaller Nth and a larger $\Delta\beta$ lead to a smaller τ, yielding a faster calibration speed. However, as the calibration process converges, the behavior of $\beta[k]$ becomes a discrete random fluctuation around 1 [12]. Referring to Fig. 8, both $x[k]$ and $e[k]$ induce this fluctuation. Their effects are diminished by the AAR operation. A larger Nth and a smaller $\Delta\beta$ lead to a smaller fluctuation in β, yielding the better SNDR performance for the DSM.

Figure 13 shows the standard deviation of the $\beta[k]$ fluctuation from the system simulation of the DSM design case. The standard deviation $\sigma(\beta)$ increases drastically for $N\text{th} < 8$. As Nth increases, the standard deviation of β fluctuation, $\sigma(\beta)$, converges to an averaged value, that can be expressed as

$$\sigma(\beta) = \frac{\Delta\beta}{\sqrt{6}} \tag{18}$$

From Fig. 4, SQNR_{NTF} is degraded by less than 1 dB if $3\sigma(\beta) < 0.015$. Using (18), we need $\Delta\beta < 0.0122$. In this design case, we choose $\Delta\beta = 0.01$ and $N\text{th} = 24$.

4.3 Simulation results

This 1st-order DSM design case is verified by using time-domain simulation. Calibration design parameters are $f_q = f_s/16, D_g = 0.25, V_c = 1\Delta, \Delta\beta = 0.01$, and $N\text{th} = 24$. The resulting time constant $\tau = 7680$ sampling periods. It takes a calibration time of 3τ for β to converge from 0.9 to 0.995, where the SQNR degradation due to a non-ideal β is less than 1 dB. Assume the DSM input bandwidth is 2 MHz and the sampling frequency is $f_s = 256$ MHz. Then a calibration time of 3τ is 0.09 m/s. Figure 14 shows the DSM output spectra before and after calibration. The input is a sine wave with a frequency of $(41/2^{16})f_s$ and an amplitude of -2 dBFS. The resulting SQNR is 58 dB before calibration, and is improved to 70 dB after calibration. The frequency components of $c[k]$ are visible in Fig. 14. They are far away from the signal band.

5 Second-order DSM design case

Figure 15 shows a 2nd-order DSM. It includes two integrators. The internal opamps of the integrators have a dc gain of 8.2 and 7.7 respectively, yielding $\alpha_1 = 0.804$, $\beta_1 = 0.902, \alpha_2 = 0.794$, and $\beta_2 = 0.897$. The regular sub-ADC1 following the 2nd integrator is single comparator.

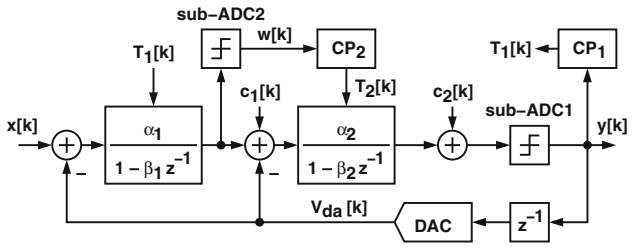


Fig. 15 A 2nd-order DSM with the proposed calibration scheme

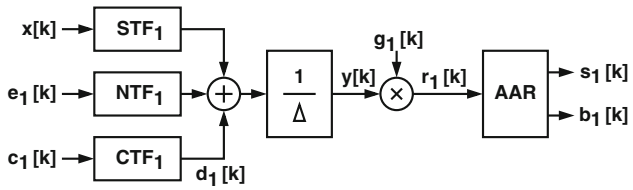


Fig. 16 Calibration signal flow diagram for β_1 calibration.

Thus, for this 2nd-order DSM, $N = 2$ and $\Delta = 2$. If the integrators are ideal and OSR = 64, then the theoretical maximum SQNR is 79 dB.

The proposed calibration scheme adjusts β_1 and β_2 separately. Integrators with adjustable β are described in Sect. 3. To calibrate β_1, a calibration signal $c_1[k] = q_1[k] \times V_{c1}$ is injected to the input of the 2nd integrator. A calibration processor, CP1, takes the sub-ADC1 output $y[k]$ and generates a control signal $T_1[k]$ to adjust β_1 of the 1st integrator. The calibration signal $c_1[k]$ is a square wave with f_{q1} frequency, V_{c1} amplitude, and 50 % duty cycle. The calibration processor CP1 is identical to the CP shown in Fig. 8. In the CP1, its $g_1[k]$ signal has a duty ratio of D_{g1} and its BPD has a threshold of Nth1. Its output $T_1[k]$ controls the β_1 of the first integrator such that $\beta_1[k] = \beta_{0,1} + \Delta\beta_1 \times T_1[k]$. Figure 16 shows the calibration signal flow diagram, where $e_1[k]$ is the quantization noise of sub-ADC1. We have

$$\Delta \cdot Y = \mathrm{STF_1X} + \mathrm{NTF1E_1} + \mathrm{CTF_1C_1} \tag{19}$$

$$\mathrm{STF_1} = \frac{H_1H_2}{1 + z^{-1}H_2 + z^{-1}H_1H_2} \tag{20}$$

$$\mathrm{NTF_1} = \frac{1}{1 + z^{-1}H_2 + z^{-1}H_1H_2} \tag{21}$$

$$\mathrm{CTF_1} = \frac{H_2}{1 + z^{-1}H_2 + z^{-1}H_1H_2} \tag{22}$$

The sub-ADC1 output $y[k]$ is a summation of the input $x[k]$ shaped by the signal transfer function $\mathrm{STF_1}$, the sub-ADC1 quantization noise $e_1[k]$ shaped by the noise transfer function $\mathrm{NTF_1}$, and the calibration signal $c_1[k]$ shaped by

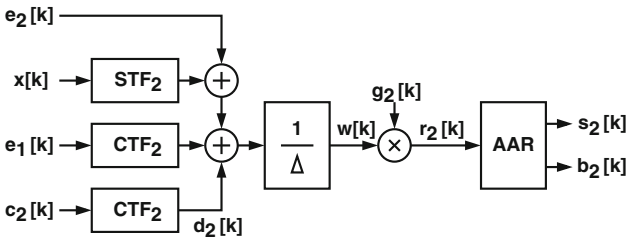


Fig. 17 Calibration signal flow diagram for β_2 calibration

$\mathrm{CTF_1}$. The sub-ADC1 has a conversion gain of $1/\Delta$. The calibration signal $c_1[k]$ go through the $\mathrm{CTF_1}$ filter, yielding $d_1[k]$. Thus, embedded in $y[k], d_1[k]$ is the step response of $\mathrm{CTF_1}$ triggered by $c_1[k]$. This step response settles toward a final value of

$$V_{cf1} = V_{c1} \times \mathrm{CTF_1}|_{z=1} \approx V_{c1} \times \frac{1 - \beta_1}{\alpha_1} \tag{23}$$

This V_{cf1} value is used to detect β_1. The calibration processor CP1 masks $y[k]$ with $g_1[k]$ to extract only the valid V_{cf1} information. It then uses the AAR processing to diminish the calibration fluctuation caused by $x[k]$ and $e_1[k]$. The CP operation is identical to those described in Sect. 4. Following the design considerations outlined in Sect. 4, we choose $f_{q1} = f_s/32, D_{g1} = 7/16, V_{c1} = 0.1\Delta$, $\Delta\beta_1 = 0.01$, and Nth1 = 96. The resulting time constant is $\tau_1 = 176421$ sampling periods.

To calibrate β_2, a calibration signal $c_2[k] = q_2[k] \times V_{c2}$ is injected to the input of sub-ADC1. The output of the 1st integrator is digitized by an extra ADC, sub-ADC2, yielding $w[k]$. For this design case, sub-ADC2 is a single comparator. A calibration processor, CP2, takes $w[k]$ and generates control signal $T_2[k]$ to adjust β_2 of the 2nd integrator. Design parameters are the calibration signal frequency f_{q2}, the calibration signal amplitude V_{c2}, the $g_2[k]$ signal duty ratio D_{g2}, the BPD threshold Nth2, and the β_2 control step size $\Delta\beta_2$. Figure 17 shows the calibration signal flow diagram, where $e_1[k]$ is the quantization noise of sub-ADC1 and $e_2[k]$ is the quantization noise of sub-ADC2. We have

$$\Delta \cdot W = E_2 + \mathrm{STF_2X} + \mathrm{CTF_2\,(E_1 + C_2)} \tag{24}$$

$$\mathrm{STF_2} = \frac{H_1 + z^{-1}H_1H_2}{1 + z^{-1}H_2 + z^{-1}H_1H_2} \tag{25}$$

$$\mathrm{CTF_2} = \frac{-z^{-1}H_1}{1 + z^{-1}H_2 + z^{-1}H_1H_2} \tag{26}$$

The sub-ADC2 output $w[k]$ is a summation of the input $x[k]$ shaped by the signal transfer function $\mathrm{STF_2}$, the sub-ADC1 quantization $e_1[k]$ shaped by $\mathrm{CTF_2}$, the sub-ADC2 quantization $e_2[k]$, and the calibration signal $c_2[k]$ shaped by $\mathrm{CTF_2}$. The sub-ADC2 has a conversion gain of $1/\Delta$. The calibration signal $c_2[k]$ go through the $\mathrm{CTF_2}$ filter, yielding

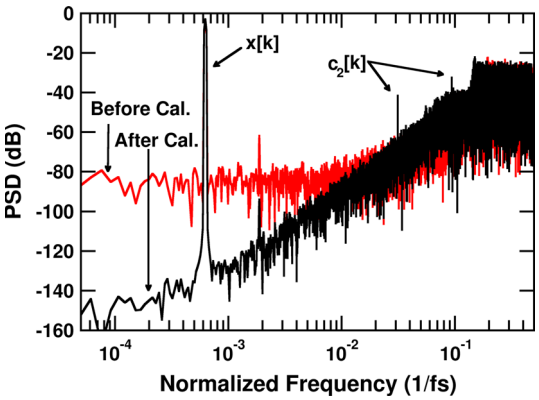


Fig. 18 Output spectra of the 2nd-order DSM design case

$d_2[k]$. Thus, embedded in $w[k], d_2[k]$ is the step response of CTF_2 triggered by $c_2[k]$. This step response settles toward a final value of

$$V_{cf2} = V_{c2} \times \mathrm{CTF}_2|_{z=1} \approx V_{c2} \times -\frac{1-\beta_2}{\alpha_2} \tag{27}$$

This V_{cf2} value can be used to detect β_2. The CP2 operation is similar to the CP1 operation. Note that V_{cf2} is negative, while V_{cf1} is positive. Thus, referring to Fig. 9, the polarity of $g_2[k]$ is inverted. To simplify design, $c_2[k]$ is identical to $c_1[k]$ and CP2 is identical to CP1. The design parameters $f_{q2}, D_{g2}, V_{c2}, \Delta\beta_2$, and Nth2 are identical those for $c_1[k]$ and CP1.

Figure 18 shows the DSM output spectra before and after calibration. The DSM input bandwidth is 2 MHz and the sampling frequency is $f_s = 256\,\mathrm{MHz}$. The input is a sine wave with a frequency of $(41/2^{16})f_s$ and an amplitude of $-3\,dBFS$. The resulting SQNR is 52 dB before calibration, and is improved to 72 dB after calibration. The SFDR is improved from 57.71 to 87.25 dB by the calibration. The calibration time of $2 \times 3\tau_1 = 4.1\,\mathrm{msec}$ is required for both β_1 and β_2 to converge from 0.9 to 0.995.

6 Calibration of high-order DSMs

The proposed calibration can be applied to DSMs of any structure. Figure 19 is a DSM containing P cascaded integrators with distributed feedback (CIFB). The j-th integrator, where $j = 1, \ldots, P$, is modeled as

$$H_j(z) = \frac{\alpha_j}{1-\beta_j z^{-1}} \quad \text{or} \quad \frac{\alpha_j z^{-1}}{1-\beta_j z^{-1}} \tag{28}$$

The calibration corrects the β of the integrators one at a time. To calibrate the j-th integrator, $H_j(z)$, a calibration signal $c[k]$ is injected at the input of the $(j+1)$-th

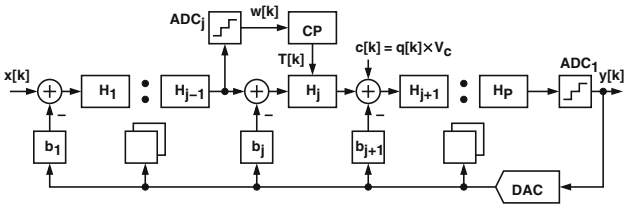


Fig. 19 Calibration of a CIFB DSM

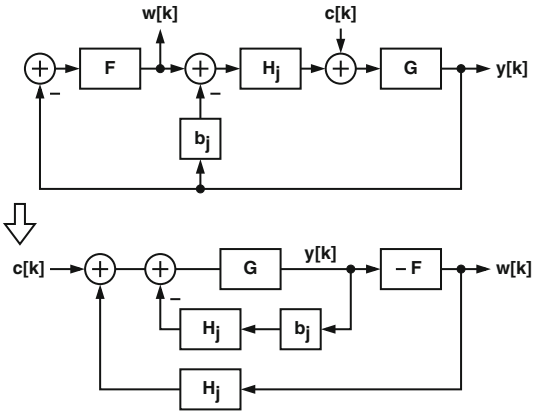


Fig. 20 $c[k]$-to-$w[k]$ signal flow in a CIFB DSM

integrator, while the output of the $(j-1)$-th integrator is digitized as $w[k]$ and send to the calibration processor (CP). The CP output $T[k]$ adjusts the β of the j-th integrator.

Figure 20 shows the $c[k]$-to-$w[k]$ signal flow, in which $x[k]$ and the quantization errors generated by the sub-ADCs are neglected. The function $F(z)$ is the transfer function from $y[k]$ to $w[k]$. It involves integrators from H_1 to H_{j-1}. The function $G(z)$ is the transfer function from $c[k]$ to $y[k]$. It involves integrators from H_{j+1} to H_P but without the contribution from $H_j(z)$. In the bottom half of Fig. 20, the signal flow is redrawn so that $F(z)$ and $G(z)$ are in the forward signal path and $H_j(z)$ and $b_j H_j(z)$ are the feedback paths. The $c[k]$-to-$w[k]$ transfer function $\mathrm{CTF_j(z)} \equiv \mathrm{W(z)/C(z)}$ is

$$\mathrm{CTF_j(z)} = \frac{-\mathrm{F(z)G(z)}}{\mathrm{H_j(z)F(z)G(z) + b_j H_j(z)G(z) + 1}} \tag{29}$$

Since the signal path of $F(z)$ is a cascade of integrators, its dc gain $F(z)|_{z=1} = F(1)$ is much larger than 1. Then, the dc gain of $\mathrm{CTF_j(z)}$ can be approximated by

$$\mathrm{CTF_j(1)} \approx -\frac{1}{\mathrm{H_j(1)}} = -\frac{1-\beta_j}{\alpha_j} \tag{30}$$

We design $c[k]$ as a square wave with an amplitude of V_c. In each $c[k]$ cycle, the step response of $\mathrm{CTF_j(z)}$ is embedded in $w[k]$. We design the $c[k]$ period to be long

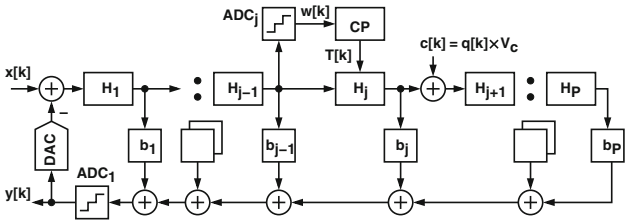


Fig. 21 Calibration of a CIFF DSM

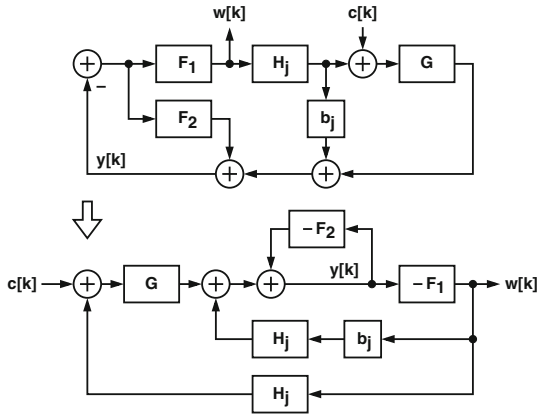


Fig. 22 $c[k]$-to-$w[k]$ signal flow in a CIFF DSM

enough so that the step response can settle toward its final value, which is $V_{cf,j} = V_c \times -(1-\beta_j)/\alpha_j$. The CP extracts $V_{cf,j}$ to determine the polarity of $1-\beta_j$, and then adjusts β_j to make it approache 1.

To calibrate the 1st integrator, $H_1(z)$, the calibration signal $c[k]$ is injected to the input of the 2nd integrator and the DSM regular digital output $y[k]$ is used as the CP input. The corresponding $c[k]$-to-$y[k]$ signal flow is similar to those shown in 20, but without the $-F(z)$ block and the outer H_j feedback path. The $c[k]$-to-$y[k]$ transfer function is

$$\mathrm{CTF_1(z)} = \frac{\mathrm{Y(z)}}{\mathrm{C(z)}} = \frac{\mathrm{G(z)}}{1 + \mathrm{b_1 H_1(z) G(z)}} \tag{31}$$

Since $b_1 H_1(1) G(1) \gg 1$, the dc gain of $\mathrm{CTF_1(z)}$ can be approximated by

$$\mathrm{CTF_1(1)} \approx \frac{1}{\mathrm{b_1 H_j(1)}} = \frac{1-\beta_1}{\mathrm{b_1}\alpha_1} \tag{32}$$

When $c[k]$ is applied, the final value of the $\mathrm{CTF_1(z)}$ step response is $V_{cf,1} \approx +V_c(1-\beta_1)/(b_1\alpha_1)$. The polarity of $V_{cf,1}$ is different from that of $V_{cf,j}$ with $j \neq 1$.

Figure 21 is a DSM containing P cascaded integrators with distributed feedforward summation (CIFF). Similar to the CIFB DSM shown in Fig. 19, to calibrate the j-th integrator, $H_j(z)$, a calibration signal $c[k]$ is injected at the input of the $(j+1)$-th integrator, while the output of the $(j-1)$-th integrator is digitized as $w[k]$ and send to the calibration processor (CP). The CP output $T[k]$ adjusts the β of the j-th integrator. Figure 22 shows the $c[k]$-to-$w[k]$ signal flow, where

$$\begin{aligned} F_1(z) &= H_1(z) \times H_2(z) \times \ldots \times H_{j-1}(z) \\ F_2(z) &= b_1 H_1(z) \times b_2 H_2(z) \times \ldots \times b_{j-1} H_{j-1}(z) \\ G(z) &= b_{j+1} H_{j+1}(z) \times b_{j+2} H_{j+2}(z) \times \ldots \times b_P H_P(z) \end{aligned} \tag{33}$$

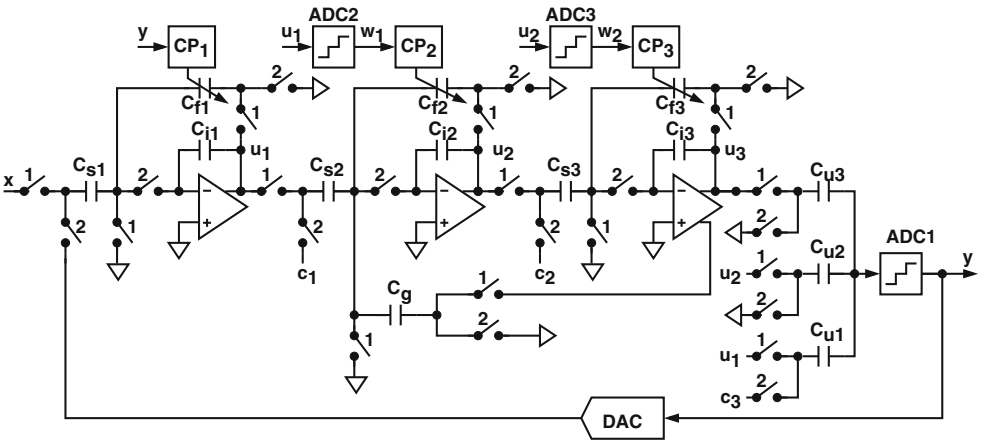
From Fig. 22, it can be shown that $\mathrm{CTF_j(1)} \approx -1/\mathrm{H_j(1)}$ for $j \geq 2$ and $\mathrm{CTF_1(1)} \approx +1/\mathrm{H_1(1)}$.

The proposed calibration technique can correct the β of all integrators in a DSM. It calibrates each individual integrator one at a time. Although a square wave is injected into the DSM for calibration, its effect on the DSM is minuscule. The calibration itself is robust. It can easily converge as long as the amplitude of the square-wave calibration signal $c[k]$ is sufficiently large. It does not require high-precision analog circuitry, and does not require cumbersome digital circuitry such as narrow-band filters. It can tolerate the non-linearity of the sub-ADCs. The design procedures for the proposed calibration scheme are similar to those described in Sects. 4 and 5.

7 Third-order DSM design case

A third-order CIFF DSM is simulated to demonstrate the proposed scheme. Figure 23 shows the DSM, which is designed in a 65 nm CMOS technology with a 1 V supply voltage. The entire circuit is fully differential. ADC1 and DAC are 2-bit to increase system stability. ADC1 comprises three comparators with thresholds of $\{0, \pm 2/9\,\mathrm{V}\}$. The output swing of DAC is ± 1 V. Signal scaling and feedforward paths are used to relax the linearity requirements of integrators. A passive SC adder preceding ADC1 combines the feed-forward paths. All of the integrators use single-stage inverter-based opamps [13]. Figure 24 shows the opamp schematic. The channel lengths of the MOSFETs are chosen to be 60 nm. The resulting dc gain is 8.4 and the gain-bandwidth is 3.9 GHz with a capacitive load of 4 pF. The DSM is operated at 640 MHz with OSR = 32. Its input bandwidth is 10 MHz.

To calibrate the first integrator H_1, the calibration signal c_1 is injected into to the second integrator H_2, and $\mathrm{CP_1}$ receives the data stream y from ADC1. To calibrate H_2, c_2 is injected to the input of the third integrator H_3, and the output u_1 from H_1 is quantized by ADC2 and sent to $\mathrm{CP_2}$. To calibrate H_3, c_3 is injected to the input of ADC1, and the output u_2 from H_2 is quantized by ADC3 and sent to $\mathrm{CP_3}$. Both ADC2 and ADC3 are 2-bit. The compensation



C_{s1}	C_{i1}	C_{s2}	C_{i2}	C_{s3}	C_{i3}	C_g	C_{u1}	C_{u2}	C_{u3}
3.981 pF	10.179 pF	976 fF	595 pF	354 fF	1013 fF	16 fF	140 fF	90 fF	80 fF

Fig. 23 A third-order CIFF DSM with local resonator feedback

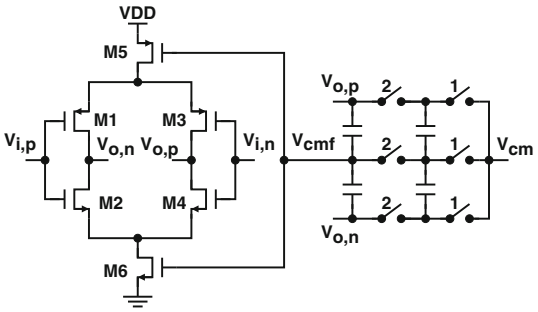


Fig. 24 Inverter-based opamp with common-mode feedback

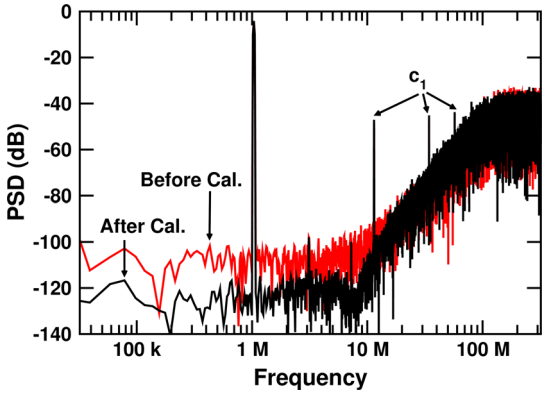


Fig. 25 Output spectra of the 3rd-order CIFF DSM design case

capacitor C_{f1} comprising a 5-bit capacitor bank can vary from 0 to 837 fF. Capacitor C_{f2} comprising a 4-bit capacitor bank can vary from 0 to 240 fF. Capacitor C_{f3} comprising a 4-bit capacitor bank can vary from 0 to 90 fF. The calibrations are performed sequentially and run in the background during the DSM operation. Calibration signals c_1, c_2, and c_3 are identical, with a frequency of 11.43 MHz and an amplitude of 0.01 V. All CPs have $D_g = 2/7$ and $N\text{th} = 96$. The calibration time, for each β to converge, is around 15 msec.

Figure 25 shows the output spectra of the DSM from the Spectre® circuit simulation. The input is a sine wave with a frequency of 1.035 MHz and an amplitude of 0.625 V. The standard variation of the outputs of all integrators is around 0.1 V. Before calibration, the quantization noise leaks into the input band and the SNDR is 73 dB. After calibration, the noise floor drops and a notch appears at 8 MHz. The SNDR is increased to 87.3 dB and the SNR

The power consumption of this DSM excluding CPs is 21 mW. The integrators consume 14.7 mW. ADC1, DAC, and the adder consume 4.1 mW. ADC2 and ADC3 consume 2.2 mW. This design reveals that the proposed technique can correct the NTF whether their zeros are placed at dc or not.

8 Conclusions

Lossy integrators in a DSM degrade the SQNR. This paper proposes a calibration technique to correct the integration leakage of the SC integrators in a DSM of any form. Although the integrators are embedded in a DSM, they can be calibrated one at a time without interrupting the normal DSM operation. Since each integrator is calibrated separately, the design parameters of the corresponding calibration signal and calibration processor can be easily optimized.

This calibration technique has been used to design a 81-dB dynamic range 16-MHz bandwidth DSM chip [14]. This chip was fabricated using a 65 nm CMOS technology. It can operate at 1.1 GHz clock rate under a 1-V supply. To maximize speed, all MOSFETs in the opamps are sized with the minimum channel length of 60 nm, resulting in an opamp dc voltage of 10.

The proposed calibration technique enables the use of low-gain opamps in wide-band high-resolution discrete-time DSMs. It is especially suitable for ultra-high-speed DSMs in advanced nanoscale CMOS technologies. It facilitates the use of amplifiers optimized for speed regardless of their dc gain.

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