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Sub-100 nm ALD-assisted nanoimprint lithography for realizing vertical organic transistors with high ON/OFF ratio and high output current

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ABSTRACT

We introduced a conformal atomic-layer-deposited aluminum oxide layer to cover the imprint mold to reduce the feature size and to strengthen the mold durability. A nano-hole array pattern with diameter down to 85 nm was successfully transferred to sample substrate to fabricate a vertical organic transistor. The *Imprint* vertical organic transistor exhibited high output current density as 4.35 cm^2/V s and high ON/OFF current ratio as 11,000 at a low operation voltage as 1.5 V.

1. Introduction

Compared to the traditional amorphous-silicon thin film transistors (a-Si TFTs), the solution-processed organic transistors are promising for the development of low-cost and large-area electronic devices on flexible substrates [1]. Since the high operation voltage caused by long channel length of the conventional transistor would bring about high power consumption, the organic transistors with vertical channels were introduced to lower down the operation voltage [2]. In the previous work, we reported that a vertical-channel solution-processed organic transistor, named space-charge-limited transistor (SCLT), showed promising transistor characteristics such as higher output current (>10 mA/cm^2) at 2 V operation voltage [3,4]. As shown in Fig. 1(a), the carriers are injected into the vertical organic semiconductor channel by an emitter, passing through the holes on the base, and finally being collected by the collector. Base electrode controls the potential profile in vertical channel to turn on or turn off the transistor. The colloidal lithography was then employed to make the base electrode in SCLT with a hope of its potential mass production. However, colloidal lithography used in our previous work might not be compatible with existing commercialized process tools, and even worse the inevitable random accumulation of nanospheres during the process could incur large holes on the base electrode of SCLT, causing leakage current and made it difficult to have uniform leakage control [3]. A solution to completely removing such accumulation was to use nano-imprint lithography (NIL). The SCLT made by using NIL exhibited an ON current

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of 0.35 mA/cm^2 and an ON/OFF current ratio of around 3000 at 1.8 V [5]. It was noted that the hole diameter of base electrode was the key parameter in determining the ON/OFF current ratio of an SCLT [6,7]. Base control ability was improved with reduced hole diameter and hence the off state current was decreased. Additionally, it is apparent that the larger the area of holes array pattern, the more SCLTs can be accommodated, which benefits the mass production. However, the sub-100 nm resolution NIL usually requires e-beam lithography to generate the imprint mold, which is expensive and low-throughput especially when a large area is to be patterned. Interference lithography (IL) can fabricate large-area, periodic nano-holes array patterns in much shorter time [8]. The period of IL is governed by $\Lambda = \lambda/2\sin\theta$, where Λ is the pattern period, λ the wavelength of light source, and θ the incident angle of light. Therefore, the inherent linewidth is limited; for example, it will not be smaller than 91 nm if a light source in 364 nm wavelength is used. To overcome this limit, in this work we will introduce a novel method which combines low-temperature atomic layer deposition (ALD) and IL to fabricate a sub-100 nm resolution hole-array photoresist (PR) pattern NIL mold. The PR structure coated with aluminum-oxide layer can be directly used as an imprint mold. By employing this method, the ON current of SCLT can increase to 4.35 mA/cm^2, 10 times more than before, and the ON/OFF current ratio can have a 300% increase to be greater than 10^4.

2. Experimental

The process steps to fabricate stamp and to produce Imprint SCLT are illustrated in Fig. 1(b) and (c), respectively.

(1) Stamp fabrication: Firstly, a mold on silicon substrate was prepared. The 175-nm-thick antireflection coating (ARC, from Nissan Chemical XHRiC-11, baked at 175 °C for 1 min) and the 200-nm-thick photoresist (ULTRA-i™ 123, ©Rohm and Haas Electric Materials, soft baked at 90 °C for 90 s) were coated on the silicon substrate. ARC was used to suppress the light reflection from bottom interface and hence to avoid the standing wave effect. Two-beam interference lithography with two-time 90-degree exposure was then used to produce a periodic hole array photoresist pattern [8]. Then, after a hard bake at 120 °C for 90 s, an aluminum-oxide (Al_2O_3) film was grown by atomic layer deposition at 130 °C to cover the photoresist. The thickness of the Al_2O_3 film was controlled by the cycle number in ALD process. In our ALD system (purchased from Syskey Technology LTD.), the Al_2O_3 was grown by using trimethylaluminum (TMA) and H_2O vapor as precursors. One cycle grows about 3-nm-thick Al_2O_3. The Al_2O_3-covered mold was then immersed into *trichloro*(3,3,3-*trifluoropropyl*)*silane* (FPTS, from Sigma–Aldrich, 0.01 mol/L in toluene) for 12 h to reduce the surface energy of the mold [9]. Then, the stamp with a bi-layered structure was formed on the mold. The bottom layer was a hard poly(dimethylsiloxane) (*h*-PDMS) and the top layer was a conventional PDMS. The *h*-PDMS solution was a mixture of vinyl PDMS prepolymer (2.5 g, VDT-731, Gelest Corp.), Pt catalyst (0.0125 g, platinum divinyltetramethyldisiloxane, SIP 6831.1, Gelest Corp.) modulator (0.0625 g, 2,4,6,8-tetramethyltetravinylcyclotetrasiloxane, 87927, Sigma–Aldrich), and hydrosilaneprepolymer (0.25 g, HMS-301, Gelest Corp.). The former three materials were firstly mixed and degassed for 10 min, then the last one was added into the mixture to finish the *h*-PDMS solution. The *h*-PDMS solution was spin coated onto the mold and baked at 60 °C for 45 min to form a 2-μm-thick *h*-PDMS film. Then, conventional PDMS produced by the mixture of Sylgard 184 A and B (with a ratio as 10 to 1) was poured slowly onto *h*-PDMS film. After baked at 60 °C for 8 h, we slowly demolded the stamp. The stamp was formed by *h*-PDMS/PDMS hybrid structure with periodic rod-array pattern.

(2) SCLT fabrication: as shown in Fig. 1(c), to fabricate SCLT, the layered substrate with anti-reflection coating (ARC, 200 nm)/aluminum metal (40 nm)/polymer insulator (cross-linked poly(4-vinyl phenol), PVP, 300 nm) on an ITO glass substrate was prepared. ITO served as the collector electrode. The cross-linkable PVP (8 wt.%) and cross-linking agent poly(melamine-co-formaldehyde) (PMF) were dissolved in propylene glycol monomethyl ether acetate (PGMEA) with a PVP:PMF mass ratio of 11:4. The solution was spin coated on an ITO glass substrate and annealed at 200 °C for 1 h to form a 300-nm film. After evaporating a 40-nm-thick Al, we spin coated 200-nm-thick ARC on the Al layer without baking, and then flipped the hybrid *h*-PDMS/PDMS stamp on ARC. After covering the stamp with a 125-μm-thick polycarbonate (PC) film, the stamp was imprinted on the substrate with a pressure of 10 kgw/

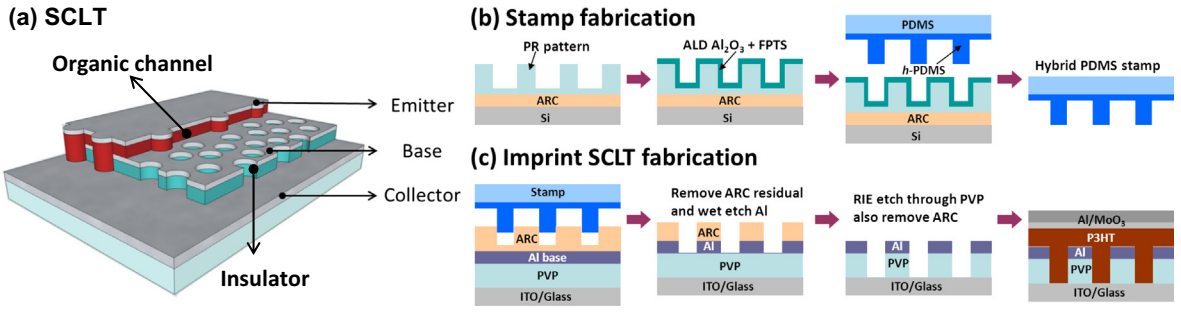

Fig. 1. (a) Schematic diagram of the space-charge-limited transistor (SCLT). Vertical channel is controlled by the base electrode with nano-hole-array pattern. (b) Fabrication process of stamp. (c) Fabrication process of *Imprint SCLT*.

cm^2. The temperature was increased to be 175 °C for 90 s and then reduced to 50 °C. The pressure then was released and the stamp was removed. The sample then exhibited periodic hole array pattern in ARC film. We used reactive ion etching to remove the residual ARC in the holes. By a simple wet etching process with standard aluminum etchant, the nano-hole array was transferred to aluminum metal to form the base electrode. The PVP at the sites without Al coverage was removed by 100 W O_2 plasma, and the PVP cylindrical nano-pores with the depth as 300 nm were formed. Then, a p-type organic semiconducting layer, poly(3-hexylthiophene) (P3HT, in chlorobenzene), was coated to form the active material with 450-nm thickness. Finally, MoO_3 (10 nm) and Al (40 nm) were deposited to serve as the emitter electrode and to complete the SCLT with an active area of 1 mm^2.

3. Results and discussion

3.1. ALD-assisted imprint process

Since the thickness of aluminum layer in an SCLT was around 40 nm, the sidewall thickness of hole-array pattern should be greater than 50 nm to accommodate the tolerance needed for wet etching the aluminum layer. If the diameter of hole was set to be 120 nm, the period of IL pattern would be 170 nm, which was beyond the current capability of our IL system. As described previously the smaller the diameter, the higher ON/OFF current ratio and the higher ON current of SCLT would be expected. The period of our IL-generated pattern was at least 250 nm, therefore, a physical dimension shrinkage method was desired to obtain sub-100 nm hole diameter without reducing the sidewall thickness. One possibility without resorting to immersion lithography or e-beam lithography is the use of using atomic layer deposition (ALD). It is known that ALD has an inherent advantage of being able to deposit ultrathin (~few Å), conformal, and smooth films on a structured surface. It could also be used to accurately adjust the hole's diameter of a hole-array pattern [10–12]. Though the direct use of photoresist structure as part of a device was very rare because of the inherent chemical and physical instabilities of photoresist, the structure could be used as an imprint mold after it was completely sealed by the ALD-made thin film. However, the photoresist (ULTRA-i™ 123, ©Rohm and Haas Electric Materials) we used in this work would melt down around 150 °C. So the low-temperature ALD process instead of the conventional one [13] was used, in which large gas purge and high pressure water vapor [14,15] were applied to the polymer surface. After 10–15 cycles of ALD process, an aluminum-oxide (Al_2O_3) film with 40–50 nm thickness with good uniformity was formed on the PR pattern. The SEM images of the mold (with PR pattern) before and after the growth of 50-nm ALD Al_2O_3 were shown in Fig. 2(a) and (b), respectively. The diameter of the hole in the pattern was reduced by 50% after ALD Al_2O_3 coverage. Note that the sidewall of holes-array pattern also became thicker, which increased the subsequent process tolerance.

3.2. Imprint process and mold releasing

Poly(dimethylsiloxane) (PDMS) was used as a stamp to transfer the pattern from the mold to the substrate in our hot embossing NIL. However, the resolution of conventional PDMS (Sylgard® 184, ©Dow Corning) stamp was not good enough for sub-100 nm NIL process [16]. The *h*-PDMS, a harder elastomer suitable for NIL was introduced. The stamp material was composed of vinylmethyl copolymers and hydrosilane components (agent A) and some additional glass fillers (agent B), which were found to be the best candidates for high-resolution NIL [17]. The *h*-PDMS was more fragile than the conventional PDMS, and easily broken during the hot embossing NIL process. To overcome this problem, we used a thick, flexible PDMS slab as a buffer layer to support the thin, stiff *h*-PDMS under layer. Such a hybrid PDMS imprint stamp was easy to handle and released from the mold during preparation [18].

It was found that, however, the large friction between *h*-PDMS and Al_2O_3 often caused structural damage of the stamp when peeled off from the mold. Such damages could be prevented by immersing the *h*-PDMS mold in the toluene solution with *trichloro*(3,3,3-*trifluoropropyl*)*silane* (FPTS) as solvent. FPTS capable of reducing surface energy served as an anti-adhesion self-assembled monolayer [9]. The effectiveness can be clearly seen in Fig. S1 in supporting information when FPTS was applied.

We successfully fabricated a large-area, sub-100 nm hole-array pattern on an aluminum substrate as an etch mask with the help of ALD and *h*-PDMS stamp. The top-view and cross-sectional view SEM images of the hole-array pattern on a substrate with layered aluminum/PVP/ITO/glass were shown in Fig. 3(a) and (b), respectively. The aspect ratio and sidewall thickness of the pattern were good enough to endure the removing process of residual layer. This fabrication method is expected to be much less expensive and time saving as compared to the use of conventional e-beam lithography.

3.3. Durability

The imprint mold is generally made from Si, SiO_2, or other rigid materials. A PR layer was usually used as a sacrificial etch mask and then completely removed after the pattern was transferred from the PR layer to the rigid substrate by using etching method. However, it is known that fine-tuning the profile of etched pattern is hard during mold fabrication, especially for the high aspect ratio pattern. In contrast, fine-tuning the profile of PR pattern is much easier. The Al_2O_3 thin film on the PR surface is hard and tough enough to protect the inner polymer structure [19]. Since oxygen, moisture and other components in the air were isolated from the inner PR structure, the lifetime of pattern would be prolonged. The ALD-assisted Al_2O_3-covered PR pattern could therefore be directly used as an imprint mold with good profile control. Fig. 4 shows

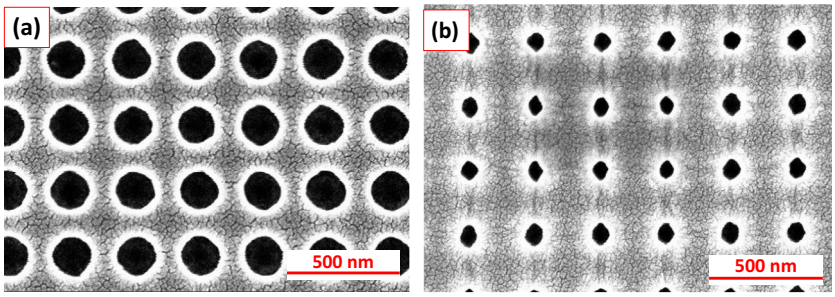

Fig. 2. SEM images of (a) PR pattern before growing ALD Al_2O_3. (hole diameter = 180 nm) and (b) PR pattern after growing ALD Al_2O_3. (hole diameter = 85 nm).

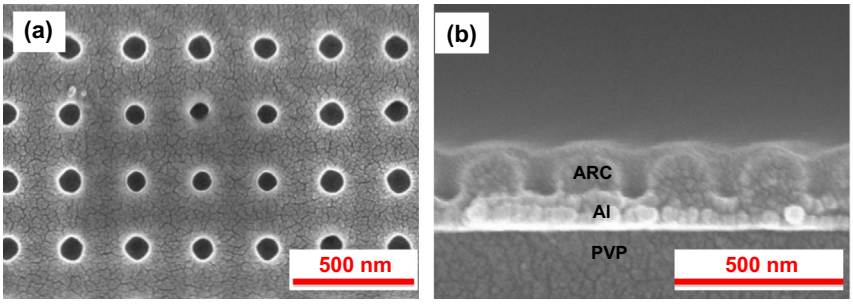

Fig. 3. (a) Top view and (b) cross-sectional SEM images of imprint nano-hole array pattern on Al substrate.

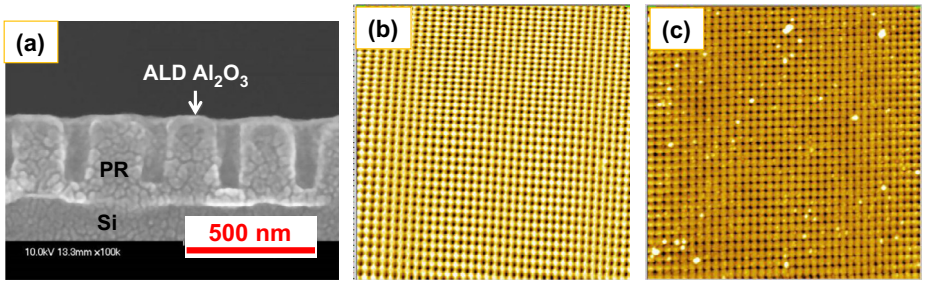

Fig. 4. (a) The cross-sectional SEM image of an ALD-covered mold. AFM images of (b) a new mold and (c) the same mold after more than 30 times for imprint use. The AFM images cover $10 \times 10\ \mu m^2$.

good mechanical durability when a new stamp was used more than 30 times for imprinting. The defects in Fig. 4(c) were resulted from the unprotected storage environment of the mold.

3.4. Pore diameter control

The ALD-assisted nanoimprint can be used not only to reduce the pore diameter, but also to adjust the pore size by simply controlling the ALD depositing cycles. To examine the ability to control the pore size by changing the ALD depositing cycles, we demonstrated the nanoimprint results by changing the ALD Al_2O_3 depositing cycle numbers and the resulting Al_2O_3 thickness. When the Al_2O_3 thickness is around 45–50 nm, the SEM images of the pristine mold, the Al_2O_3-covered mold, and the imprinted pattern on ARC film were shown in Fig. 5(a)–(c), respectively. When Al_2O_3 thickness reduces to be around 8–10 nm, the SEM images of the pristine mold, the Al_2O_3-covered mold, and the imprinted pattern on ARC film were shown in Fig. 5(d)–(f), respectively. Compare Fig. 5(c) and (f), by changing the ALD-Al_2O_3 thickness, we successfully obtained a nanoimprinted pore array with the pore diameter modulated from about 85 nm (Fig. 5(c)) to about 125 nm (Fig. 5(f)).

3.5. Imprint transistor

Finally, the hybrid stamp transferred from an ALD-covered mold was used to produce the space-charge-limited transistor (SCLT) by following the process steps illustrated in Fig. 1(c). It is noted that, as shown in Fig. 3, the ALD-assisted imprint process produced sub-100 nm hole array on aluminum film. The hole pattern was then transferred

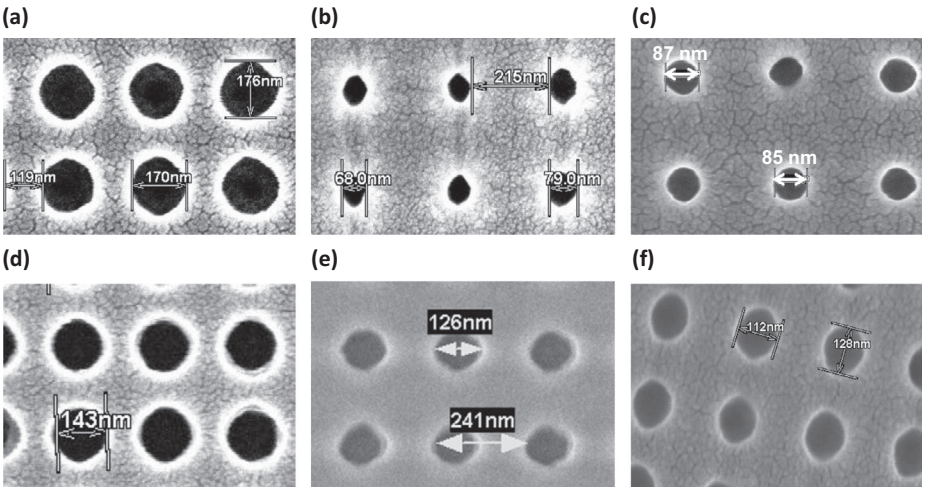

Fig. 5. When the Al_2O_3 thickness is around 45–50 nm, the SEM images of (a) the pristine mold, (b) the Al_2O_3-covered mold, and (c) the imprinted pattern on ARC film. When the Al_2O_3 thickness is around 8–10 nm, the SEM images of (d) the pristine mold, (e) the Al_2O_3-covered mold, and (f) the imprinted pattern on ARC film.

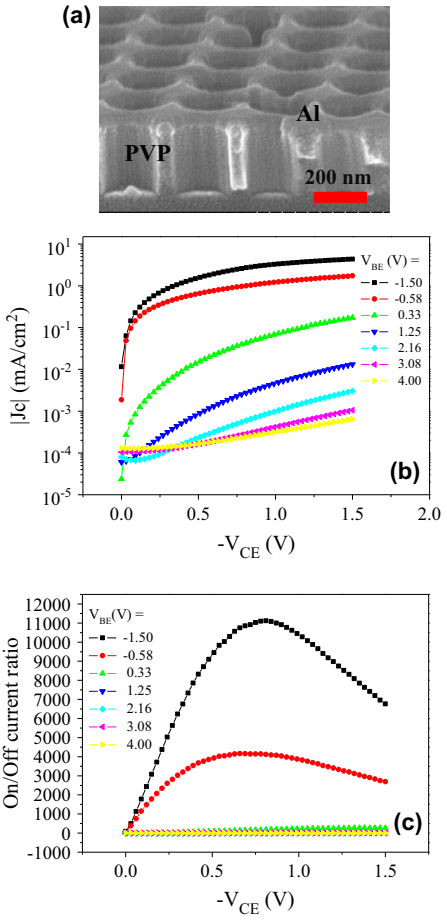

Fig. 6. (a) SEM image of SCLT substrate after the PVP etching-through process. (b) The output current density J_C as a function of V_{CE}. Different V_{BE} is applied to turn on or turn off the SCLT. (c) The ON/OFF current ratio as a function of V_{CE}.

to aluminum by wet etching process. The underlying PVP layer was etched through by oxygen plasma to form cylinder-like vertical channels as shown by the SEM image in Fig. 6(a). Due to the aluminum wet etching process, the diameter of the vertical channels was increased to be around 200 nm. The collector current density (J_C) as a function of collector to emitter voltage (V_{CE}) is plotted in Fig. 6(b). When base to emitter voltage (V_{BE}) was −1.5 V and V_{CE} was −1.5 V, output current density as high as 4.35 mA/cm^2 could be obtained. Such a current density was 10 times larger than our previous reported *Imprint SCLT* [5]. The ON/OFF current ratio was also plotted as a function of V_{CE} in Fig. 6(c). When V_{CE} was −0.5 V to −1 V, ON/OFF ratio higher than 10,000 was obtained and the off state current density was around 2–5 × 10^{-4} mA/cm^2, which corresponded to 20–50 pA when the active region was 100 μm × 100 μm. In our previous reported *Imprint SCLT*, ON/OFF ratio was 3000 and the output current was only 0.35 mA/cm^2. Here in this work, the 200-nm channel diameter successfully improved the transistor performance. The transfer characteristic, the collector current density (J_C) as a function of base to emitter voltage (V_{BE}), was also shown in Fig. S2(a) in supporting information. The calculated transconductance (gm) and the current gain (J_C/J_B) were plotted as a function of V_{BE} in Fig. S2(b). In on state region, the current gain was between 465 to 5000 and the transconductance was around 40 mS. When V_{BE} was −1.5 V and V_{CE} was −1.5 V, base leakage current was increased (10^{-2} cm^2/V s). In future work, a good insulator surrounding the base electrode is required to suppress the base leakage current and to lower down the power consumption. Here, in this work, the large output current density and the high ON/OFF ratio satisfy the basic requirement for OLED driving.

The influence of pore size on transistor performance was also investigated by using Silvaco TCAD simulator. The simulated transfer characteristics of SCLT with pore

diameter as 300 nm, 200 nm, and 100 nm were compared in Fig. S3 in supporting information. When the pore diameter decreased, an improved switching property was obtained due to the enhanced base control ability. The simulated off-state current, however, was much smaller than the experimental off-state current. This is because that, in real cases, the leakage current in PVP layer was around 10^{-3} to 10^{-4} mA/cm^2. Hence, as shown in Fig. 6(b), the minimum off-state current of SCLT was around 10^{-3} to 10^{-4} mA/cm^2. Even though there was some difference between the simulated and experimental results, the simulation curves verified the pore diameter effect as well as the switching and amplification function of the proposed SCLT.

4. Conclusion

We demonstrated high performance vertical channel organic transistor by using ALD-assisted nano-imprint technology. A conformal aluminum oxide layer grown by atomic layer deposition covered the imprint mold to reduce the feature diameter from 180 nm to 85 nm. With the reduced feature size, imprinted nano-hole array was used to reduce the diameter of vertical channel. The reduction of channel diameter could significantly enhance base electrode control over the vertical channel and hence greatly improve transistor ON/OFF current ratio. Together with high enough output current density and low production cost, the proposed imprint vertical organic transistor is promising for applications such as flexible electronics and organic-light-emitting-diode driving.

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Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.orgel.2014.10.008.

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