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High performance AlInN/AlN/GaN p-GaN back barrier Gate-Recessed Enhancement-Mode HEMT

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ABSTRACT

In the present work, we propose and perform extensive simulation study of the novel device structure having a p-GaN back barrier layer inserted in the conventional AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT device for reducing the short channel effects, gate leakage and enhancing the frequency performance. The influence of the p-GaN back barrier layer on the device performance of the newly proposed structure is done using 2D Sentaurus TCAD simulations. The simulations use Drift–Diffusion (DD) model, Masetti and Canali model, which are calibrated/validated with the previously published experimental results. Simulation are done to analyze the transfer characteristics, transconductance (g_m), Gate leakage current (I_g), drain induced barrier lowering (DIBL), subthreshold slope (SS), threshold voltage (V_{th}), On-current Off-current ratio (I_{on}/I_{off}), gate capacitance (C_{gg}) and cut off frequency (f_T) of the proposed device. A comparison is done between the device without back barrier layer and the proposed device with p-GaN back barrier layer. Use of p-GaN back barrier layer helps to achieve a higher positive V_{th} due to the depletion effect, reduced I_g, reduced DIBL, prevents degradation of SS and helps to increase the f_T. Very impressive f_T up to 123 GHz, as compared to 70 GHz for the device without back barrier. These results indicate that AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT structure with p-GaN back barrier is a promising candidate for microwave and switching application.

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1. Introduction

The AlInN/GaN-based high electron mobility transistor (HEMT) has emerged as superior alternative to the conventional AlGaN/GaN HEMT for high-power, high-frequency applications [1–3]. The AlInN/GaN heterostructure is gaining importance due to several structural advantages over AlGaN/GaN heterostructure. Lattice matching by using 17% of indium in AlInN i.e. $Al_{0:83}In_{0:17}N$/GaN [1] avoids stress at the interface, which helps to improve the device's reliability [4,5]. Another advantage is that strong spontaneous polarization existing in an AlInN/GaN heterostructure induces a higher two-dimensional electron gas (2DEG) density in the channel [2], which implies radio-frequency (RF) performances could be much improved by scaling down gate length as well as the AlInN barrier thickness [6,7]. Taking the advantage of these material properties, excellent performance has been reported for the AlInN/GaN HEMT devices over past decade. Wang et al. reported very high drain current (I_d) of 2.5 A/mm for 100-nm gate length AlInN/GaN HEMT having a 6.9-nm AlInN barrier thickness [4]. Ostermaier et al. presented the recessed gate normally Off InAlN/AlN Barrier HEMT having f_T of 33 GHz. Operation [8]. Wang et al. reported g_m in excess of 800 mS/mm for the Gate-Recessed Enhancement-Mode AlInN/AlN/GaN HEMT device [9]. In 2010, Sun et al. reported a f_T of 205 GHz for the 55 nm gate-length device with an 11-nm-thick AlInN barrier [3]. In addition, stable device operation up to 1000 °C has been reported, which shows the potential of AlInN/GaN HEMT devices for RF applications operating in harsh environments [2].

In order to enhance the high-frequency performance of AlInN/GaN HEMT the gate length needs to be scaled down below 50 nm, and a thin barrier layer of less than 3 nm is required to reduce the short-channel effects. However, immoderate scaling of the top AlInN barrier layer in these devices causes a notable drop in the 2DEG density and leads to serious increase in the gate leakage current [10]. A back-barrier structure is an alternative solution to circumvent the short channel effects without further top-barrier layer scaling. Many other groups have successfully deployed AlGaN back-barrier structure in the AlInN/GaN HEMT structure and significant improvement in DC and RF performance was observed [11,12]. Additionally, the concept of a p-GaN buffer layer in AlGaN/GaN MOSFET was successfully demonstrated by Kim et al. [13]. However, all the reported AlGaN back barrier HEMT devices are depletion mode devices making it difficult to deploy for switching application.

In the present work, we propose and perform the simulation study of a novel p-GaN back barrier Gate-Recessed AlInN/AlN/GaN HEMT structures. This device would support enhancement mode operation, exhibit reduced short channel effects, reduced leakage and higher f_T. In this structure the AlGaN back barrier layer is avoided by doping a small portion of the existing GaN buffer layer with p type material, making it p-GaN back barrier layer. The performance of the proposed device needs to be analyzed comprehensively for checking its viability for high frequency and switching applications. Thus, extensively simulations are done to analyze the performance of the proposed device. The parameters analyzed in the simulation include transfer characteristic, g_m, gate leakage, DIBL, SS, I_{on}/I_{off} and f_T. The results obtained from the simulations are compared with the previously published experimentally data by Wang et al. [9], for the device without p-GaN back barrier.

2. Device description

The structure of the newly proposed p-GaN back barrier AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT on SiC substrate and device without p-GaN Back Barrier are shown in Fig. 1 and Fig. 2 respectively. The p-GaN back barrier device of Fig. 2 has gate length (L_g) of 150 nm, 4.8 nm AlInN barrier, 1 nm AlN spacer layer, 30 nm GaN channel (T_c) is untentionally doped, 100 nm p-GaN back barrier layer and an iron doped GaN semi insulating buffer layer grown on SiC substrate. Both devices are passivated with a 140 nm and 200 nm SiN prior to and after gate definition respectively. The gate consists of Pt/Au (150 nm) metal and having 2 × 75 μm gate width (W_g) and goes up to AlN surface. Source and drain consist of Ti metal and a contact resistance R_c of 0.6 Ω-mm [9] included in simulation. The source/drain regions are doped with a concentration 5E20 cm^3 and have abrupt doping profile at the source and drain ends. Narrow bandgap GaN layer just beneath the wide bandgap AlInN barrier

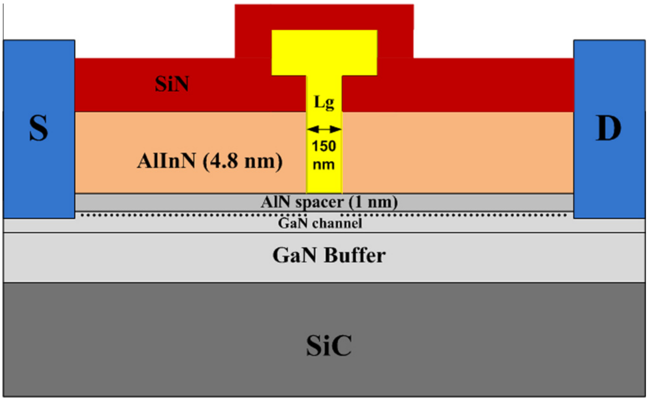

Fig. 1. Cross-sectional view of AlInN/AlN/GaN HEMT structure without p-GaN back barrier. The heterostructure consists of UID narrow bandgap GaN channel and wide bandgap barrier layer of $In_{0.17}Al_{0.83}N$ having width 30 nm and 4.8 nm respectively. Source/drain region doping is 5e10^{20} cm^{3}. The gate length L_g is kept fixed at 150 nm having 2 × 75 µm gate width (W_g).

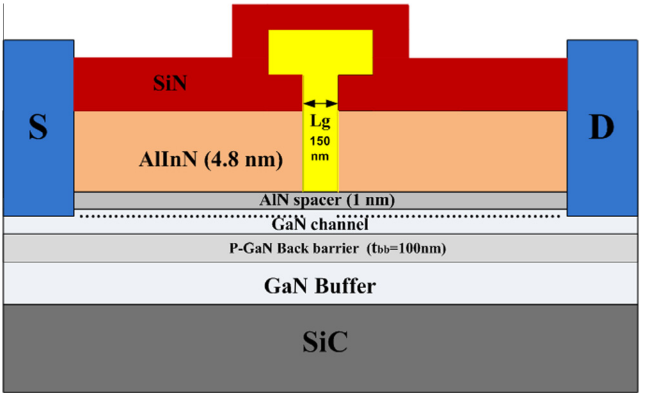

Fig. 2. Cross-sectional view of AlInN/AlN/GaN HEMT structure with p-GaN back barrier. The heterostructure consists of UID narrow bandgap GaN channel and wide bandgap barrier layer of $In_{0.17}Al_{0.83}N$ having width 30 nm and 4.8 nm respectively and the p-GaN back barrier width (t_{bb}) of 100 nm. Source/drain region doping is 5e10^{20} cm3. The gate length L_g is kept fixed at 150 nm having 2 × 75 µm gate width (W_g).

layer, confines the channel at the heterostructure interface. The barrier layer provides a strong carrier confinement in the quantum well at the hetero-interface and the inclusion of an AlN spacer layer to improve the 2DEG mobility [14,15]. In Table 1 the physical properties of narrow bandgap GaN and

Table 1
Physical Properties of $In_{0.17}Al_{0.83}N$ and GaN.

Material	GaN	$In_{0.17}Al_{0.83}N$
Eg (eV)	3.4	4.70
CBO (eV)	0.31	–
VBO (eV)	0.39	–
εo	9.5	11.7
Lattice constant (A)	3.186	3.190
μ_e (cm^2/Vs)	1160	1540
μ_h (cm^2/Vs)	22	82

wide bandgap $Al_{0.83}$ $In_{0.17}N$ are listed. A 100 nm p-GaN back barrier structure is introduced between the unintentionally doped GaN channel and Fe-doped GaN buffer, which is shown in Fig. 2.

3. Simulation model calibration and experimental comparison

In this section we simulated the AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT device shown in Fig. 1 for calibrating the simulation model. The simulated transfer characteristics are compared with the experimentally obtained transfer characteristics from previously published work [9]. The model parameters are tuned to achieve close matching between experimental and simulation results. Once the matching is done, the calibrated simulation model is then applied for simulating the proposed AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT device with p-GaN back barrier.

The simulations are done using Sentaurus TCAD Drift–Diffusion (DD) transport model [16]. The DD model provides relatively fast simulation and runs with an acceptable level of accuracy. As the temperature effects are not analyzed in this work, the Thermodynamic and Hydrodynamic model are not chosen. Several important physical effects such as bandgap narrowing, variable effective mass, doping dependent mobility at high electric fields and spontaneous polarizations are also accounted in simulations.

Though the simulated AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT structure consists of intrinsic semiconductor in all the layers except p-GaN back barrier, there is usually the presence of unintentional doping in GaN-based semiconductors. This unintentionally doped GaN was believed to be *n*-type due to nitrogen vacancies [17]. Thus, due to the presence of this unintentional doping there is a degradation in mobility. To consider the degradation in mobility due to nitrogen vacancies, the Masetti mobility model (Eq. (1)) is introduced in the simulation which accounts for mobility due to impurity scattering in the semiconductor [18]. The degradation in mobility due to nitrogen vacancies could be simulated by placing a light n-type doping (acceptor doping concentration $N_{A,0}$) of 3E16 cm^{-2} in the GaN layer. As the GaN material is *n*-type, the donor doping concentration $N_{D,0}$ is zero in Eq. (1).

$$\boldsymbol{\mu}_{\mathbf{dop}} = \boldsymbol{\mu}_{min1} \boldsymbol{e}^{\frac{\boldsymbol{P_c}}{\boldsymbol{N}_{\boldsymbol{A},0}+\boldsymbol{N}_{\boldsymbol{D},0}}} + \frac{\boldsymbol{\mu}_{\boldsymbol{const}} - \boldsymbol{\mu}_{min2}}{1+\left(\frac{\boldsymbol{N}_{\boldsymbol{D},0}+\boldsymbol{N}_{\boldsymbol{A},0}}{\boldsymbol{c_r}}\right)^{\boldsymbol{\alpha}}} - \frac{\boldsymbol{\mu}_1}{1+\left(\frac{\boldsymbol{c_s}}{\boldsymbol{N}_{\boldsymbol{A},0}+\boldsymbol{N}_{\boldsymbol{D},0}}\right)^{\beta}} \tag{1}$$

The values of the various coefficients and constants in Eq. (1) are given in Table 2, whereas $\boldsymbol{\mu}_{\boldsymbol{const}}$ refers to the constant mobility value given in the constant mobility model [16]. For recombination, the Shockley–Read–Hall (SRH) model is used with SRH, radiative and Auger recombination values of $\boldsymbol{\tau}_{\mathrm{SRH}} = 60$ ns, $C_{rad} = 1.4 \times 10^{-9}$ cm^3/s, $C_{\mathrm{Auger}} = 4 \times 10^{-29}$ cm^6/s [19]. For considering impact ionization, the van Overstraeten–de Man model is implemented.

For considering spontaneous polarization in an AlInN/GaN heterostructure the fixed charge ($\boldsymbol{n_{SP}}$) listed in Table 3 was introduced at each interface [20]. The AlInN/GaN devices are primarily used for high power and high voltage applications due to their large bandgap as well as high electron saturation drift velocity. This drift velocity in such devices would be the limiting factor for the mobility as the device experiences a high electric field condition. Thus, it is necessary to include the Canali

Table 2
The default coefficients for GaN in the Masetti model [18].

Symbol	Electrons	Holes	Units
μ_{min1}	85	33	cm^2/V s
μ_{min2}	75	0	cm^2/V s
μ_1	50	20	cm^2/V s
P_c	6.50×1015	5.00×10^{15}	cm^3
C_r	9.50×1016	8.00×10^{16}	cm^3
C_s	7.20×1019	8.00×10^{20}	cm^3
α	0.55	0.55	–
β	0.75	0.7	–

Table 3
Polarization charge density at each interface [20].

	n_{sp} (GaN) (cm^{-2})	n_{sp} (AlInN) (cm^{-2})	Total (cm^{-2})
SiN/AlInN	–	-4.54×10^{13}	-4.54×10^{13}
AlInN/GaN	-1.81×10^{13}	4.54×10^{13}	2.73×10^{13}

Table 4
Values of *v*–*E* curve parameters for GaN and AlInN used in the simulation.

Parameter	GaN	AlInN
μ_{low} (cm^2/(V s))	800	1417
v_{sat} (10^7 cm/s)	1.8	1.11
β	1.7	1.109

model [21] (high field dependence model) in the simulation. The Canali mobility model used in the simulation is given by Eq. (2). Table 4 summarizes the low field mobility and velocity parameters used in the simulation for GaN and AlInN. These parameters were chosen to match the *v*–*E* curve with the results of [22], as per equation (2). Donor type traps are introduced at the SiN/AlInN interface with the energy of the trap level defined as $E_{c;min}$ (AlInN) minus E_T. The $E_C - E_T = 0.4$ eV and a trap density N_T of 5×10^{13} cm^2 were used to match the simulated and experimental transfer characteristics (Fig. 3). In the simulation GaN buffer bulk trap are considered to be 5×10^{17} cm^{-3} which are defined to be acceptor-like. The effects of a non-uniform distribution of trapped electrons in a direction parallel to the interface are also considered in the simulation, as the current continuity equation and Poisson equation are solved self- consistently [16].

$$\boldsymbol{v}(\mathbf{E}) = \frac{\boldsymbol{\mu}_{\mathbf{low}}}{\left[1 + \left(\frac{\boldsymbol{\mu}_{\mathbf{low}}\mathbf{E}}{\boldsymbol{v}_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{2}$$

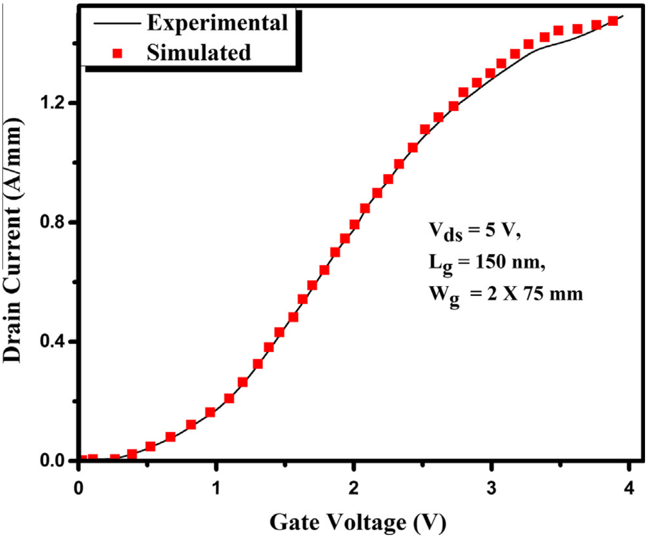

Fig. 3. Experimental (solid lines) and simulated (symbols) transfer characteristics for AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT without p-GaN back barrier after tuning the simulation model, showing very good agreement between the experimental [9] and simulated results.

The simulated transfer characteristics (Fig. 3) of the device shows very good agreement between the experimental results, thus validating our approximation of the carrier transport model and other model parameters. As the model is validated, extensive simulations of the p-GaN back barrier AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT device have been performed.

4. Results and discussion

Fig. 4 shows the transfer characteristics of the 150 nm gate length AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT device (Fig. 2) with 100 nm width p-GaN back barrier with a hole concentration of 1×10^{17} cm^{-3} device. The peak drain current observed was 1.24 A/mm at V_{ds} = 5 V which is lower than the 1.5 A/mm obtained for the device without back barrier (structure shown in Fig. 1). Reduction in drain current for device with p-GaN back barrier is mainly due to lower sheet charge density and higher threshold voltage. The threshold voltage also increases from 0.15 V for device without back barrier to 0.4 V for p-GaN back barrier device. Higher positive threshold voltage is highly desirable for power switching applications [23].

The variation in transconductance (g_m) with gate voltage for devices with and without back barrier is shown in Fig. 5. Higher values of transconductance are highly desirable for CMOS applications. The device with p-GaN back barrier shows the g_m of 589 mS/mm, which is lower than the 704 (mS/mm) obtained for device without back barrier. The main reason for reduction in g_m is the higher access resistance of the p-GaN back barrier device. In addition, the gate voltage swing (GVS), defined as the 10% drop from $g_{m,max}$, is about 0.6 V for both devices, indicating that back barrier approach does not affect the GVS. Broader g_m profile provides an improved linear behavior from which a smaller intermodulation distortion, a smaller phase noise and a larger dynamic range could be expected.

The reverse bias gate current of AlInN/GaN devices can be decomposed into three distinct components i.e., thermionic emission (TE), Poole–Frenkel (PF) emission, and Fowler–Nordheim (FN) tunneling. The PF emission component has strong temperature dependence, whereas FN tunneling component is observed only at low temperatures [16,24]. As we are simulating for room temperature the PF emission component is only considered here. Fig. 6 shows the gate leakage current for the both devices. The leakage of the p-GaN back-barrier is about 10 times lower in magnitude than the device without back barrier. This improvement was expected due to the depletion effect on the undoped-GaN

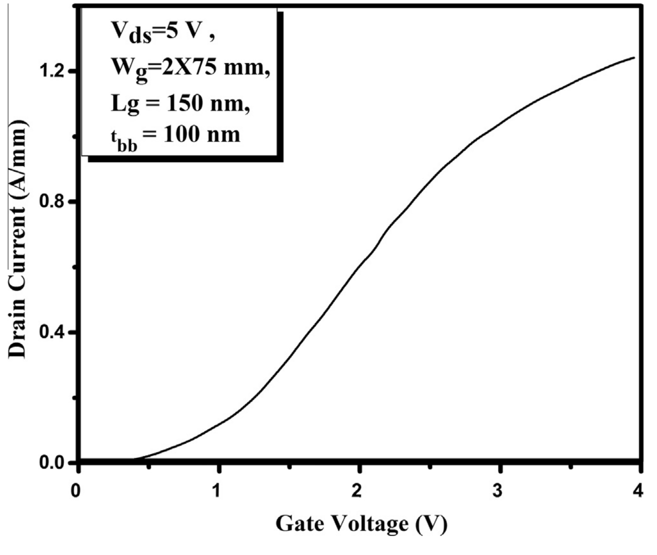

Fig. 4. Simulated transfer characteristics curve of an AlInN/AlN/GaN Gate-Recessed Enhancement Mode HEMT with a p-GaN back barrier layer device. L_g = 150 nm, $W_g = 2 \times 75$ µm, p-GaN back barrier width (t_{bb}) 100 nm and V_{ds} = 5V are kept constant.

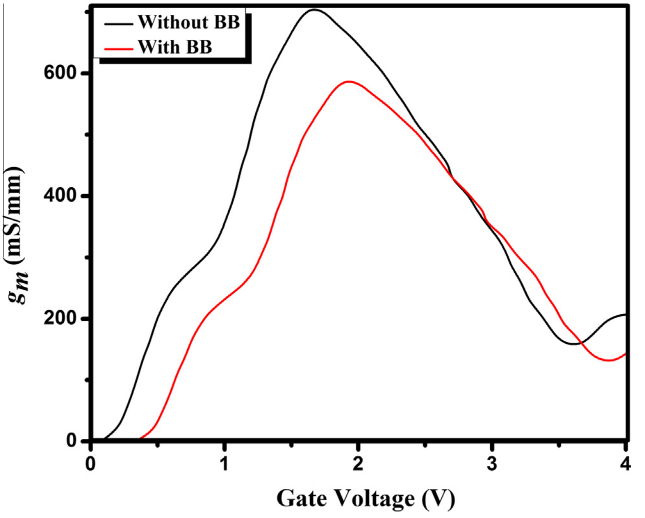

Fig. 5. Simulated (red line) and experimental (black line) curves showing variation in g_m with V_{gs} for an AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT devices with and without p-GaN back barrier layer devices. L_g = 150 nm, $W_g = 2 \times 75$ µm, t_{bb} = 100 nm and V_{ds} = 5V are kept constant. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

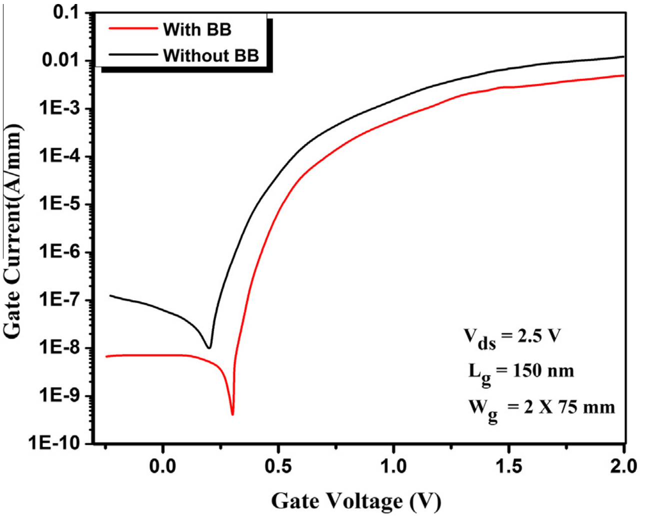

Fig. 6. Simulated (red line) and experimental (black line) curves Gate leakage current of an AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT devices with and without p-GaN back barrier layer devices. L_g = 150 nm, $W_g = 2 \times 75$ µm, t_{bb} = 100 nm and V_{ds} = 2.5 V are kept constant. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

channel layer, owing to the extremely high potential barrier caused by the p-GaN layer. Lower gate leakage is beneficial for switching application, as it will lead to reduced stand-by power dissipation. Lower gate leakage also helps to attains very high I_{on}/I_{off} ratio for the back barrier device.

The Fig. 7 shows the simulated energy band diagrams of AlInN/AlN/GaN heterostructure Gate-Recessed Enhancement-Mode HEMT with and without p-GaN back-barrier, as obtained using a 1D

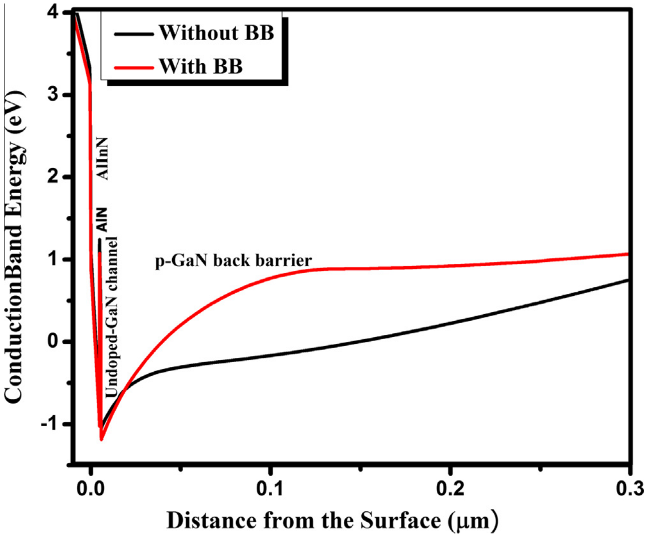

Fig. 7. Simulated curves (both) for conduction band diagram of an AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT devices with and without p-GaN back barrier layer devices. L_g = 150 nm, $W_g = 2 \times 75$ μm, t_{bb} = 100 nm and V_{ds} = 5 V are kept constant.

Poisson solver. The existence of a high-potential p-GaN back-barrier is evident. As seen from the figure the p-GaN back barrier layer has higher conduction band energy, which increase electrostatic barrier leading to deeper quantum well. The deeper quantum well will increase in 2DEG confinement in the channel region. Consequently, spreading of electrons from the channel to the buffer layer will be reduced leading to possible reduction in buffer leakage current, which needs to be investigated further.

Fig. 8 the subthreshold transfer characteristics for device with p-GaN back barrier at V_{ds} = 0.1 and V_{ds} = 2.5 V. The subthreshold slope (SS) that determines rapid switching off capability of a transistor can be defined as the change in gate voltage required to produce one decade change in subthreshold drain current. It is desirable to have a steep subthreshold slope for switching off the transistor rapidly. Subthreshold slope of 78.5 mV/decade was observed for the p-GaN back barrier, which is lower than the 84 mV/decade obtained in the without back barrier device [9]. Important parameter describing electrostatic integrity of HEMTs is DIBL, which can be expressed as the shift of threshold voltage caused by change in the drain voltage. The DIBL of 44 mV/V was observed as against the 100 mV/V reported for the without back barrier device [9]. Lower values of DIBL and SS represent excellent electrostatic gate control and immunity to short channel effects. Additionally, very high I_{on}/I_{off} ratio in the range of 10^7 is obtained due to very low I_{off} current.

Fig. 9 shows the variation in total gate capacitance (C_{gg}) with V_{gs} for the device with and without p-GaN back barrier. At low V_{gs}, C_{gg} is low and is mainly dominated by parasitic capacitance, whereas at higher V_{gs}, it attains high value. The presence of p-GaN back barrier partially depletes 2DEG in the channel, which leads to reduction in total effective gate capacitance as compared to the device without back barrier.

The trend related to the variation in cutoff frequency (f_T) as a function of V_{gs} for device with and without back barrier is shown in Fig. 10. The f_T is the frequency when the current gain is unity and is an important measure for high-speed digital applications (speed and high swing). Maximizing f_T is the primary goals for RF applications. The cutoff frequency can be given as [7]

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1 + 2(C_{gd}/C_{gs})}} \approx \frac{g_m}{2\pi(C_{gd} + C_{gs})} \approx \frac{g_m}{2\pi C_{gg}} \quad (3)$$

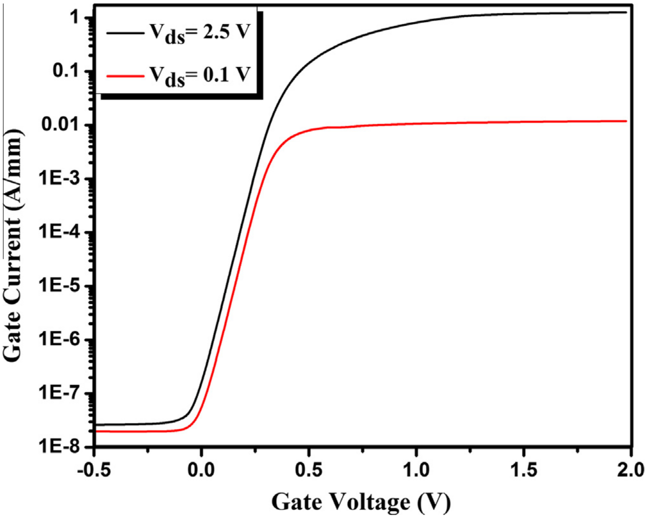

Fig. 8. Simulated curves (both) showing subthreshold characteristics of an AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT with a p-GaN back barrier layer at different V_{ds}. $L_g = 150$ nm, $W_g = 2 \times 75$ µm, $t_{bb} = 100$ nm are kept constant. (DIBL = 44 mV/V, I_{on}/I_{off} ratio >10^7, and $S = 78.5$ mV/dec are observed).

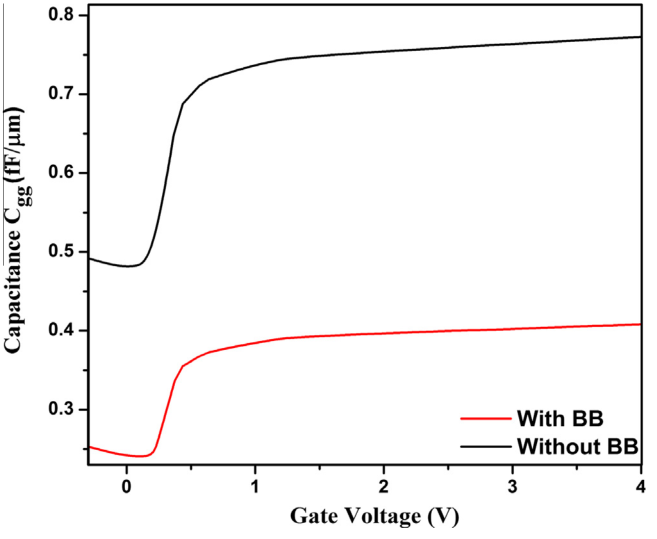

Fig. 9. Simulated curves (both) for C_{gg} versus V_{gs} curve for AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT with and without p-GaN back barrier layer devices. $L_g = 150$ nm, $W_g = 2 \times 75$ µm, $t_{bb} = 100$ nm and $V_{ds} = 0.1$ V are kept constant. Measured at $f = 1$ MHz.

Fig. 10 shows the trend related to the variation of f_T with V_{gs} for devices with and without p-GaN back barrier. The p-GaN back barrier device exhibits very impressive peak f_T of 123 GHz. The f_T starts to increase with gate bias initially and then falls gradually. For lower gate voltage the initial surge in f_T is attributed to increase in g_m and relatively stable C_{gg}. As V_{gs} increases further, f_T drops due to the collective effect of the lower accelerated increase of C_{gg} and the decrease of g_m. Cutoff frequency increases because the rate of decrease of g_m with p-GaN back barrier (Fig. 5) is lower than the rate of decrease of C_{gg} (Fig. 9).

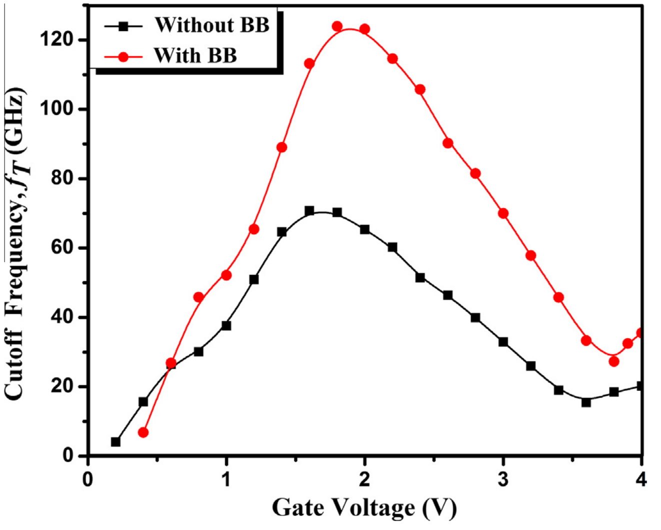

Fig. 10. Simulated curves (both) for f_T variations with V_{gs} for an AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT with and without p-GaN back barrier layer devices. L_g = 150 nm, W_g = 2 × 75 μm, t_{bb} = 100 nm are kept constant.

5. Conclusion

We have studied by simulation, the effect of p-GaN back barrier layer on the device performance of the proposed the p-GaN back barrier AlInN/AlN/GaN Gate-Recessed Enhancement-Mode HEMT. The results obtained from the simulations are compared with the previously reported results by other group for the device without back barrier layer. The device with p-GaN back barrier has shown excellent electrostatic control leading to reduced DIBL, reduced SS and very low gate leakage. The device also exhibits very high I_{on}/I_{off} ratio in the range of 10^7. However, the device showed lower I_d and g_m due to lower sheet charge density and higher access resistance. Additionally, the device offers a very high f_T of 123 GHz. Thus, p-GaN back barrier approach can be effectively deployed to scale the gate length further which would help in attaining high-frequency performance.

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References

[1] J. Kuzmik, IEEE Electron Device Lett. 22 (2001) 510–512.
[2] F. Medjdoub, J.F. Carlin, M. Gonschorek, et al., International Electron Devices Meeting, San Francisco, California, USA, 2006, pp. 11–13.
[3] H.F. Sun, A.R. Alt, H. Benedickter, et al, IEEE Electron Device Lett. 31 (2010) 957–959.
[4] H. Wang, J. Chung, X. Gao, et al, Phys. Status Solidi (C) 7 (2010) 2440–2444.
[5] J. Kuzmik, G. Pozzovivo, C. Ostermaier, et al, J. Appl. Phys. 106 (2009). pp. 124503–124503-7.
[6] D.S. Lee, J.W. Chung, H. Wang, et al, IEEE Electron Device Lett. 32 (2011) 755–757.
[7] H. Pardeshi, G. Raj, S. Pati, et al, Superlattices Microstruct. 60 (2013) 47–59.
[8] C. Ostermaier, G. Pozzovivo, J.F. Carlin, et al, IEEE Electron Device Lett. 30 (10) (2009) 1030–1032.
[9] R. Wang, P. Saunier, C. Lian, et al, IEEE Electron Device Lett. 31 (2010) 1383–1385.
[10] F. Medjdoub, M. Alomari, J.F. Carlin, et al, IEEE Electron Device Lett. 29 (2008) 422–425.
[11] D. Seup Lee, Xiang Gao, Shiping Guo, et al, IEEE Electron Device Lett. 32 (2011) 617–619.
[12] L. Bo, F. Zhihong, D. Shaobo, et al, J. Semiconduct. 34 (2013) 044006.
[13] D.S. Kim, S.N. Kim, K.W. Kim, et al, J. Korean Phys. Soc. 58 (5) (2011) 1500–1504.
[14] M. Gonschorek, J.F. Carlin, E. Feltin, et al, Appl. Phys. Lett. 89 (2006) 062106.

[15] J.Q. Xie, X.F. Ni, M. Wu, et al, Appl. Phys. Lett. 91 (3) (2007) 132116.
[16] Synopsys, TCAD Sentaurus device user's manual VG-2012.06.
[17] M.O. Manasreh, III-Nitride Semiconductors: Electrical, Structural and Defects Properties, Elsevier Science, Amsterdam, Netherlands, 2000.
[18] G. Masetti, M. Severi, S. Solmi, IEEE Trans. Electron Devices 30 (7) (1983) 764–769.
[19] G. Ji, H.G. Liu, Y.B. Su, et al, Chin. Phys. B 21 (2012) 058501.
[20] H. Pardeshi, G. Raj, G. Pati, et al, Superlattices Microstruct. 60 (2013) 10–22.
[21] C. Canali, G. Majni, R. Minder, et al, IEEE Trans. Electron Devices 22 (11) (1975) 1045–1047.
[22] J.D. Albrecht, R.P. Wang, P.P. Ruden, et al, J. Appl. Phys. 83 (1998) 4777.
[23] T. Kachi, in Proceedings of IEEE Compound Semiconductor IC Symposium, San Francisco, CA, USA, October 16–19, 2007, pp. 13.
[24] S. Turuvekere, N. Karumuri, A.A. Rahman, et al, IEEE Trans. Electron Devices 60 (10) (2013) 3157–3164.