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Monolithic wideband linear power amplifier with 45% power bandwidth using pseudomorphic high-electron-mobility transistors for long-term evolution application

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A fully integrated, monolithic, wideband linear power amplifier using pseudomorphic high-electron-mobility transistor (pHEMT) technology has been developed for long-term evolution (LTE) applications. Implemented through the stacked field-effect transistor (stacked-FET) configuration, the amplifier exhibited a small signal gain of 15 dB and an output power of 25 dBm at 1 dB compression (P_{1dB}) with a power-added efficiency (PAE) of 36% from 1.7 to 2.7 GHz yielding 45% power bandwidth. Moreover, when tested under a 10 MHz LTE-modulated signal, the amplifier achieved a 3% error-vector-magnitude (EVM) at 23 dBm output power over the entire power bandwidth. © 2014 The Japan Society of Applied Physics

The growing demands for higher data rate and larger bandwidth have accelerated the development of modern cellular communication systems to satisfy customers' needs. Recently, cellular services based on the so-called fourth-generation (4G) wireless standards, such as long-term evolution (LTE), have been deployed on a large scale. Generally, spectrally efficient modulation schemes such as orthogonal frequency division multiplexing (OFDM) are employed to guarantee high-data-rate transmission. Despite the advantages offered by such advanced systems, the signals with a high peak-to-average power ratio (PAPR) have also made the power amplifier design very challenging. Highly linear power amplifiers with good efficiency over a wide bandwidth are necessary to meet the stringent signal-quality specifications of the system.

Operating the power amplifier (PA) in the large power back-off region is the conventional approach to achieve the desired linearity requirement. However, such an approach inevitably leads to poor efficiency, which is undesirable especially in mobile applications. In the past, research efforts were devoted to achieving both high linearity and efficiency simultaneously using various technologies.[1–17] Among them, the envelope tracking configuration, in which the power supply to the main amplifier is modulated instantaneously in accordance with the power level, has been very popular.[4–6] It allows the main amplifier to operate in the power saturation region, thus boosting the power-added efficiency (PAE) significantly at the linear output level. Recently, a PAE of 25.4% at linear power output has been achieved, enabling a fully integrated CMOS PA to deliver a PAE comparable to those of conventional PAs based on III–V compound semiconductors.[4]

Other than the envelope tracking topology, PAs based on the Doherty configuration have also been good candidates for addressing concerns about achieving high linearity and efficiency simultaneously.[13,14] Bandwidth enhancement using an additional phase compensation network has been successfully applied to solve the bandwidth limitations in conventional Doherty PAs.[13] Despite the effectiveness of both configurations, circuit complexity appears to be the major issue since additional circuit networks other than the core amplifiers must be implemented to guarantee satisfactory performance. In this paper, we present a monolithic integrated linear power amplifier based on the stacked field-effect transistor (stacked-FET) configuration fabricated by the standard pseudomorphic high-electron-mobility (pHEMT) process. The stacked-FET approach has been very effective in delivering high power for broadband operation since the optimum output load impedance can be adjusted through the bias condition.[18–22] With the proper adjustment of the feedback capacitance, we managed to implement a linear PA with a power bandwidth of 45% for LTE applications.

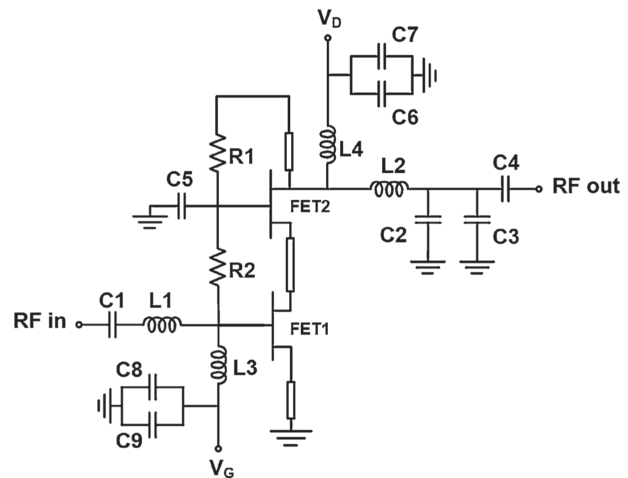

Fig. 1. Circuit schematic of the proposed stacked-FET configuration designed for LTE applications.

Figure 1 shows the schematic of the designed linear PA for LTE applications. It consists of two FETs stacked in series. Each FET has a total gate width of 1.2 mm; thus, the total gate width in the amplifier is 2.4 mm. In the proposed circuit, C1 and C4 are blocking capacitors at the input and output ports, respectively. C6, C7, C8, and C9 are bypass capacitors. L1, L2, C2, and C3 are matching components to provide necessary impedance matching over the desired band of operation. L3 and L4 serve as RF chokes and L4 is implemented using a high-impedance transmission line to reduce the total chip area. Both FETs were biased at class AB with $V_D = 6$ V and $V_G = -1$ V for efficiency consideration, and the biasing network was implemented through the resistive voltage divider network, which also helped to stabilize the circuit. The resistors R1 and R2 were chosen to be 500 and 400 Ω, respectively, yielding a quiescent current of 110 mA in our case.

The capacitor connected to the gate of FET2 (C5) played a critical role in determining the overall performance of the

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Table I. Key parameters of the in-house developed standard pHEMT process.

Parameter	Value
Active device	
Gate length (μm)	0.15
Source-to-drain spacing (μm)	2
Maximum drain current $I_{DS,max}$ (mA/mm)	620
Maximum transconductance g_m (mS/mm)	450
Threshold voltage V_{th} (V)	−1.3
Breakdown voltage V_{bk} (V)	9.3
Current-gain cutoff frequency f_T (GHz)	65 (at $V_{DS} = 3$ V)
Power density at 2 GHz (mW/mm)	426
Passive components	
SiN MIM capacitor (pF/mm^2)	380
NiCr TFR resistor (Ω/square)	55

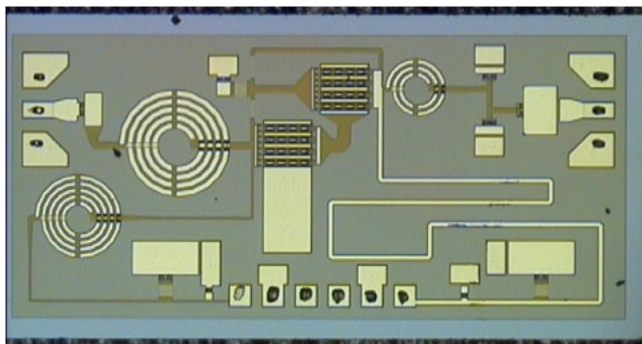
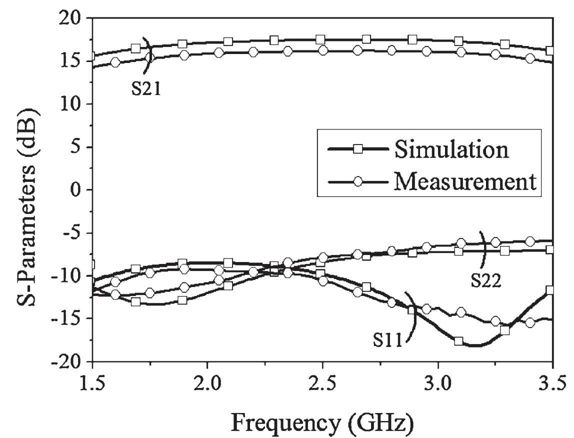


Fig. 2. (Color online) Photograph of the chip fabricated using in-house-developed standard pHEMT process. The overall chip area is 2 mm^2.



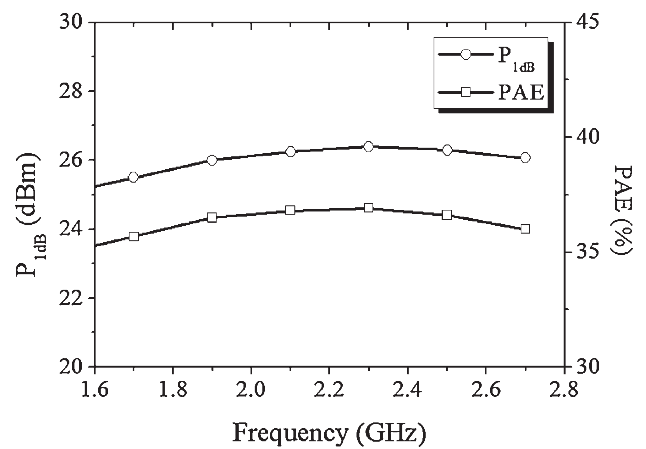


Fig. 3. (a) Measured *S*-parameters of the amplifier using on-wafer probing system with simulation results included. (b) Measured P_{1dB} and PAE as functions of frequency.

circuit. Such capacitance presented a finite impedance at the gate of FET2 to allow an appropriate amount of RF voltage swing at the gates.[22] The amount of capacitance also determines the load impedance presented to FET1 at the bottom, which, in turn, affects the power and linearity performance of the circuit. In our specific design targeted at the upper band for LTE applications, the optimal value of C5 was chosen to be 0.7 pF. The designed circuit was fabricated using an in-house-developed standard pHEMT process, the details of which were included in our previous publications.[23,24] Table I lists the key process parameters for the device and passive components. Note that the parameters for the device were extracted from the measurement results of a 2 × 50 μm test device with the same gate width. The photograph of the fabricated chip is shown in Fig. 2. Its total area was 2 mm^2 including the ground–signal–ground (GSG) probing pads at the input and output.

Figure 3(a) shows the measured scattering parameters (*S*-parameters) of the amplifier with an on-wafer probing system. The simulation results are also included for comparison. As is observed, the amplifier exhibited a relatively broadband gain performance of 15 dB from 1.7 to 2.7 GHz. Overall, the simulation and measurement results showed good agreement over the band of interest. Figure 3(b) shows the results of the on-wafer power measurement. With a continuous-wave (CW) signal as the input, the amplifier delivered an output power exceeding 25 dBm at 1 dB compression (P_{1dB}) from 1.7 to 2.7 GHz. P_{1dB} remained almost constant across the band with a corresponding power bandwidth of 45% centered at 2.2 GHz. To the best of our knowledge, this is the highest power bandwidth ever reported among linear PAs for LTE applications. The measured PAE as a function of frequency is also included in Fig. 3(b). We observed a similar trend in frequency as P_{1dB} with a peak PAE of 37.2% at around 2.1 GHz.

With the performance verified, the chip was then packaged by flip-chip technology[25,26] for linearity measurement. Figure 4 shows the complete PA module after packaging. Figure 5 shows the measured small-signal performance before and after packaging. Only a very minor gain degradation due to flip-chip packaging is observed. The RSMBV100A vector signal generator and RFSV7 signal analyzer from Rhode and Schwartz were adopted as the main test equipment to characterize the linearity performance of the packaged amplifier. Figure 6(a) shows the measured error-vector-magnitude (EVM) as a function of output power at 2.2 GHz for a 10 MHz 16QAM LTE signal with a PAPR of 6.7 dB. It is observed that the packaged amplifier demonstrated an EVM of less than 3% up to 23 dBm output power. The corresponding screen capture of the measured constellation at the same power level is shown in Fig. 6(b). Finally, Table II summarizes the performance characteristics of our PA and state-of-the-art PAs with different technologies.

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Table II. Performance characteristics of state-of-the-art LTE PAs.

	This work	Ref. 4	Ref. 6	Ref. 10
Modulation	LTE 16QAM	LTE	LTE 16QAM	LTE 16QAM
Bandwidth (MHz)	10	10	10	5
Frequency (GHz)	2.2	1.95	0.93	2.4
Gain (dB)	15	24	28	16.3
Linear P_{out} (dBm)	23 (EVM < 3%)	25.6 (ACLR < −32 dBC)	26 (EVM < −22 dB)	24.3 (EVM < 5%)
PAE (%)	35	25.4	17	42%
Technology	0.15 µm pHEMT stacked-FET	90 nm CMOS envelope tracking	90 nm CMOS	0.35 µm SiGe BiCMOS envelope tracking

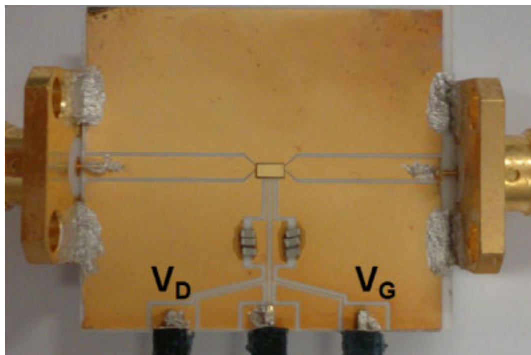


Fig. 4. (Color online) Photograph of the complete PA module packaged by flip-chip technology.

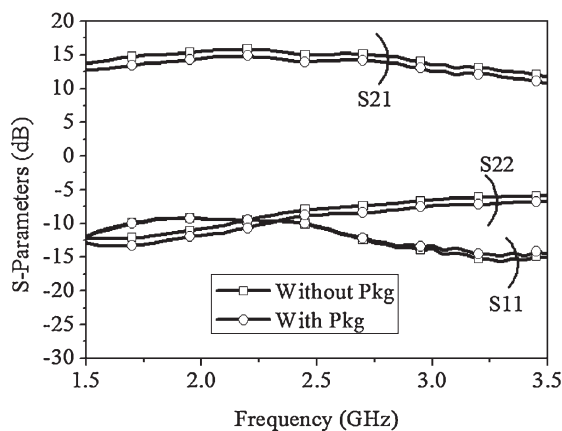
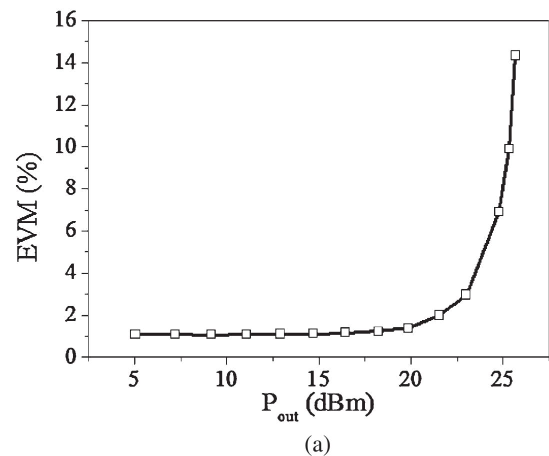
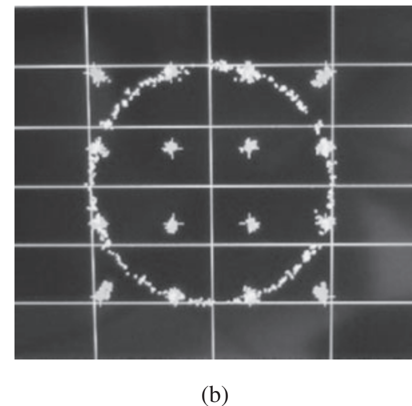


Fig. 5. Measured small-signal performance of the amplifier with and without flip-chip packaging.



(a)



(b)

Fig. 6. (a) Measured EVM as a function of output power at 2.2 GHz. (b) Screen capture of the measured constellation at 23 dBm output power at 2.2 GHz.

In this work, we successfully demonstrated the feasibility of realizing a linear power amplifier for LTE applications by adopting the stacked-FET configuration. The design was implemented by standard pHEMT process technology and flip-chip packaging to form a complete module. Experimental results verified that the proposed simple configuration exhibited a linearity performance with the best power bandwidth comparable to those of other state-of-the-art PAs for LTE applications.

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