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A compact 12-bit DAC with novel bias scheme

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Abstract: A compact and low-power design of a 12-bit binary-weighted current-steering DAC is presented. Instead of 4096 unit current cells, the proposed design uses 192 unit current sources with two reference currents. The silicon area of the generation circuit of two reference currents is very compact as well. The area of the total current source arrays is smaller than four times the area of 6-bit current source arrays, which has significantly reduced the dimension of the analog part of a conventional 12-bit DAC. The proposed DAC achieves 400 MS/s update rate and consumes 38.7 mW from single 1.8 V supply.

Keywords: digital-to-analog converter, DAC, compact area

Classification: Integrated circuits

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1 Introduction

The current-steering digital-to-analogue converter (DAC) is a good candidate for high-speed DAC applications because of the good linearity and power efficiency. Current-steering DACs are based on an array of current sources that are switched to

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the output. The three different architectures used to implement the switched current source array are binary, unary, and segmented [1, 2]. Without a large number of transistors for thermometer decoder, the binary-weighted architecture is capable for high-speed, low-power and small-area DAC applications [3]. Since the static performance of a DAC mainly depends on the matching of current source arrays (CSA), some circuit techniques were used to suppress the gradient errors due to process variations [4, 5]. However, reducing random mismatch among the current source transistors only depends on increasing area. To minimize the chip size of the 12-bit DAC, this paper proposes a new architecture of 12-bit binary-weighted current-steering DAC with two reference currents. This technique is effective for both unary and segmented architectures as this technique is aimed for the area reduction of current source arrays, independent of either binary-weighted or unary structure. The number of unit current sources is reduced from 4096 to 192, and the total area is compact even though the generator of two reference currents is included.

2 Proposed 12-bit DAC architecture

Fig. 1 shows the architecture of the proposed 12-bit binary-weighted DAC. B0-B11 are digital inputs, which are synchronized by re-timing latches. The current switches are binary-weighted, and the binary current sources are implemented as a combination of unit current sources. The current source arrays are divided into 2 groups, while A1 maps to bit 0 ~ bit 5 and A2 maps to bit 6 ~ bit 11. The reference current of A1 is CS1 and the reference current of A2 is CS2, where the CS2 is generated by A11 and CM12. The A11 is a replica of A1 and CM12 is a current mirror of total current of A11, as shown in Fig. 2. In the layout, A1 and A11 are placed next to each other, so the matching between A11 and A1 will be good. The difference between A1 and A11 is that A1 is controlled by current switches, but that A11 is always turned on to produce reference current, as shown in Fig. 3. The total current of A11 is used to generate the reference current CS2 by using current mirror CM12. Furthermore, gradient-induced mismatch among current sources could be compensated by using a common-centroid scheme, as shown in Fig. 4. Because the drain current of M1 in Fig. 2 is the sum of 64 unit current sources with symmetry

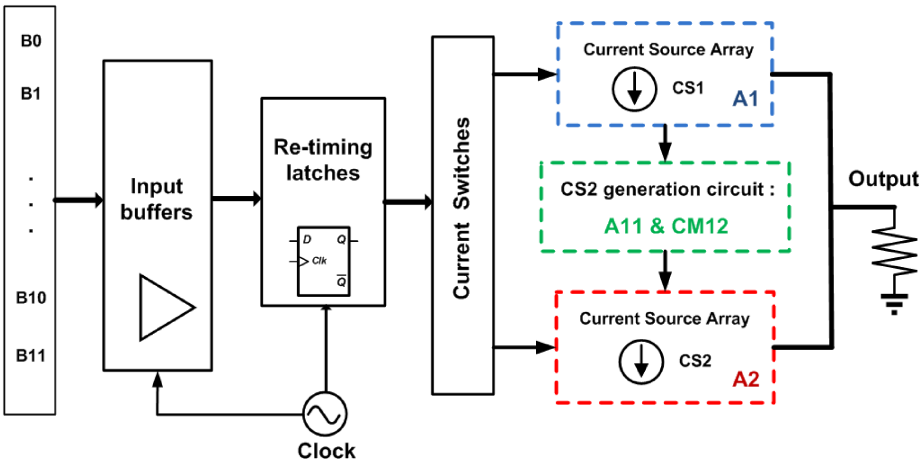

Fig. 1. Circuit architecture of the proposed 12-bit DAC

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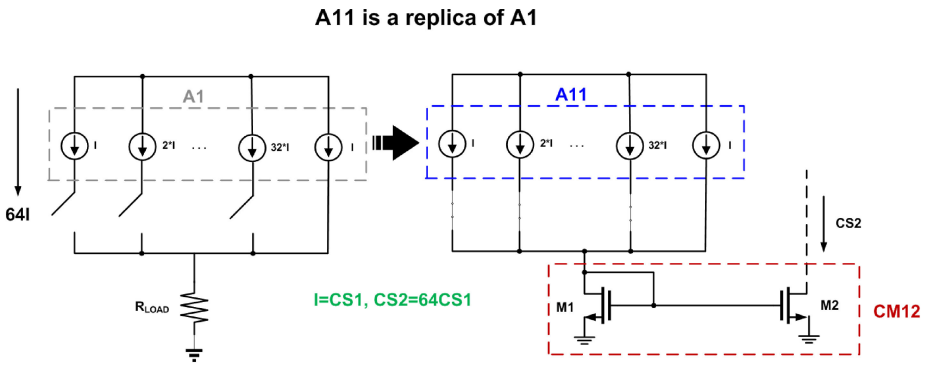

Fig. 2. CS2 generation circuit

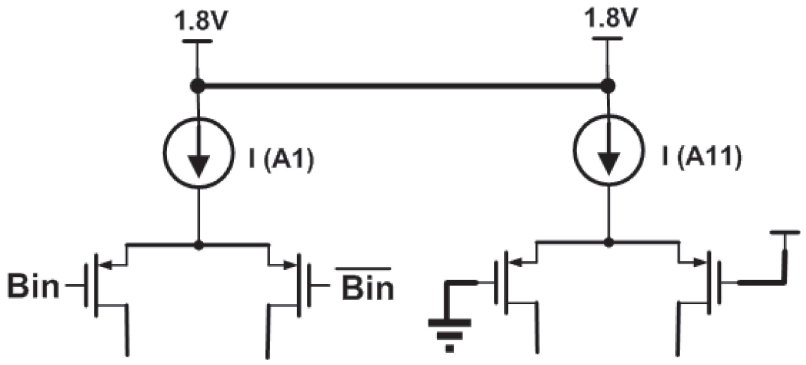

Fig. 3. Difference between A1 and A11 for 1-bit explanation

D	D	D	D	D	D	D	D	D	D
D	B2	B5	B5	B5	B5	B5	B5	B2	D
D	B5	B5	B4	B4	B5	B4	B5	B5	D
D	B5	B4	B4	B3	B3	B4	B4	B5	D
D	B5	B4	B3	B1		B3	B5	B5	D
D	B5	B5	B3	B0	B1	B3	B4	B5	D
D	B5	B4	B4	B3	B3	B4	B4	B5	D
D	B5	B5	B4	B5	B4	B4	B5	B5	D
D	B2	B5	B5	B5	B5	B5	B5	B2	D
D	D	D	D	D	D	D	D	D	D

D: Dummy devices

Fig. 4. Layout scheme for 6-bit current source arrays

layout, the gradient errors of A11 will be averaged and CS2 is very close to the drain current of M1.

2.1 Current-source transistor design

To achieve a 99.7% INL yield specification for a 12-bit DAC, the specification for the unity current-source matching is 0.25%, and the closed-forms of analytical expressions have been derived in [6]. The process mismatch of MOS transistors in the CSA is characterized by A_{VT} and A_{β} parameters provided by foundry, and the random mismatch can be reduced by increasing the size of transistors [7, 8]. The size versus current-source transistor relation is given in Eqs. (1) and (2).

$$\frac{W}{L} = \frac{2I}{\mu C_{ox}(V_{gs} - V_t)^2} \tag{1}$$

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$$WL = \left(A_\beta{}^2 + \frac{4A_{VT}{}^2}{(V_{gs} - V_t)^2} \right) \Big/ \frac{\Delta I^2}{I^2} \tag{2}$$

The current-source transistor of a 6-bit LSB is designed with the unit current of 5 uA, where the transistor size is W1 = 8.6 um, L1 = 13 um. The current-source transistor of 6-bit MSB is designed with the unit current of 320 uA, where the transistor size is W2 = 69 um, L2 = 1.6 um. The product of W1*L1 is equal to the product of W2*L2 due to the same resolution and over-drive voltage, so the area of 6-bit LSB CSA is the same as 6-bit MSB CSA approximately.

2.2 Current-mirror transistor design

It is clear that the critical portion of the proposed idea is the matching between CS2 and 64CS1, that is, the accuracy of the generation circuit of CS2. Thus, we design the current-mirror transistors of the CS2 generation circuit with 12-bit accuracy using Eqs. (1) and (2). The size of M1/M2 in Fig. 2 is designed as W = 16 um and L = 3 um. To ensure the random mismatch of the current mirror is less than 1 LSB, the Monte Carlo simulation was performed with 5000 runs, and the simulation result is depicted in Fig. 5. The mean value of the drain current of M2 in Fig. 2 is 319.8 uA, and 1 sigma value is 0.77 uA. Thus the 3 sigma value of the drain current of M2 is smaller than 0.5 LSB, where 1 LSB is 5 uA. This result guarantees the generation circuit of CS2 is working with 99.7% yield.

If the area of the 6-bit LSB CSA is A, then the area of the 6-bit MSB CSA is A, and the area of A11 is A as well. Thus, the area of the total CSA is smaller than 4A as the total area of the entire CS2 generation circuit is smaller than 2A. For a conventional 12-bit DAC, the area of CSA is 64A. Therefore, the area of the proposed DAC is about 1/16 of the conventional 12-bit current-steering DAC. Shrinking the size of the CSA also reduces the number of required driving buffers or driving strength. In practice, the dimension of the current mirror in Fig. 2 can be over-designed to 14-bit accuracy to further reduce the mismatch between M1 and M2. The penalty of increasing area is small and the design will become more robust for mass production.

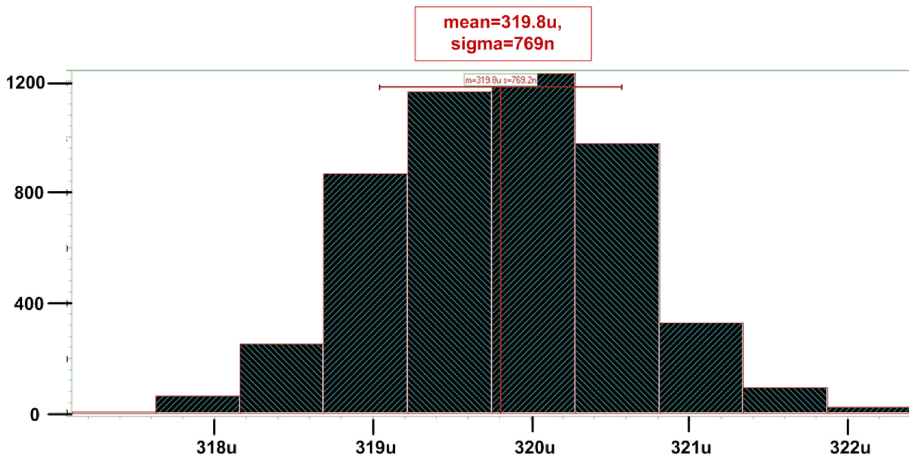

Fig. 5. Histogram of Monte Carlo simulation of I(M2) in Fig. 2.

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3 Simulation results

A 12-bit 400 MS/s current-steering DAC was designed based on the TSMC 0.18 µm CMOS process. All simulations have been performed on differential outputs with 25 ohm loading, respectively. For static performance, the simulated INL is within 0.2 LSB and DNL is within 0.1 LSB, as shown in Fig. 6. Because the maximum of DNL often occurs during the major code transition (011…1 to 100…0) for binary-weighted DAC, the Monte Carlo simulations for DNL were performed for major code transition with 1000 runs. The result indicates the DNLs are within 0.15 LSB, as shown in Fig. 7. The converter is monotonic as DNL is smaller than 1 LSB.

For dynamic performance, at 400 MHz clock frequency, the SFDR was 77 dB with 100 MHz output frequency. The time-domain output waveform is depicted in Fig. 8, and the output spectrum is depicted in Fig. 9. Furthermore, the DAC consumes 38.7 mW from a single supply of 1.8 V. Table I summarizes the performance. The FoM used in [7] is applied here, as shown in Equation (3).

$$FoM = \frac{POWER}{2^N \times Sample\ Rate} \tag{3}$$

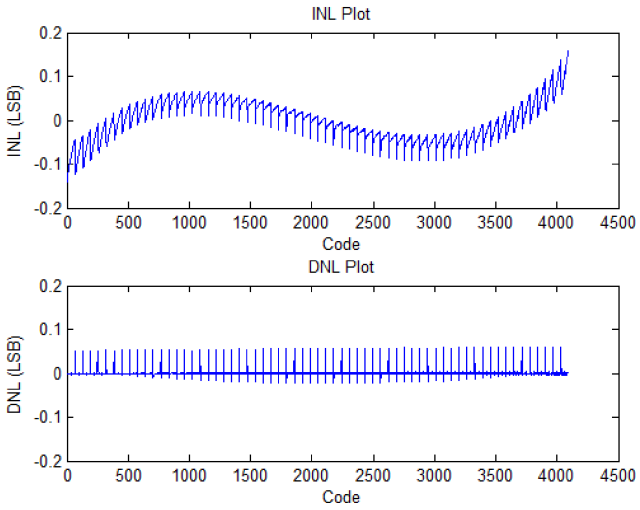

Fig. 6. INL and DNL

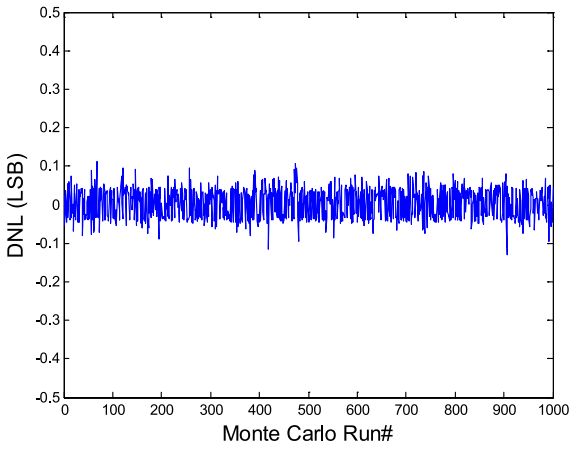

Fig. 7. Monte Carlo simulations for DNL during major code transitions

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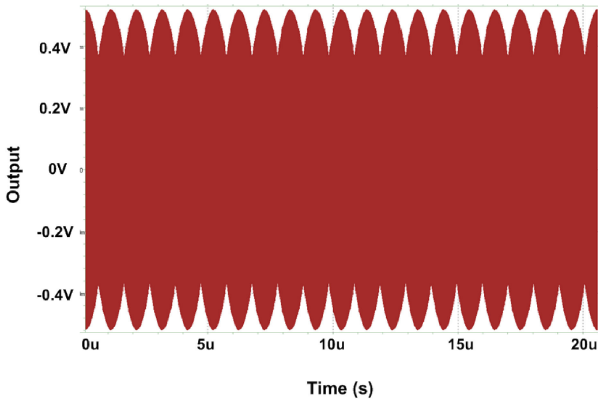

Fig. 8. Time-domain waveform for a 100-MHz output signal

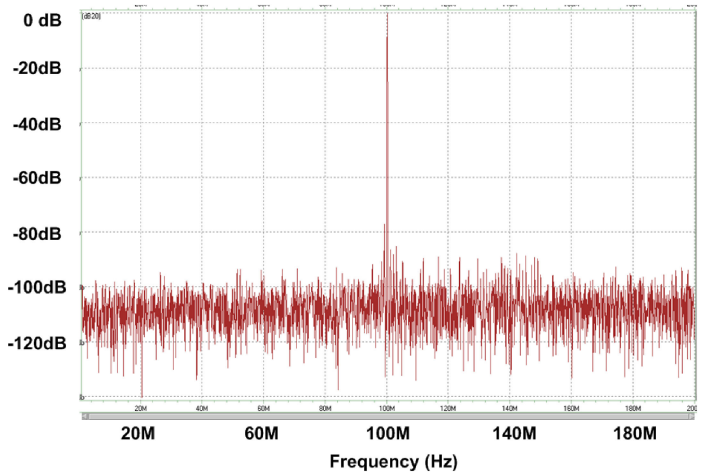

Fig. 9. Output spectrum for a 100-MHz signal at 400 MS/s clock

Table I. Performance summary

Technology	CMOS 0.18 um
Resolution	12 bits
Clock rate	400 MS/s
SFDR	77 dB
DNL	< 0.1 LSB
INL	< 0.2 LSB
Supply Voltage	1.8 V
Area	~ 1/16 of conventional 12-bit DAC
Power Consumption	38.7 mW
FoM	0.02 pJ

4 Conclusion

A novel bias method with low power and compact area for a 12-bit binary-weighted DAC is proposed. Simulation results validate the technique of the two reference currents. The area of the proposed DAC is about 1/16 of a conventional 12-bit

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current-steering DAC. The proposed DAC implemented by the standard CMOS 0.18 um process achieves 400 MS/s clock rate and consumes 38.7 mW from single 1.8 V supply.

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