Improved Reliability of HfO_2/SiON Gate Stack by Fluorine Incorporation

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***Abstract*—Effects of fluorine (F) incorporation on the reliabilities of pMOSFETs with HfO_2/SiON gate stacks have been studied. In this letter, fluorine was incorporated during the source/drain implant step and was diffused into the gate stacks during subsequent dopant activation. The authors found that F introduction only negligibly affects the fundamental electrical properties of the transistors, such as threshold voltage $V_{\rm th}$, subthreshold swing, gate leakage current, and equivalent oxide thickness. In contrast, reduced generation rates in interface states and charge trapping under constant voltage stress and bias temperature stress were observed for the fluorine-incorporated split. Moreover, the authors demonstrated for the first time that F incorporation could strengthen the immunity against plasma charging damage.**

***Index Terms*—Bias temperature instability (BTI), fluorine (F), hafnium oxide, plasma charging damage.**

I. Introduction

RECENTLY, HfO_2 has emerged as the leading high-k dielectric to replace the conventional SiO_2. However, a number of pending issues need to be resolved before HfO_2 can be inducted into the mainstream ultra-large-scale integration (ULSI) technology. These issues include solving mobility degradation and threshold voltage instability, as well as reducing the number of fixed charges and charge traps [1]–[4]. Although there exist numerous literature reports regarding methods to incorporate nitrogen [5], [6] or Si [7], [8] into Hf-based films or stacks so as to improve the film's quality, however, to the best of our knowledge, the effect of F incorporation on HfO_2 gate dielectric was seldom addressed [9], [10]. In this letter, fluorine incorporation through fluorine implantation into the source/drain regions was used to evaluate its impact on the constant voltage stress (CVS) instability and negative bias temperature instability (NBTI) of pMOSFETs with HfO_2 gate stacks. Our results clearly show that these degradations are improved in the F-incorporated samples. Moreover, because few studies [9] have been performed regarding plasma charging effects of HfO_2 gate stacks, we have therefore carried out a systematic study in this regard and found that larger antenna ratio will result in much severe degradation. More importantly, our data also show that the plasma charging damage can be significantly improved by the F incorporation into the HfO_2 gate stacks.

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II. Experiment

pMOSFETs with HfO_2/SiON gate stacks were fabricated in this letter. The thin (0.6 nm) interfacial oxynitride layer (SiON) was first grown by rapid thermal processing (RTP) in an N_2O ambient at 700 °C. Subsequently, a 3-nm HfO_2 layer was deposited by atomic vapor deposition (AVD) using an AIXTRON Tricent system at a substrate temperature of 500 °C. Wafers were then annealed in an N_2 ambient at 700 °C for 20 s to improve the HfO_2 film quality. Next, a 200-nm polycrystalline silicon (poly-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD). Then, the gate electrode was patterned through lithographic and etching processes. Some wafers then received a fluorine (F, 2×10^{15} cm^{-2}) ion implantation into the source/drain region without removing the photoresist on the gate electrode. This was deliberately performed to avoid the potential complication caused by fluorine-enhanced boron penetration. After photoresist removal, source/drain regions were formed by regular boron implantation, with the dopants activated at 950 °C by rapid thermal annealing for 20 s in an N_2 atmosphere. It should be noted that the thermal budget of dopant activation also served to diffuse the F species into the HfO_2 gate stacks. After passivation layer deposition, contact holes and aluminum metalization were formed. Finally, a forming gas annealing at 400 °C was performed for 30 min to complete the device fabrication.

The equivalent oxide thickness (EOT) of the gate dielectric was extracted from high-frequency (100 kHz) capacitance–voltage (C–V) curves at strong inversion (EOT $= \varepsilon_{\rm SiO_2}/C_{\rm inv}$) without considering the quantum effect. Charge pumping current was measured with fixed amplitude method at a frequency of 1 MHz [11].

III. Results and Discussion

Fig. 1 depicts the typical I_d–V_g curves of pMOSFETs with HfO_2/SiON gate stacks, both with and without F incorporation. The inset table shows the corresponding transistor parameters. It can be seen that all key device parameters, including the interface state density $N_{\rm it}$, EOT, $V_{\rm th}$, and gate leakage current,

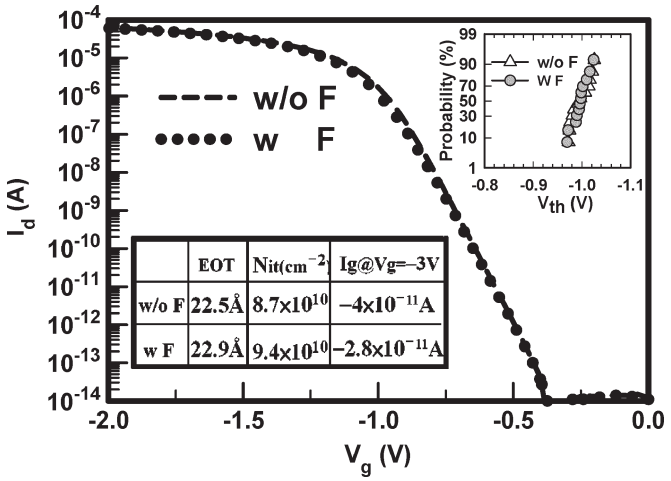

Fig. 1. Typical transfer characteristics of pMOSFETs with HfO_2 gate stack, both with and without fluorine incorporation.

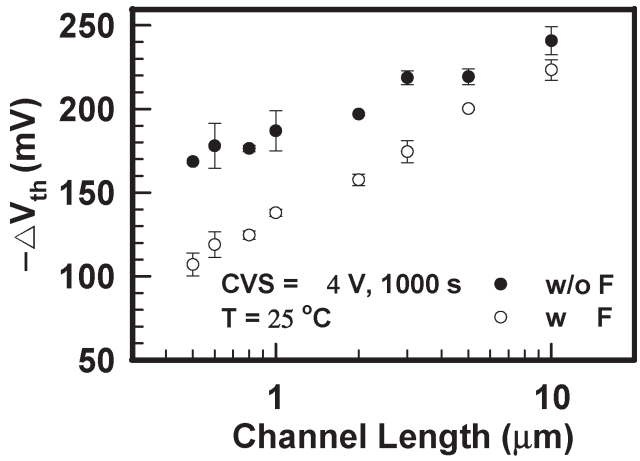

Fig. 3. Threshold voltage shift ($\Delta V_{\rm th}$) as a function of channel length. Devices were stressed at 25 °C and $V_g = -4$ V.

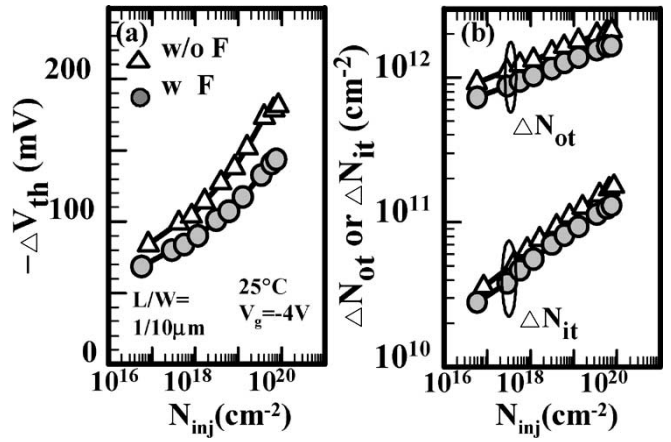

Fig. 2. (a) Threshold voltage shift ($\Delta V_{\rm th}$) and (b) generation of interface states ($\Delta N_{\rm it}$) and trapping charge ($\Delta N_{\rm ot}$), both plotted in log scale, as a function of injection charge density ($V_g = -4$ V). The degradation was dominated by $\Delta N_{\rm ot}$, rather than $\Delta N_{\rm it}$.

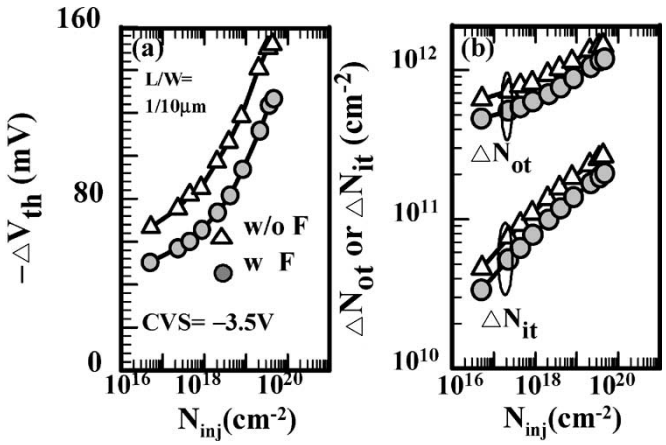

Fig. 4. (a) $\Delta V_{\rm th}$ and (b) $\Delta N_{\rm it}$ and $\Delta N_{\rm ot}$, for splits with and without F incorporation, as a function of injection charge density at $T = 125$ °C under stress voltage of -3.5 V.

are essentially indistinguishable between the samples with and without F incorporation. The inset at the upper right corner shows that the distribution of $V_{\rm th}$ is not affected by the addition of F. All these data suggest that little or no adverse impact on the fundamental electrical properties is achieved with F introduction.

For the reliability evaluation, negative CVS test was performed at 25 °C, with the transfer curves measured for monitoring $\Delta V_{\rm th}$ at various stressing times. The results are shown in Fig. 2(a). To reduce the unstable fast charge detrapping effects [1]–[4], a small positive voltage (0.5 V) with a duration of several seconds was applied to detrap these charges before $I_d - V_g$ and charge pumping measurements without inducing extra damage to the gate stacks. This step thus allows much accurate estimation of the slow trap density without the complication due to the interval variation between voltage stressing and parameter measurement. In other words, the precaution allows us to focus on the slow traps in the gate stacks in this letter. It is clear that the F-incorporated sample always shows smaller $\Delta V_{\rm th}$ than the control counterpart. To further gain insights into the degradation mechanism during voltage stressing, the interface state generation $\Delta N_{\rm it}$ and the increase of effective bulk trap density $\Delta N_{\rm ot}$ are plotted as a function of the injection charge density in Fig. 2(b). It should be noted that $\Delta N_{\rm ot}$ was calculated from $\Delta V_{\rm th}$ by assuming that the charge was trapped at the interface between the dielectric and the substrate. Apparently, $\Delta N_{\rm ot}$ was significantly larger than $\Delta N_{\rm it}$, suggesting that the degradation under CVS was dominated by the charge trapping in the bulk of HfO_2 films, rather than the generation of interface states, whether fluorine was incorporated or not. Moreover, F incorporation was found being able to suppress the charge trapping in the bulk of HfO_2 films. Although reduced charge injection during stressing was a plausible cause for the observed improvement in the F-incorporated split, it contradicted with the observation that the improvement became more visible with decreasing channel length, as show n in Fig. 3. If the improvement seen in F-incorporated split was indeed due to reduced injection charges, no dependence of the improvement on the channel length should be expected. Therefore, we concluded that the improvement was indeed the result of the F incorporation.

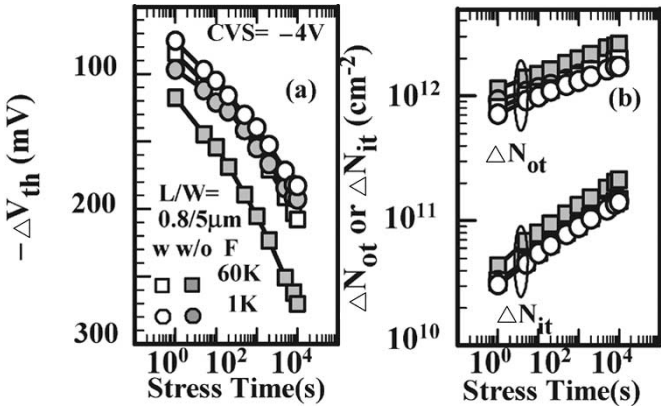

Fig. 5. Time dependence of (a) $\Delta V_{\rm th}$ and (b) $\Delta N_{\rm it}$ under CVS for pMOSFETs with different AARs, both with and without F incorporation. Higher AAR results in much severe degradation, whereas the F-incorporated split exhibits lower $\Delta V_{\rm th}$ and $\Delta N_{\rm it}$.

Fig. 4(a) and (b) compares the dependence of threshold voltage shift and the interface generation, respectively, on injection charge density for splits with and without F incorporation. The BT stress condition was $V_g = -3.5$ V under 125 °C. It can be seen that F-incorporated films exhibit NBTI improvement similar to fluorine-induced NBTI improvement in SiOF case [12], [13]. The major degradation of NBTI is caused by the positive charge trapping in the films rather than the interface generation, suggesting that the positive charge trapping is not entirely caused by the H^+ capturing. Therefore, in addition to positive charge caused by H species, a significant amount of extra trapping centers must be present in the $HfO_2/SiON$ gate stack. Fluorine atoms seem to effectively decorate these trapping centers, leading to reduced degradation.

In our process, the photoresist layer that remained after metal patterning was stripped with O_2 plasma in a downstream plasma asher, whose configuration and plasma potential distribution could be found in [14]. Using CHARM-2 wafer sensor, it has been previously shown [14] that the potential distribution was highly negative and positive at the wafer center and edge, respectively. Fig. 5 shows the time evolution of the threshold voltage shift and interface state generation for the devices with area antenna ratios (AARs) of either 1×10^3 or 6×10^4, both with and without F incorporation. All measurements were performed on devices located at the same die location (i.e., wafer center). Fig. 4 shows that the hole trapping in the bulk, rather than the interface generation, is the preponderant mechanism responsible for the degradation. From the Weibull plot of $V_{\rm th}$ for the fresh devices located at the wafer center, it is found that the control devices with AAR of 6×10^4 depict larger $|V_{\rm th}|$ values than their counterparts with F incorporation (data not shown). This is consistent with previous results in CVS and NBTI. Moreover, all these results are in-line with the hypothesis that plasma antenna charging effect creates more hole traps in the $HfO_2/SiON$ gate stacks and that F-incorporated devices are more robust to plasma charging effect.

IV. Conclusion

In this letter, we found that the reliabilities of pMOSFETs with $HfO_2/SiON$ gate stacks under both CVS and NBTI stresses are significantly improved by the F incorporation. In addition, we demonstrated for the first time that plasma charging effect induces hole trapping in the $HfO_2/SiON$ gate stacks. Finally, we found that the plasma charging effect can be effectively suppressed with F incorporation.

References

[1] S. Zafar, A. Callegari, E. Gusev, and M. Fischetti, "Charge trapping related threshold voltage instabilities in high permittivity gate dielectric stacks," *J. Appl. Phys.*, vol. 93, no. 11, pp. 9298–9303, Jun. 2003.

[2] J. Zhu, T. P. Ma, S. Zafar, and T. Tamagawa, "Charge trapping in ultrathin hafnium oxide," *IEEE Electron Device Lett.*, vol. 23, no. 10, pp. 597–599, Oct. 2002.

[3] E. P. Gusev and C. P. D'Emic, "Charge detrapping in HfO_2 high-k gate stacks," *Appl. Phys. Lett.*, vol. 83, no. 25, pp. 5223–5225, Dec. 2003.

[4] A. Kerber, E. Carter, L. Pantisano, M. Rosmeulen, R. Degraeve, T. Kauerauf, G. Groeseneken, H. E. Maes, and U. Schwalke, "Characterization of V_T instability in SiO_2/HfO_2 gate dielectrics," in *Proc. 41st Int. Reliab. Phys. Symp.*, Dallas, TX, 2003, p. 41.

[5] C. S. Kang, H. Cho, R. Choi, Y. Kim, C. Y. Kang, S. J. Rhee, C. Choi, M. S. Akbar, and J. C. Lee, "The electrical and material characterization of hafnium oxynitride gate dielectrics with TaN-gate electrode," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 220–227, Feb. 2004.

[6] C. S. Kang, H. Cho, K. Onishi, R. Choi, Y. H. Kim, R. Nieh, J. Han, S. Krishnan, A. Shahriar, and J. C. Lee, "Nitrogen concentration effects and performance improvement of MOSFETs using thermally stable HfO_xN_y gate dielectrics," in *IEDM Tech. Dig.*, 2002, pp. 865–868.

[7] T. Iwamoto, T. Ogura, M. Terai, H. Watanabe, N. Ikarashi, M. Miyamura, T. Tatsumi, M. Saitoh, A. Morioka, K. Watanabe, Y. Saito, Y. Yabe, T. Ikarashi, K. Masuzaki, Y. Mochizuki, and T. Mogami, "A highly manufacturable low power and high speed HfSiO CMOS FET with dual poly-Si gate electrodes," in *IEDM Tech. Dig.*, 2003, pp. 639–642.

[8] Y. Kim, H. J. Lim, H. Jung, J. Lee, J. Park, S. K. Han, J. H. Lee, S. Doh, J. P. Kim, N. I. Lee, Y. Chung, H. Y. Kim, N. K. Lee, S. Ramanathan, T. Seidel, M. Boleslawski, G. Irvine, B. Kim, H. Lee, and H. Kang, "Characteristics of ALD $HfSiO_x$ using new Si precursors for gate dielectric applications," in *IEDM Tech. Dig.*, 2004, pp. 511–514.

[9] H.-H. Tseng, M. E. Ramon, L. Hebert, P. J. Tobin, D. Triyoso, S. Kalpat, J. M. Grant, Z. X. Jiang, D. C. Gilmer, D. Menke, W. J. Taylor, O. Adetutu, and B. E. White, "Threshold voltage instability and plasma induced damage of poly-Si/HfO_2 devices -positive impact of deuterium incorporation," in *Proc. ICICDT*, 2004, pp. 255–259.

[10] A. Mineji, Y. Tamura, T. Watanable, H. Ozaki, F. Ootsuka, T. Aoyama, K. Shibata, K. Tsujita, N. Ohashi, M. Yasuhira, and T. Arikado, "Integration of manufacturable 65 nm-node HfSiON transistors optimized with low-thermal-budget CMOS process," in *IEDM Tech. Dig.*, 2004, pp. 927-930.

[11] A. Kerber, E. Carter, L. Pantisano, M. Rosmeulen, R. Degraeve, G. Groeseneken, H. E. Maes, and U. Schwalke, "Charge trapping in SiO_2/HfO_2 gate dielectrics: Comparison between charge pumping and pulsed I_D-V_G," *Microelectron. Eng.*, vol. 72, no. 1–4, pp. 267–272, Apr. 2004.

[12] C. H. Liu, M. T. Lee, C. Lin, J. Chen, K. Schruefer, J. Brighten, N. Rovedo, T. B. Hook, M. V. Khare, S. Huang, C. Wann, T. Chen, and T. H. Ning, "Mechanism and process dependence of negative bias temperature instability (NBTI) for pMOSFETs with ultrathin gate dielectrics," in *IEDM Tech. Dig.*, 2001, pp. 861–864.

[13] Y. Mitani, M. Nagamine, H. Satake, and A. Toriumi, "NBTI mechanism in ultra-thin gate dielectric-nitrogen-originated mechanism in SiON," in *IEDM Tech. Dig.*, 2002, pp. 509–512.

[14] C. C. Chen, H. C. Lin, C. Y. Chang, M. S. Liang, C. H. Chien, S. K. Hsien, and T. Y. Huang, "Improved immunity to plasma damage in ultra thin nitrided oxides," *IEEE Electron Device Lett.*, vol. 21, no. 1, pp. 15-17, Jan. 2000.