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Characterizing the electrical properties of raised S/D junctionless thin-film transistors with a dual-gate structure

Ya-Chi Cheng[1], Hung-Bin Chen[1,2], Jun-Ji Su[1], Chi-Shen Shao[2], Cheng-Ping Wang[1], Chun-Yen Chang[2] and Yung-Chun Wu[1*]

Abstract

This letter demonstrates a p-type raised source-and-drain (raised S/D) junctionless thin-film transistors (JL-TFTs) with a dual-gate structure. The raised S/D structure provides a high saturation current (>1 µA/µm). The subthreshold swing (SS) is 100 mV/decade and the drain-induced barrier lowering (DIBL) is 0.8 mV/V, and the I_{on}/I_{off} current ratio is over 10^8 A/A for $L_g = 1$ µm. Using a thin channel structure obtains excellent performance in the raised S/D structure. Besides the basic electrical characteristics, the dual-gate structure can also be used to adjust V_{th} in multi-V_{th} circuit designs. This study examines the feasibility of using JL-TFTs in future three-dimensional (3D) layer-to-layer stacked high-density device applications.

Keywords: Junctionless (JL); Thin-film transistor (TFT); Raised source-and-drain (raised S/D); Dual-gate; Reliability

Background

Recently, the concept of the junctionless (JL) field-effect transistor (FET), which contains a heavily, uniformly, and homogeneously doping species in the channel and source/drain (S/D), has been intensively studied [1-4]. The JL device is intrinsically a gated resistor, i.e., a resistor with a gate for controlling the carrier density and the current flow. The advantages of JL devices include (1) avoidance of the use of an ultra-shallow source/drain junction, which greatly simplifies the process flow, (2) low thermal budgets owing to implant activation annealing after the gate stack formation is eliminated, and (3) the current transport is in the bulk of the semiconductor, which reduces the impact of imperfect semiconductor/insulator interfaces. These features have also been demonstrated with poly-Si thin-film transistor (TFT) [5-7], which are suitable for monolithic three-dimensional (3D) vertically stacked integrated circuits (ICs), which continue the applicability of Moore's law [8]. However, the JL channel

thickness should be thin enough to turn off the JL devices. This limits the saturation current of the junctionless thin-film transistor (JL-TFT) [7,9]. Meanwhile, it adversely increases series resistance in the S/D and decreases drain current. In order to conquer this issue, the raised source-and-drain (raised S/D) structure is used for this works.

In this work, the thin-channel structure trimmed by oxidation and HF is used for turning off the devices, and the raised S/D structure is built for high saturation current. A dual-gate structure can be applied in multi-threshold voltage (multi-V_{th}) applications [10], and its temperature is discussed for the p-type raised S/D JL-TFTs.
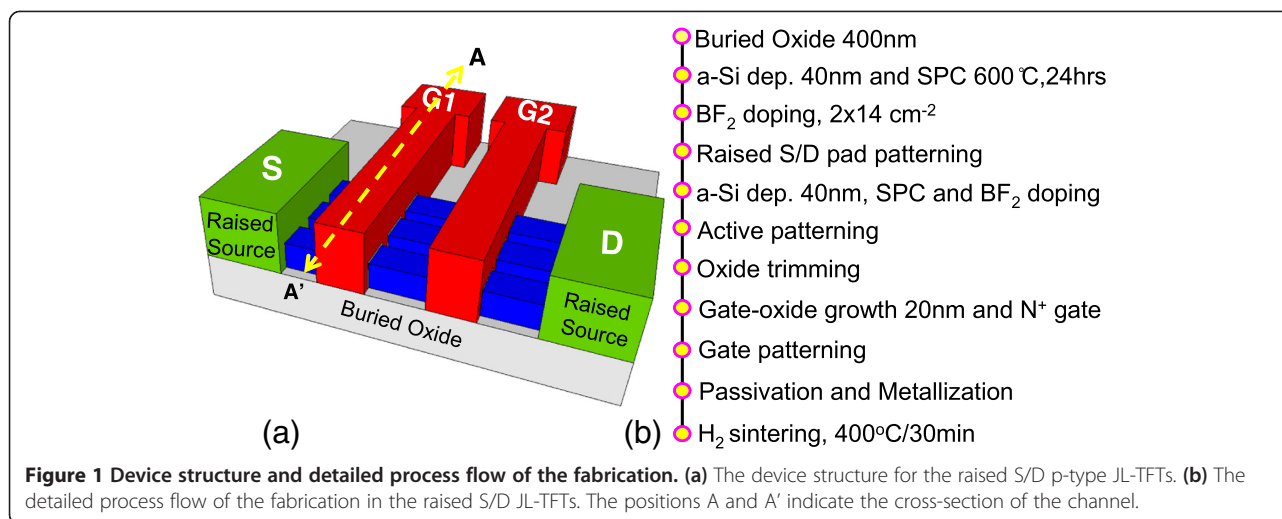
Methods
Device fabrication and experiment
Figure 1a schematically presents the proposed device structure of the raised S/D JL-TFT, and Figure 1b shows the detailed process flows of the fabrication in the raised

* Correspondence: ycwu@ess.nthu.edu.tw
[1]Department of Engineering and System Science, National Tsing Hua University, 101, Section 2, Kuang Fu Road, Hsinchu 30013, Taiwan
Full list of author information is available at the end of the article

Figure 1 Device structure and detailed process flow of the fabrication. (a) The device structure for the raised S/D p-type JL-TFTs. **(b)** The detailed process flow of the fabrication in the raised S/D JL-TFTs. The positions A and A' indicate the cross-section of the channel.
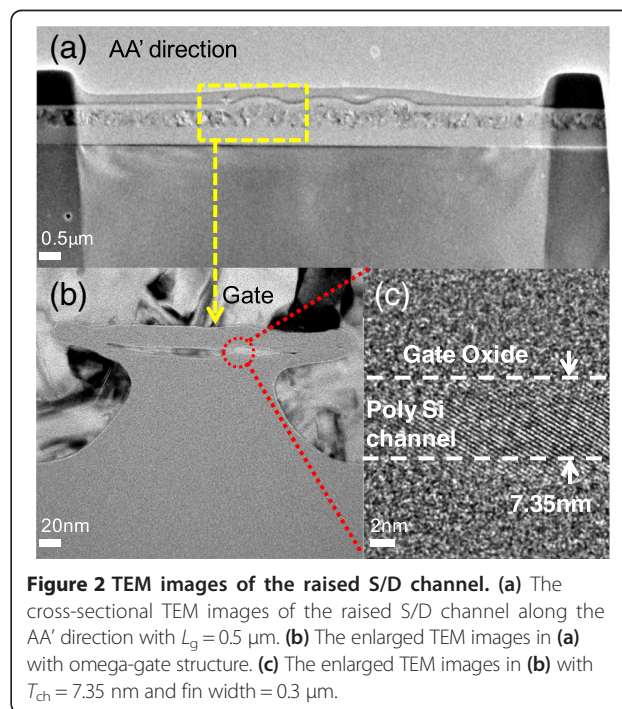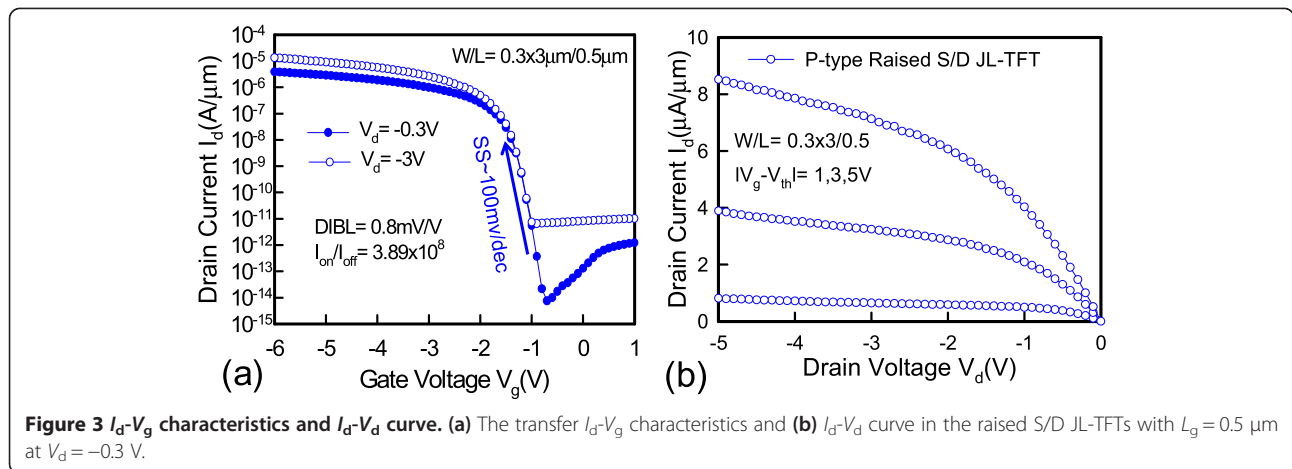
S/D JL-TFT. The p-type raised S/D JL-TFT is fabricated by initially growing a 400-nm thermal silicon dioxide layer on a 6-in. silicon wafer. A 40-nm amorphous Si (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C. Then, the a-Si layer was formed by solid-phase recrystallized (SPC) process at 600°C for 24 h in nitrogen ambient. After borondifluoride (BF_2) ion implantation with 30 keV at a dose of 2×10^{14} cm^{-2} for the p^+ raised S/D doping followed by furnace annealing at 600°C for 4 h, the raised S/D is patterned by e-beam lithography. Subsequently, using the same method for the production of a-Si deposition (40 nm), the implantation (30 keV, BF_2, 2×10^{14} cm^{-2}) and the SPC process form the channel layer. While serving as a channel, the active layer was patterned by e-beam lithography and then anisotropically etched by time-controlled reactive ion etching (RIE). The patterned width of each nanosheet channel is 0.3 μm. Then, the active channel was mesa-etched by time-controlled wet etching of dilute HF to form the omega-shaped channel. Next, a sacrificial oxide as a trimming process was thermally grown at 900°C for 2 h, which consumes around 22-nm-thick poly-Si. Subsequently, the dry oxide of 20-nm thickness was deposited as the gate oxide layer, consuming around 10-nm-thick poly-Si to form a 7.35-nm-thick channel. The 150-nm-thick *in situ* doped n^+ poly-silicon was deposited as a gate electrode and patterned by e-beam and RIE. Additionally, a 200-nm SiO_2 passivation layer was deposited. Finally, a 300-nm-thick Al-Si-Cu metallization was performed and sintered at 400°C for 30 min.

Results and discussion

Figure 2a shows the cross-sectional transmission electron microscopic (TEM) image along the AA' direction,

as shown in Figure 1a. Figure 2b,c displays the enlarged images of Figure 2a. The nano-sheet channel of the raised S/D structure is covered by the omega-gate electrode, which is expected to improve electrostatic gate control and achieve superior performance [11]. Figure 2c clearly shows that the nano-sheet channel thickness is 7.35 nm, and the TEM photograph shows that the single-crystal-like channel with large grain size is expected to achieve superior performance because of the oxidation
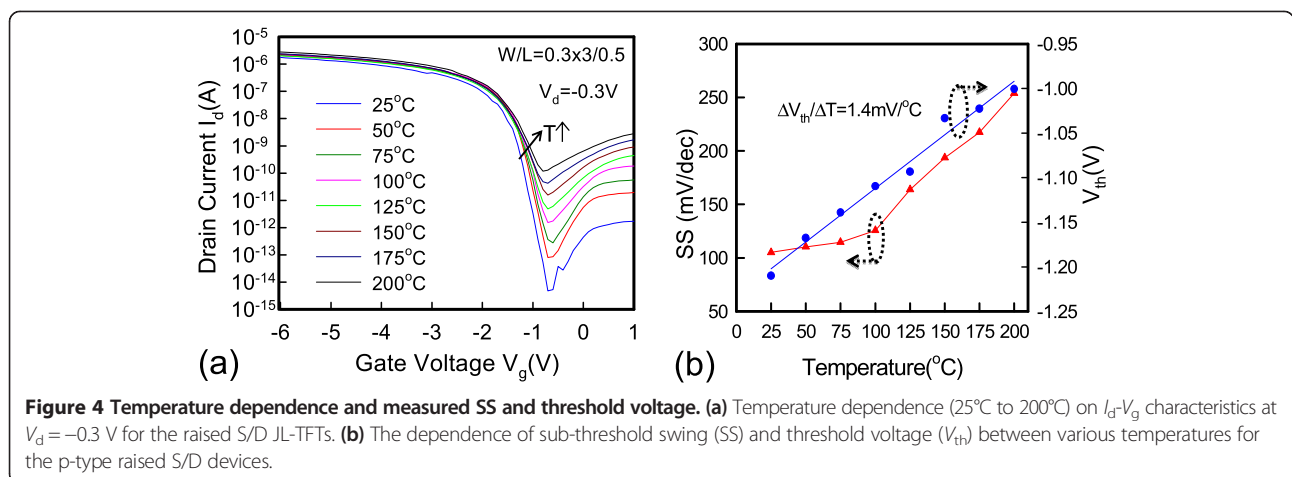

Figure 2 TEM images of the raised S/D channel. (a) The cross-sectional TEM images of the raised S/D channel along the AA' direction with $L_g = 0.5$ μm. **(b)** The enlarged TEM images in **(a)** with omega-gate structure. **(c)** The enlarged TEM images in **(b)** with $T_{ch} = 7.35$ nm and fin width = 0.3 μm.

Figure 3 I_d-V_g characteristics and I_d-V_d curve. (a) The transfer I_d-V_g characteristics and **(b)** I_d-V_d curve in the raised S/D JL-TFTs with $L_g = 0.5$ μm at $V_d = -0.3$ V.

trimming process. The channel region is doped with a boron concentration of 4×10^{19} cm^{-3}. Figure 3a plots the transfer I_d-V_g characteristics of the raised S/D JL-TFT with $L_g = 0.5$ μm. The on current (I_{on}) is defined as the drain current at $V_g = -6$ V for the raised S/D JL-TFT. The off current (I_{off}) is defined as the lowest drain current. The excellent transfer characteristics of the raised S/D JL-TFT with $L_g = 0.5$ μm include the following: (1) subthreshold swing (SS) = 100 mV/decade, (2) DIBL = 0.8 mV/V, and (3) I_{on}/I_{off} current ratio = 3.85×10^8. Figure 3b shows the I_d-V_d output characteristics of the raised S/D JL-TFT. The on resistance is low at various over-drive voltages with the raised S/D structure. Figure 4a demonstrates the temperature dependence of the raised S/D JL-TFT. Based on the I_d-V_g curves in Figure 4a, Figure 4b presents the measured SS and threshold voltage (V_{th}) as functions of temperature at $V_d = -0.3$ V. This figure reveals that, as the temperature increases,

the absolute V_{th} value decreases and the SS increases. The positive shifting of V_{th} for the raised S/D device is discussed in Figure 4b. The V_{th} is defined as the gate voltage at $I_d = 10^{-9}$ A. The V_{th} equation could be presented as the following [12]:
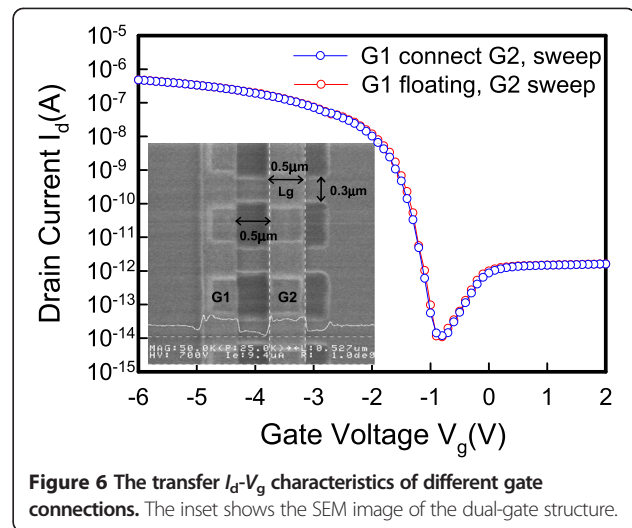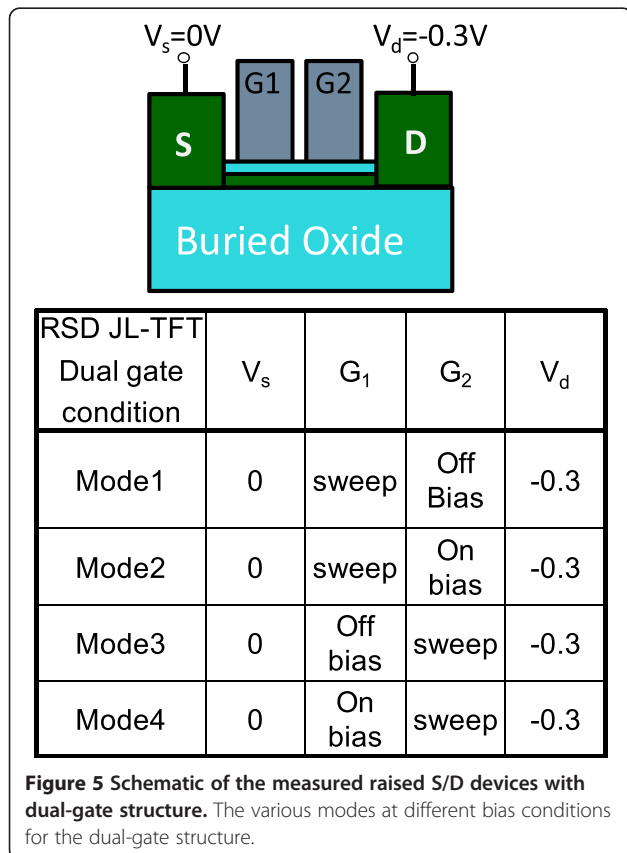
$$V_{th} = V_{fb} + \frac{qN_A W_D{}^2}{\varepsilon_{Si}} + \frac{qN_A W_{ch} W_D}{C_{ox}} - \frac{\pi^2 \hbar^2}{2qm_h^*}\left[\frac{1}{T_{ch}{}^2} + \frac{1}{W_{ch}{}^2}\right]$$

(1)

where V_{fb} is the flat-band voltage, C_{ox} is the gate capacitance per unit of length, N_A is the carrier concentration, W_D is the depletion width, W_{ch} is the effective channel width, T_{ch} is the channel thickness, and m_h^* is the effective mass of the confined holes. When the device is heated, the bandgap (E_g) decreases. Therefore, N_A increases. For

Figure 4 Temperature dependence and measured SS and threshold voltage. (a) Temperature dependence (25°C to 200°C) on I_d-V_g characteristics at $V_d = -0.3$ V for the raised S/D JL-TFTs. **(b)** The dependence of sub-threshold swing (SS) and threshold voltage (V_{th}) between various temperatures for the p-type raised S/D devices.

the above reasons, absolute V_{th} is expected to decrease with increasing temperature. Notably, the temperature dependence of the threshold voltage for the poly-channel device is 1.4 mV/°C. This value is close to the V_{th} temperature dependence of the single-crystal channel (1.65 mV/°C) [13].

Figure 5 shows the dual-gate structure with different operation modes. In mode 1, G1 is sweeping, G2 has an off-state bias condition, and V_d is applied at −0.3 V. In mode 2, G1 is sweeping, and G2 has an on-state bias condition. The reverse conditions for G1 and G2 occur in mode 3 and mode 4. Figure 6 shows the I_d-V_g characteristics. The red line represents that G1 is floating and G2 is sweeping. The blue line represents that G1 connects G2 and they are sweeping simultaneously. The experimental data show a good match in the I_d-V_g curves, which indicates that the series resistance between G1 and G2 is insignificant and does not degrade electrical performance. The inset in Figure 6 shows the scanning electron microscope (SEM) image of the dual-gate structure. The distance between the dual gate is 0.5 μm. Figure 7 depicts the I_d-V_g curves for different operation modes. The electrical performances for mode 1 and mode 2 are similar to those for mode 3 and mode 4 at V_d = −0.3 V. Figure 7a,c shows that, when the G2 and G1 approaches off-state bias

Figure 6 The transfer I_d-V_g characteristics of different gate connections. The inset shows the SEM image of the dual-gate structure.
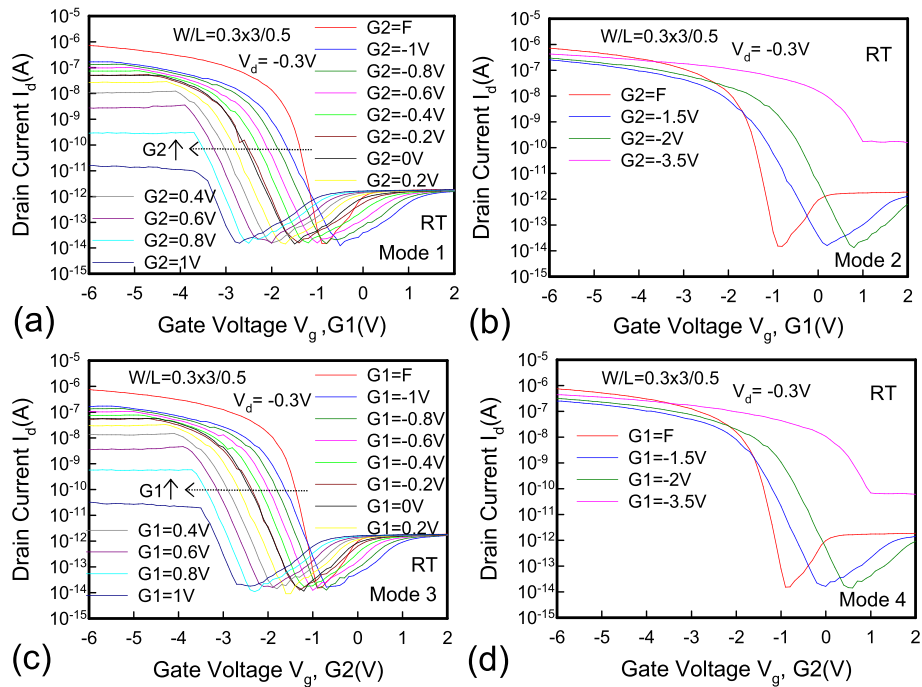
condition, the on current is clearly pinning and absolute V_{th} is increasing. Figure 7b,d shows that, when the G2 and G1 approaches on-state bias condition, the on current is increasing and the absolute V_{th} is decreasing. In Figure 8a, the V_{th} can be adjusted by the dual-gate structure applying different gate bias. In Figure 8b, the V_{th} sensitivity of G2 bias is approximately 1.23 V/V, and the experimental data show that the relationship is linear. The detailed results are discussed by 3D TCAD simulation in Figure 9. To obtain accurate numerical results for a nanometer-scale device, the device is simulated by solving 3D quantum-corrected equations using the commercial tool, Synopsys Sentaurus Device [14]. In quantum-corrected equations, a density gradient model is used in the simulation, as listed below [15,16]:

$$n = NcF_{1/2}\left(\frac{E_{F,n}-Ec-\Lambda_n}{KT_n}\right)$$
$$\Lambda_n = -\frac{\gamma\hbar^2}{12m_n}\left[\nabla^2 \ln n + \frac{1}{2}(\nabla \ln n)^2\right] \quad (2)$$

where n is the electron concentration, Nc is the effective density of states of the conduction band (Ec), $F_{1/2}$ is the Fermi-Dirac integral, μn is the effective mass of the electron, and T_n is the electron temperature. The bandgap narrowing model, the band-to-band tunneling model, and the Shockley-Read-Hall recombination with the doping-dependent model are also considered. The direct tunneling model is not utilized because high-*k*/metal-gate technology is used. The mobility model used in the device simulation is according to Mathiessen's rule, which is expressed as

$$\frac{1}{\mu} = \frac{D}{\mu_{surf\_aps}} + \frac{D}{\mu_{surf\_rs}} + \frac{1}{\mu_{bulk\_dop}} \quad (3)$$
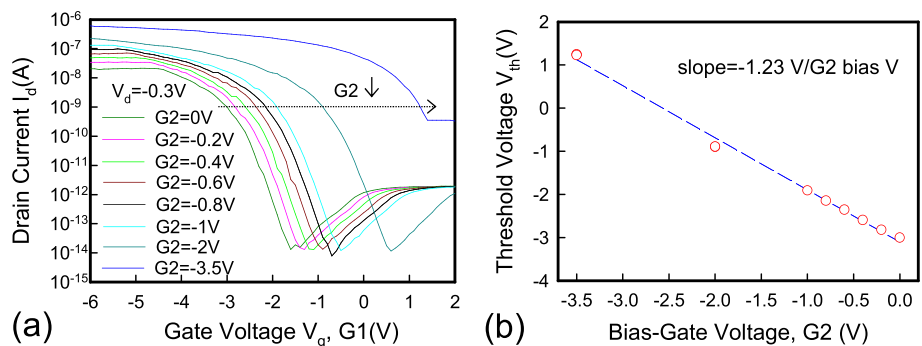

RSD JL-TFT Dual gate condition	V_s	G_1	G_2	V_d
Mode1	0	sweep	Off Bias	-0.3
Mode2	0	sweep	On bias	-0.3
Mode3	0	Off bias	sweep	-0.3
Mode4	0	On bias	sweep	-0.3

Figure 5 Schematic of the measured raised S/D devices with dual-gate structure. The various modes at different bias conditions for the dual-gate structure.

Figure 7 The transfer I_d-V_g characteristics for various modes (a-d), listed in Figure 5.

where $D = \exp(x/l_{crit})$, x is the distance from the interface, and l_{crit} is a fitting parameter. The mobility consists of three parts: 1) surface acoustic phonon scattering (μ_{surf_aps}), 2) surface roughness scattering (μ_{surf_rs}), and 3) bulk mobility with doping-dependent modification (μ_{bulk_dop}). The details are described in [14,17]. Figure 9a shows the high off current when G1 is sweeping at 2 V and G2 is at on-state bias of −3.5 V. When the G2 is in extreme on-state, band-to-band tunneling occurs easily according to the simulation results. Figure 9b shows the pinning mechanism when G1 is sweeping and G2 is at

off-state bias. When the G2 voltage approaches off-state, the valence band will be dropped off, which retards the hole transport and causes a saturation current. Figure 10 shows the temperature characteristics of the dual-gate structure. High-temperature performance is similar to that at room temperature.

Conclusions

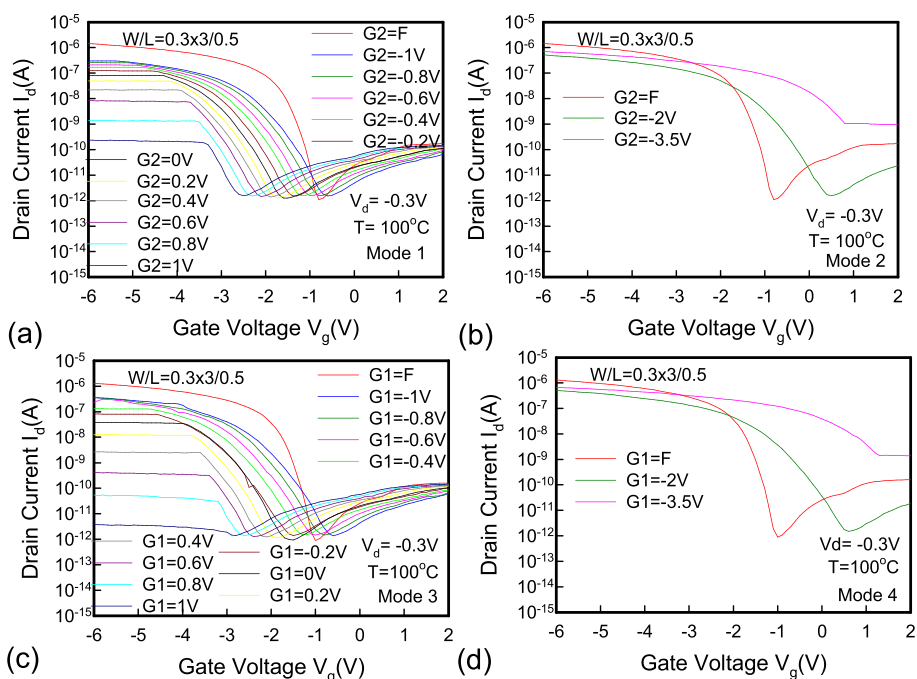This work realizes the p-type raised S/D JL-TFTs and dual-gate structure. In our devices, the thin channel

Figure 8 Transfer I_d-V_g characteristics and G2 bias dependence. (a) The transfer I_d-V_g characteristics at different G2 gate bias. **(b)** The impact of G2 bias dependence on the V_{th} for the raised S/D JL-TFTs.

Figure 9 Simulation results at (a) G1 = 1 V, G2 = −4 V for mode 2 situation and (b) G1 = −4 V, G2 = 1 V for mode 1 situation.

formed by the oxidation trimming process and raise S/D structure are used. Due to these two ideas, the high on current (>1 μA/μm), low off current (10^{-14} A), and small SS (100 mV/decade) could be achieved. It is a promising structure to get a good-performance JL device and conquer the low-I_{on} issue of JL devices. The temperature of the raised S/D devices is discussed for the electrical parameters (SS, V_{th}). It is worthy to notice that the dual-gate structure can be used to adjust V_{th} to fulfill the multi-V_{th} circuit designs. The devices are highly promising for future further scaling and 3D stacked IC applications.

Figure 10 The temperature dependence of dual-gate JL-TFTs at 100°C on I_d-V_g characteristics (a-d).

Competing interests

Authors' contributions

Y-CC and H-BC handled the experiment and drafted the manuscript. J-JS, C-SS, and C-PW fabricated the samples and carried out the electrical characterization. Y-CW supervised the work and reviewed the manuscript. C-YC participated in the design and coordination of the study. All authors read and approved the final manuscript.

Acknowledgements

Author details

[1]Department of Engineering and System Science, National Tsing Hua University, 101, Section 2, Kuang Fu Road, Hsinchu 30013, Taiwan. [2]Department of Electronics Engineering, Institute of Electronics, National Chiao Tung University, 1001, Ta Hsueh Road, Hsinchu 30013, Taiwan.

References

1. Lee CW, Afzalian A, Akhavan ND, Yan R, Ferain I, Colinge JP: **Junctionless multigate field-effect transistor.** *Appl Phys Lett* 2009, **94**:053511.
2. Colinge JP, Lee CW, Afzalian A, Akhavan ND, Yan R, Ferain I, Razavi P, O'Neil B, Blake A, White M, Kelleher AM, McCarthy B, Murphy R: **Nanowire transistors without junctions.** *Nat Nanotechnol* 2010, **5**:225.
3. Colinge JP, Lee CW, Ferain I, Akhavan ND, Yan R, Razavi P, Yu R, Nazarov AN, Doria RT: **Reduced electric field in junctionless transistors.** *Appl Phys Lett* 2010, **96**:073510.
4. Rios R, Cappellani A, Armstrong M, Budrevich A, Gomez H, Pai R, Rahhal-orabi N, Kuhn K: **Comparison of junctionless and conventional trigate transistors with Lg down to 26 nm.** *IEEE Electron Device Lett* 2011, **32**:1170.
5. Lin HC, Lin CI, Huang TY: **Characteristics of n-type junctionless poly-Si thin-film transistors with an ultrathin channel.** *IEEE Electron Device Lett* 2012, **33**:53.
6. Su CJ, Tsai TI, Liou YL, Lin ZM, Lin HC, Chao TS: **Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels.** *IEEE Electron Device Lett* 2011, **32**:521.
7. Chen HB, Chang CY, Lu NH, Wu JJ, Han MH, Cheng YC, Wu YC: **Characteristics of gate-all-around junctionless poly-Si TFTs with an ultrathin channel.** *IEEE Electron Device Lett* 2010, **34**:897.
8. Choi SJ, Han JW, Kim S, Moon DI, Jang M, Choi YK: **A novel TFT with a laterally engineered bandgap for of 3D logic and flash memory.** *VLSI Symp Tech Dig* 2010, 111. doi:10.1109/VLSIT.2010.5556191.
9. Lin HC, Lin CI, Lin ZM, Shie BS, Huang TY: **Characteristics of planar junctionless poly-Si thin-film transistors with various channel thickness.** *IEEE Trans Electron Devices* 2013, **60**:1142.
10. Kursun V, Friedman EG: *Multi-voltage CMOS Circuit Design.* New York: Wiley; 2007.
11. Barraud S, Coquand R, Cassé M, Koyama M, Hartmann J-M, Maffini-Alvaro V, Comboroure C, Vizioz C, Aussenac F, Faynot O, Poiroux T: **Performance of omega-shaped-gate silicon nanowire MOSFET with diameter down to 8 nm.** *IEEE Electron Device Lett* 2012, **33**:1526.
12. Trevisoli RD, Doria RT, De SM, Pavanello MA: **Threshold voltage in junctionless nanowire transistors.** *Semicond Sci Technol* 2011, **26**:1.
13. Lee CW, Borne A, Ferain I, Afzalian A, Yan R, Akhavan ND, Razavi P, Colinge JP: **High-temperature performance of silicon junctionless MOSFETs.** *IEEE Trans Electron Devices* 2010, **57**:620.
14. Synopsys: *TCAD Sentaurus Device, Ver. E-2010.12.* Mountain View: Synopsys, Inc; 2011.
15. Walker A, Jeffrey FW, Gilbert A, Karin H: *User's Manual for Synopsys Sentaurus Device.* Ottawa: 2010.
16. Ancona MG, Iafrate GJ: **Quantum correction to the equation of state of an electron gas in a semiconductor.** *Phys Rev B* 1989, **39**:9536.
17. Reggiani S, Valdinoci M, Colalongo L, Rudan M, Baccarani G, Stricker AD, Illien F, Felber N, Fichtner W, Zullino L: **Electron and hole mobility in silicon at large operating temperatures. I. Bulk mobility.** *IEEE Trans Electron Devices* 2002, **49**:490.