A Fully Integrated Nose-on-a-Chip for Rapid Diagnosis of Ventilator-Associated Pneumonia

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***Abstract*—Ventilator-associated pneumonia (VAP) still lacks a rapid diagnostic strategy. This study proposes installing a nose-on-a-chip at the proximal end of an expiratory circuit of a ventilator to monitor and to detect metabolite of pneumonia in the early stage. The nose-on-a-chip was designed and fabricated in a 90-nm 1P9M CMOS technology in order to downsize the gas detection system. The chip has eight on-chip sensors, an adaptive interface, a successive approximation analog-to-digital converter (SAR ADC), a learning kernel of continuous restricted Boltzmann machine (CRBM), and a RISC-core with low-voltage SRAM. The functionality of VAP identification was verified using clinical data. In total, 76 samples infected with pneumonia (19 Klebsiella, 25 Pseudomonas aeruginosa, 16 Staphylococcus aureus, and 16 Candida) and 41 uninfected samples were collected as the experimental group and the control group, respectively. The results revealed a very high VAP identification rate at 94.06% for identifying healthy and infected patients. A 100% accuracy to identify the microorganisms of Klebsiella, Pseudomonas aeruginosa, Staphylococcus aureus, and Candida from VAP infected patients was achieved. This chip only consumes 1.27 mW at a 0.5 V supply voltage. This work provides a promising solution for the long-term unresolved rapid VAP diagnostic problem.**

***Index Terms*—Continuous restricted Boltzmann machine (CRBM), gas classification, nose-on-a-chip, ventilator-associated pneumonia (VAP).**

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I. Introduction

VENTILATED patients are easily infected to cause pneumonia because of various types of bacteria, leading to septicemia shock, cardiopulmonary failure, and even death. The mortality rate for ventilator-associated pneumonia (VAP) [1], [2] lies between 20% and 50%, and can be even higher in certain intensive care units (ICUs). The standard operating procedure involves conducting a chest X-ray, drawing blood, and performing a sputum culture, and then treating the patient with antibiotics for the suspected microorganisms, based on the experience of the treating physician [3]. It is usually unclear if the antibiotics are effective when culturing a specimen in the first 5 days, the most crucial period for patient survival, as shown in Fig. 1(a).

Breath of patients has recently been used to detect pneumonia infections [4], [5]. Paramedics have noticed a distinct odor from patients that are infected with VAP, which offers a possibility for fast pneumonia infection detection. By detecting the smell, pneumonia can be identified more easily. However, conventional gas-analysis methods require examining the gas samples in the laboratory using either a gas chromatography mass spectrometry (GC-MS) analyzer [6] or a Fourier infrared spectrometer (FT-IR) [7]. Although GC-MS and FTIR offer relatively accurate results, they do not suit for monitoring in daily life since these instruments are bulky and the procedure is time consuming. A light-weight device with fast and accurate detection is therefore crucial for gas analysis in detecting VAP. The electronic nose (e-nose) offers an alternative for gas identification. The e-nose uses an array of sensors to acquire the specific response pattern for each type of gas, and identifies this specific pattern for disease identification [8], [9]. The e-nose has recently been widely adopted for diagnosis, including for dermal drugs, lung cancer, kidney disease, reproduction medication, diabetes, and asthma [10], [11]. Although e-noses are available in the market, the current products are still not popular owing to its massive volume and high cost regarding personal healthcare applications [12]–[15].

Fig. 1(b) shows the application scenario for fast detection by examining metabolic waste at the proximal end of the expiratory device by using a miniaturized, battery-powered, gas-sensing device. This enables real-time monitoring and rapid diagnosis of VAP, thereby reducing the mortality rate caused by this problem in ICUs. To minimize the form factor of the gas-sensing system, a nose-on-a-chip is proposed in this work. A fully integrated

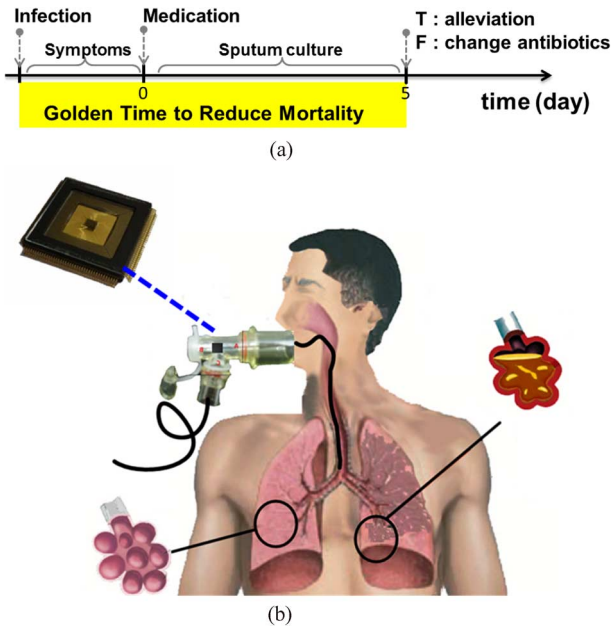


Fig. 1. (a) Standard operating procedure for VAP treatment. (b) Target application scenario for rapid VAP diagnosis.

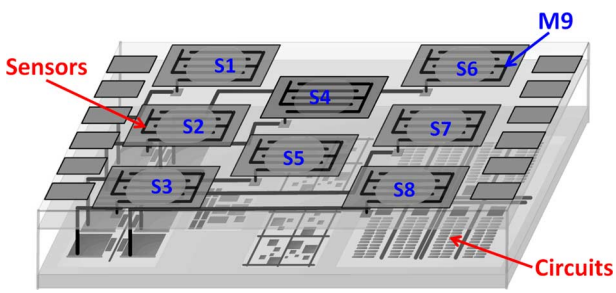


Fig. 2. The 3D structure of the proposed nose-on-a-chip.

low-power nose-on-a-chip [16] with a robust learning kernel is developed to meet this vital clinical requirement.

II. Chip Architecture

The proposed nose-on-a-chip integrates sensors and related circuits into one chip. The sensors form an array to generate a specific response pattern corresponding to the incoming gas. The related circuits acquire the sensor signals and process the sensed data. Fig. 2 shows the 3D structure of the proposed chip. Lower-layer metals (M1 to M8) are used for the circuits, and the top metal (M9) is used for the sensing electrodes. In the design stage, sensory areas are defined using the PAD mask to remove silicon nitride. Thus, the sensing materials can be coated on the electrodes to form the on-chip sensors. Polymer-carbon composites are adopted for the sensing materials [17], [18]. Regarding the sensing materials, carbon particles provide stable electrical conductivity, while various organic polymers on the chemical sensor array provide gas selectivity. When the sensor is exposed to gas, if the polymer reacts with the incoming molecule, the composite swells and forms a longer conduction path, resulting in an increased resistance. Unlike the traditional circuit-integrated compatible sensors such as metal-oxide, which

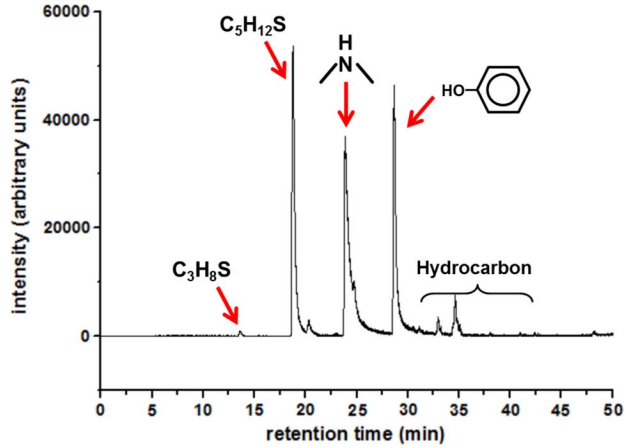


Fig. 3. GS-MS analysis result of *in vitro* VAP experiment for Enterobacter aerogenes at the 24th hour.

can only be operated at high temperature, this kind of chemiresistive sensor functions at room temperature. The chemiresitive sensor also features low power consumption and is highly compatible with CMOS technology without requiring a specific (e.g., MEMS) process. The electronic circuits are implemented underneath the on-chip sensors for signal acquisition, gas classification, and system operation.

III. Sensors for the Nose-on-a-Chip

A. Target Gas Identification

VAP *in vitro* experiments were conducted to determine the target gases in order to choose the corresponding sensing materials. Ten of the most common germs (Escherichia coli, Klebsiella oxytoca, Acinetobacter baumannii, Klebsiella pneumoniae, Stenotrophomonas maltophilia, Proteus mirabilis, Enterobacter aerogenes, Enterobacter cloacae, Pasteurella multocida, and Staphylococcus aureus) were collected and cultured. The bacterial culture was placed in a 1000 mL sample bag with 5% CO_2 and 95% air in an incubator at 37°C, and then the metabolized gas was collected to conduct GC-MS for 2, 4, 6, and 24 hours. The results revealed that carbide, sulfide, and ammonia are target gases for VAP detection [19], [20]. A sample analysis result is shown in Fig. 3.

B. On-Chip Sensor Array

Composites of polymer and carbon are proposed as sensing materials such that the sensors can operate at room temperature. Insulating polymers and carbon materials serve for gas selectivity and electrical conduction path, respectively. Carbon black and carbon nanotubes are commonly used as carbon materials. Mesoporous carbon [21], [22] is another appropriate candidate. For the nanocomposites of mesoporous carbon and the various types of polymer directly grown on carbon, in such a nanoscale design, the nanocomposites allow analyte molecules to diffuse and directly interact with the polymer materials. Consequently, the nanocomposites have an enhanced sensitivity and reversibility for gas detection compared with dense polymer films. Eight different polymers with various functional groups were selected in this work.

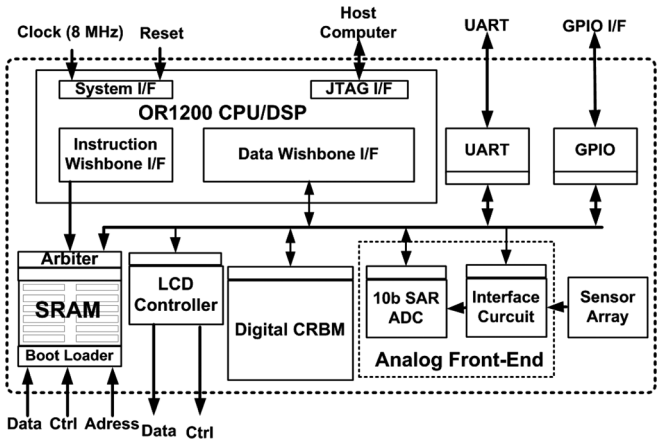
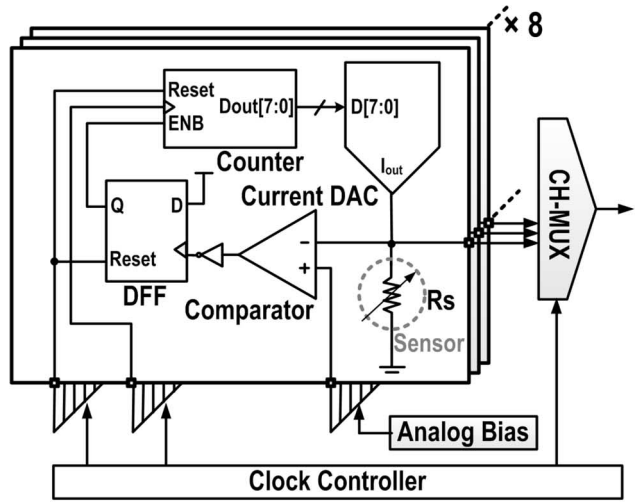
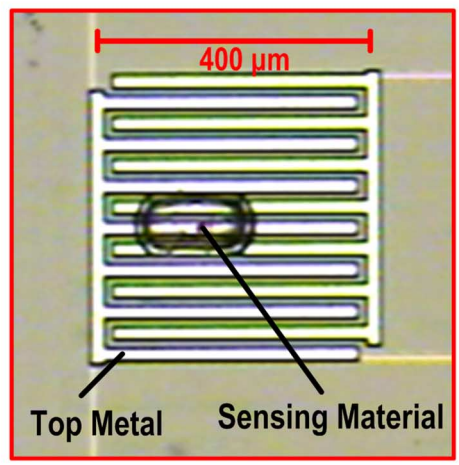


Fig. 4. System block diagram of the proposed nose-on-a-chip.



(a)



(b)

Fig. 5. (a) Schematic of the 8-channel adaptive interface circuit. (b) Zoom-in view of the on-chip sensor.

Material deposition must be conducted more carefully since the size of an on-chip sensor is much smaller than that of a discrete sensor. First, the sensing material was deposited after undergoing homogenous sonication. Even so, the nanocomposite material might not be distributed uniformly to form a conductive path between the electrodes. An interdigitated, rather than a two-lead, electrode structure is adopted to resolve this problem. In the proposed design, the CB mask with $400 \times 400\ \mu\mathrm{m}^2$ was used to define the sensing material titration region. After chip fabrication, the silicon nitride protective layer, which is enclosed using the CB mask, was removed [23], and the materials were deposited on the electrodes.

IV. Microelectronics for the Nose-on-a-Chip

A. System Block Diagram

The system block diagram of the proposed nose-on-a-chip is shown in Fig. 4. The nose-on-a-chip comprises six parts: an array of integrated sensors, a sensor interface circuit, a 10-bit SAR analog-to-digital converter (ADC), a reduced instruction set computing (RISC)-core processor (OR1200), a continuous restricted Boltzmann machine (CRBM) kernel as a specific digital signal-processing unit for data clustering, and an 8 K × 32 b SRAM. The chip integrates eight sensors on the surface and processing circuits at the bottom in a standard CMOS process without any post-MEMS fabrication.

B. Adaptive Interface Circuitry

The resistance of the polymer-carbon composite sensor usually shifts with temperature, humidity, and background odors. An interface circuit that can adapt to sensor resistances is therefore required to eliminate potential shifts in sensor resistance caused by nonideal environmental interferences [24], [25].

The schematic of the adaptive interface circuit for canceling the baseline signal is shown in Fig. 5(a). A zoom-in view of the on-chip sensor is shown in Fig. 5(b). The adaptive interface comprises a comparator, a D-flip-flop, an 8-bit counter, and an 8-bit digital-to-analog converter (DAC). Through a feedback loop, and using the counter and current DAC as a controllable current source, the interface circuit can bias the sensor voltage with various initial resistances to a preset voltage. The multiplexor (CH-MUX) selects the sensor signal from eight different channels, and the selected signal is then sent to the SAR-ADC. This circuit is operated in the following two modes: 1) adaptive mode: the D-flip-flop and counter are reset first, the counter then begins counting up, and the value of the sensor voltage $\mathrm{V_s}$ starts increasing. When the sensor voltage $\mathrm{V_s}$ reaches the reference voltage $\mathrm{V_{ref}}$, the counter stops, and the feedback loop is broken; and 2) sensing mode: the sensor signals are read out when the sensor is exposed to the test gas. In this mode, the sensor is biased by a constant current set by the counter, and thus, the relationship between $\mathrm{V_s}$ and $\mathrm{R_s}$ is as shown in (2). The change of the sensor voltage $(\Delta \mathrm{V_s}/\mathrm{V_{ref}})$ is proportional to the percentage change of the sensor resistance $(\Delta \mathrm{R_s}/\mathrm{R_{s0}})$, as shown in (4)

$$V_{adp0} = R_{S0} \cdot I_{Bias} \cdot N_{counter} \tag{1}$$

$$V_{adp.gas} = (R_{S0} + \Delta R_S) \cdot I_{Bias} \cdot N_{counter} \tag{2}$$

$$V_{adp.gas} = \left(1 + \frac{\Delta R_S}{R_{S0}}\right) \cdot V_{adp0} \tag{3}$$

$$\Delta V_S = V_{adp.gas} - V_{adp0} = \frac{\Delta R_S}{R_{S0}} \cdot V_{adp0} \tag{4}$$

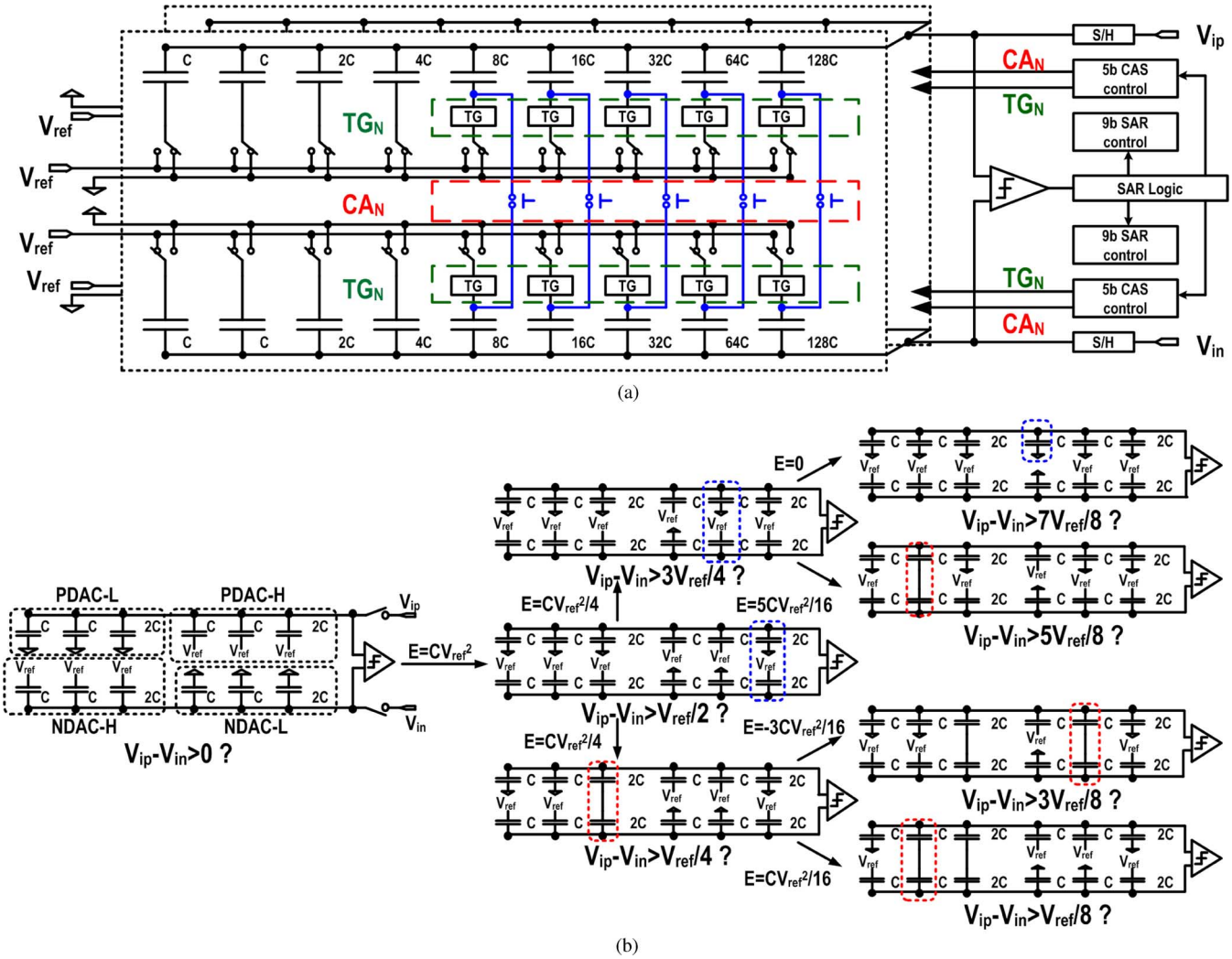


Fig. 6. (a) The SAR ADC circuit diagram. (b) The CAS DAC with a 4b conversion example.

where V_{adp0} is the adapted voltage after baseline signal cancellation, R_{s0} is the initial resistance of the sensor, I_{Bias} is the unit current of the DAC, $N_{Counter}$ is the counted number after adaptive mode, $V_{adp.gas}$ is the sensor voltage after gas-sensing, ΔR_s is the resistance increment after gas-sensing, and ΔV_s is the sensor voltage increment after gas-sensing. By solving (4), the information containing $\Delta R_s/R_{s0}$, which is considered as the odor data subject to further analysis, is obtained.

C. SAR Analog-to-Digital Converter

Inherently, a successive-approximation register (SAR) ADC has high power efficiency in the low-voltage operation. In the proposed nose-on-a-chip, it requires an ADC that operates at hundreds of kS/s to a few MS/s with medium resolution (8 to 12b). The DAC switch array and the SAR controller are the main power-hungry blocks in SAR ADC designs. A 0.5 V 10b asynchronous SAR ADC is implemented in this work. The supply voltage is scaled down appropriately for different speeds to minimize power consumption of SAR control and DAC switching energy. Moreover, a charge average switching (CAS) DAC [26] is adopted to reduce the switching energy of the DAC without extra voltage reference and common-mode shift. In the near-threshold operation with a scaled-down supply, double-boosted sample-and-hold (S/H) circuits and local-boosted switches are implemented to achieve the 10b accuracy requirement.

Fig. 6(a) shows the circuit diagram of the implemented SAR ADC. The MSB capacitor (512C) is split into two sub-DAC arrays (128C to C). One sub-DAC array resets to ground and the other resets to Vref in the sampling phase for the following CAS procedure. A top-plate sampling technique is applied to effectively reduce the DAC switching energy. The CAS technique is to generate the required top-plate voltage shift through charge averaging between the bottom plates of PDAC and NDAC instead of the conventional charging/discharging operation. The charge-averaging function is achieved by enabling equalization switches from CAS control (by CA_N) rather than switching to the reference voltages. The on-resistance of CAS switching is increased severely in the operation for passing Vref/2 due to the near-threshold operation and unsufficient over-drive voltage headroom. Local-boosted switches are implemented for CA_N to ensure a completed averaging function without sacrificing speed and accuracy.

The CAS DAC with 4b conversion is illustrated in Fig. 6(b). First, the input signal is sampled on the top plates of P/N DAC

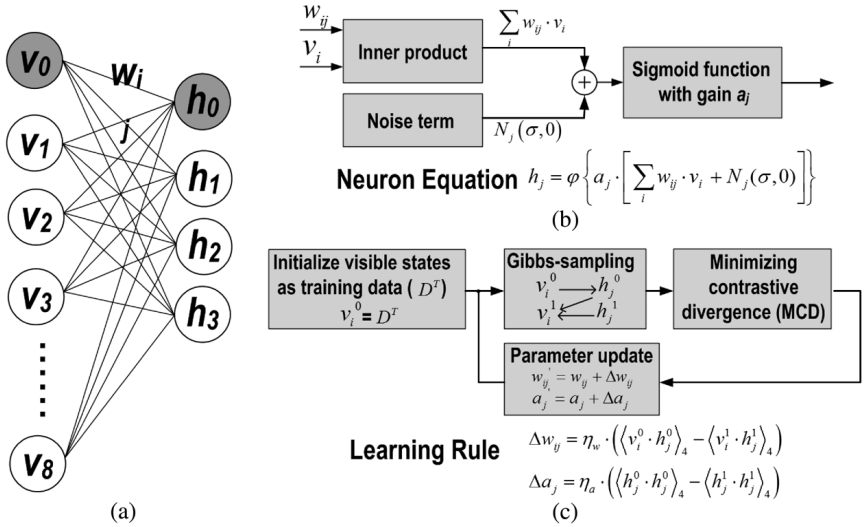


Fig. 7. The CRBM of a (a) neural network, (b) hidden space mapping process, and (c) learning process.

combined of PDAC-H/PADC-L and NDC-H/NDAC-L, respectively. In the sampling phase, the bottom plates of PDAC-H/NDAC-H and PDAC-L/NDAC-L are connected to Vref/Gnd respectively. For simplicity, the case with Vip $>$ Vin in the symmetric DAC switching procedure for the differential SAR ADC is shown. It shows that the required voltage for the following comparison is achieved by charge averaging operation of corresponding capacitor instead of complementary switching to Vref/Gnd. This 4b DAC conversion example demonstrates a 36.2% saving of DAC switching energy with CAS operation compared to conventional rail switching. With the optimized transistor sizing and careful layout, the power overhead of the required boosted control circuit is around 3% in the implemented 10b ADC.

D. Continuous Restricted Boltzmann Machine (CRBM) Kernel

In biomedical applications, raw sensory signals are typically high dimensional, noisy, and drifting. To facilitate an *in situ* diagnosis, a low-power embedded system is required to fuse sensory signals robustly in real time. A probabilistic neural network, called CRBM, has been shown to be capable of classifying biomedical data reliably [27], [28]. As advanced technology continues to involve shrinking transistors, transistor mismatches and nonlinearity increase significantly, such that the CRBM system requires complex analog circuits to achieve a sufficient resolution (10 bit) for parameter training. The complexity renders the analog design to lose power and area advantages over digital designs. In addition, transmitting analog signals precisely in a large-scale neural network is challenging because of the reduced supply voltage. The digital CRBM (dCRBM) system is immune to transistor mismatches and noise interferences, preserving a satisfactory precision for training the dCRBM on chip. In addition, digital implementation facilitates adapting and storing parameters in digital memory directly. The dCRBM system was integrated with an e-nose microsystem to perform dimensional reduction and data clustering on the sensory signals of the e-nose, which facilitate reliable data classification.

The CRBM consists of one visible and one hidden layer of stochastic neurons with interlayer connections as shown in Fig. 7(a). In the hidden space-mapping process of the CRBM as shown in Fig. 7(b), let v_i and h_j represent the states of neurons i and j, respectively. With $\{v_i\}$, the states of hidden neurons $\{h_j\}$ are derived using the neuron equation, where w_{ij} represents the connection weight between neurons i and j. The term N_j is a zero-mean Gaussian noise with variance σ^2, and φ is the sigmoid function. The CRBM learns to regenerate training examples as its visible states. Therefore, the number of visible neurons is equal to the dimension of the data to be modeled, and the number of hidden neurons is chosen based on the data complexity. During training as shown in Fig. 7(c), each training datum is set as the initial state of visible neurons, v^0. With v^0, the initial state of hidden neurons, h^0, is sampled. By sampling visible and hidden neurons alternatively once more to obtain the one-step sampled v^1 and h^1, the updated values for all parameters can be calculated according to this minimizing-contrastive-divergence (MCD) rule, where η_w and η_{a} are the learning rate, and $\langle\cdot\rangle_4$ denotes the expectation over four data. The parameter aj of visible neurons is updated by the same MCD, with h_j^0 and h_j^1 replaced by v_j^0 and v_j^1, respectively.

Fig. 8 shows the architecture of the dCRBM system [29]. Because the e-nose contains eight sensors, a pilot simulation indicated that a CRBM network of eight visible and three hidden neurons is required. Nevertheless, the dCRBM system actually contains only one multiplier, one accumulator/subtractor, one sigmoid circuit, and one noise generator. To reduce the circuit complexity, the nonlinear sigmoid function was approximated using piecewise-linear (PWL) curves. The noise term was realized using the linear-feedback shift register (LFSR) [30]. The LFSR generates a pseudo-random binary sequence, and the counter counts the number of "1"s during each of the 32 clock cycles. The counter output was then subtracted by 16 and divided by 2^N, resulting in a Bernoulli-distributed random value with a zero mean. The integer N controls the variance of the random value, corresponding to σ. The multiplier is designed to accept 10-bit inputs and generate a 20-bit output. The subtractor/

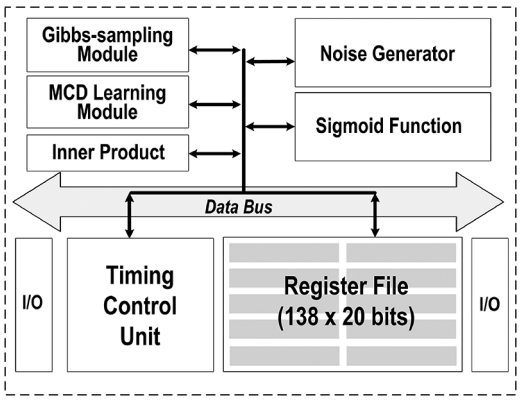


Fig. 8. The architecture of the dCRBM system.

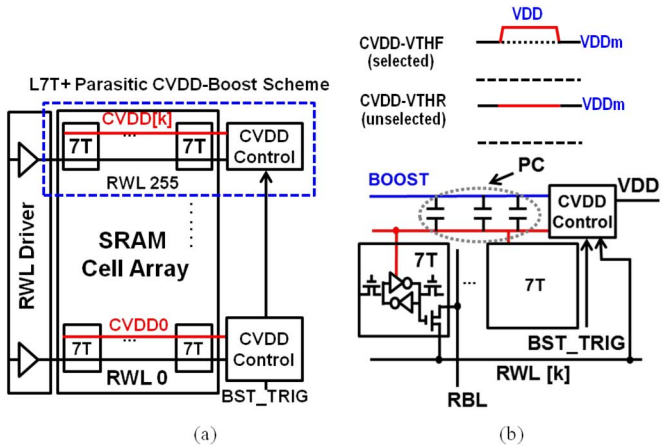


Fig. 10. (a) The SRAM macro and cell structure. (b) The BOOST-CVDD.

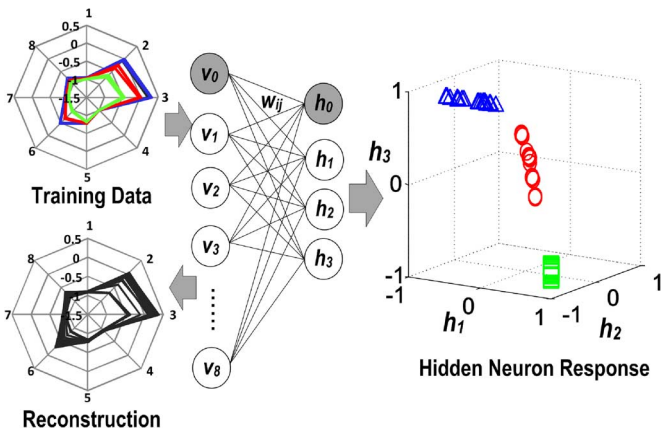


Fig. 9. Result of dCRBM training data, output results, and reconstruction pattern.

accumulator also maintains a 20-bit resolution for computations during training. The register file contains a memory capacity of 138 words $\times$ 20 bits for storing the parameters and the Gibbs sampled states during training of the dCRBM system [31].

The dCRBM system reduces the data dimension, enlarges the difference between data groups, and cooperates with the RISC-core for data processing. The dCRBM experimental results are shown in Fig. 9; three types of odor test were used to examine the capability of the dCRBM. The 8D radar plot revealed the sensory responses to the three types of odor. Each curve corresponds to the sensory response of one experimental trial. By adapting the connection weights $\{w_{ij}\}$ and the sigmoid gain $\{a_j\}$, the CRBM learned to regenerate training examples as the states of visible neurons. The CRBM kernel was trained to model three types of sensory data for 10,000 epochs, and it requires 4,926 clock cycles for each epoch. After training, the CRBM was able to reconstruct the training data as the states of visible neurons through Gibbs sampling. The similarities between the reconstruction and the training data indicated that the data were modeled appropriately. Moreover, the learning trajectories of all $\{a_j\}$ and $\{w_{ij}\}$ reached equilibrium after 5000 training epochs. The hidden neurons of the trained CRBM responded differently to sensory data, as shown by Fig. 9. The projection of data into the hidden space assisted in clustering the sensory data, and in reducing the data dimensions for reliable classification. The similarities between the reconstruction and the training data then indicated the adequacy of the data modeled. Finally, when entering three types of 8D gas data, the 3D output result revealed clear separation among these three odor types. Furthermore, the similarities were adequate between the reconstruction and the training data, indicating that the data were modeled appropriately.

E. Memory

Fig. 10 shows the SRAM macro and cell structure for a low-voltage system. To achieve a low VDDmin, this nose-on-a-chip employs a previously reported L-shaped 7T (L7T) SRAM cell, which consists of a 6T SRAM cell and a one-transistor (1T) read-decoupled read-port (RP) for preventing the read-disturbance problem [32]. However, this L7T cell suffers from a limited read bitline (RBL) voltage swing because of the BL clamping current from unselected RPs of the accessed column, particularly for a long-RBL. To increase the read margin/RBL swing without introducing an additional supply source, the gate bias of 1T-RP is increased by boosting the cell-VDD (CVDD) in a read cycle through the designed parasitic capacitors (PC) between metal lines (BOOST-CVDD) on top of SRAM cells. This parasitic boosted-CVDD (PBV) scheme introduces only 1% of the area overhead and less than 10% power overhead due to the added CVDD control logics. In standby mode, a high boost-enabled signal (BST_TRIG) is maintained. The level required for CVDD depends on the row address: 1) increased (CVDD-VTHF) for a larger ICELL (selected row); and 2) reduced (CVDD-VTHR) for a lower VRBL-L clamping point (unselected row). A reduced CVDD also helps suppress any RBL leakage caused by the negatively forced V_{GS} of RP in read-H. Thus, this paper proposes OFS-CVDD, which switches the power of CVDD to VDD, and VDDm for selected and unselected rows, respectively. In the precharge phase, the RBL precharge signal is activated to precharge RBL to VDD. After asserting the selected RWL, the VDD-precharged VRBL is boosted by VBST. This helps increase 1) the sensing margin for read-"H" by VBST; and 2) the cell current (ICELL) of RP for read-"L" because of boosted V_{DS}.

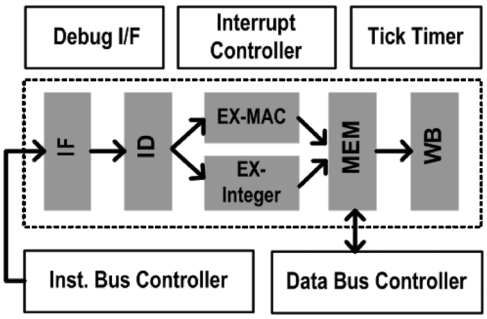


Fig. 11. The functional blocks of the RISC core.

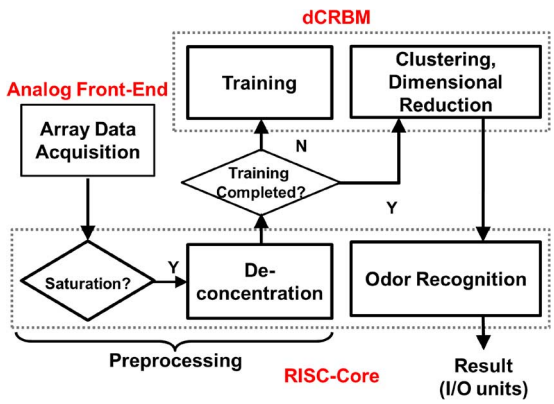


Fig. 12. Data flow of the system.

F. Reduced Instruction Set Computing Core (RISC-Core)

In the nose-on-a-chip, a RISC-core is used to meet the requirements of the microcontroller of the system and algorithm. An OpenRISC 1200 core, which is designed and implemented based on a scalar 32 bit RISC-core [33], [34], is adopted. The functional blocks of the RISC-core are depicted in Fig. 11. Apart from the five-stage integer pipeline, a multiply-accumulate (MAC) unit is also integrated to improve power efficiency and design flexibility. With an event-driven peripheral control and a real-time task-scheduling capability, this processing unit occupies 39.8 k gates. A 32-kb low-power SRAM is embedded to store instructions and the data. The RISC core includes peripherals, such as GPIOs and UART, for potential data interface. A JTAG interface provides debugging and memory-programming capabilities. OpenRISC 1200 is an open-source Verilog Intellectual Property, and appropriate adjustments can be made to the hardware for various applications. Therefore, OpenRISC 1200 is also ideal for a low-power low-voltage nose-on-a-chip.

During initialization, the boot loader (Fig. 4) loads the program from an external device (Flash/UART) to the internal memory (L7T SRAM). Once the program is loaded, the RISC-core accesses the program from the SRAM. In the e-nose microsystem, the RISC-core executes a complete program in order to control the entire system and communicates with the dCRBM unit. The data flow is shown in Fig. 12. The software in the system has two main functions: to control the overall system, and to process the received gas data.

The nose-on-a-chip has eight on-chip sensors for detecting gases to form a "fingerprint" of a specific gas. To acquire the

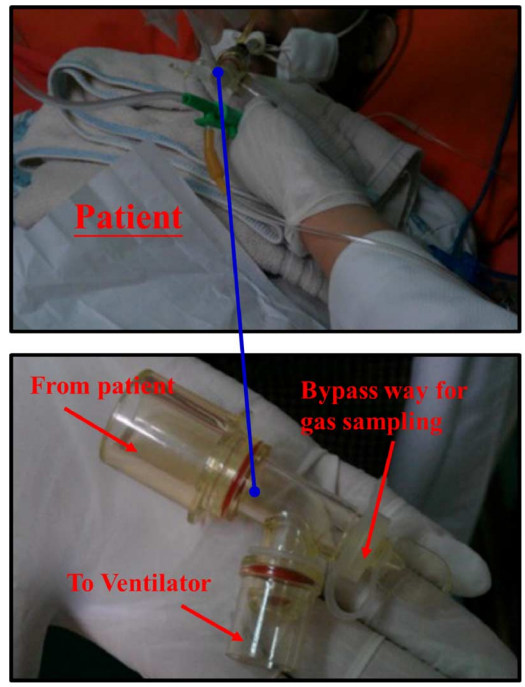


Fig. 13. Clinical experiment setup of the VAP patients at the proximal end of the expiratory device.

array responses of these eight sensors, an 8-to-1 multiplexer (CH-MUX) is used to select the on-chip sensors, according to the 3 bit control signal from the RISC-core. According to the signal processing requirement, the control signal speed is set at 100 kHz. The digitized sensor signals are sent to the RISC-core for preprocessing. When the testing gas flows in, the resistance of the sensor increases rapidly in the beginning and then saturates to a stable value. The received data is preprocessed by two steps. First, the RISC-core determines whether all the sensors reach steady state. After all the sensors reach saturation, the sensor resistance values are captured. Second, the array data undergo normalization to cancel the concentration effect with the gas fingerprint pattern.

The preprocessed data is then sent to dCRBM. There are two different phases of dCRBM: training phase and testing phase. In the training phase, the RISC-core transmits the preprocessed signal to the dCRBM system for training the parameters. In the testing phase, the RSIC-core transmits the preprocessed signal to the dCRBM system for data clustering and dimensional reduction. After the dCRBM testing phase, the data are returned to the RISC-core for odor recognition. Finally, the system controller exports the message to the LCD/UART/GPIO for display and/or communication.

V. Clinical Verification

Fig. 13 shows the clinical experiment setup with VAP patients approved by institutional review board (IRB) of Taipei Medical University, Taiwan. The sampled gas was obtained at the proximal end of the expiratory device by using a bypass approach. The sampled gas was collected through the tube. To ensure safety, the sampling time was restricted to 10 s. For a pilot test, the sensor raw data was obtained using a commercial electronic nose Cyranose, which has been applied in

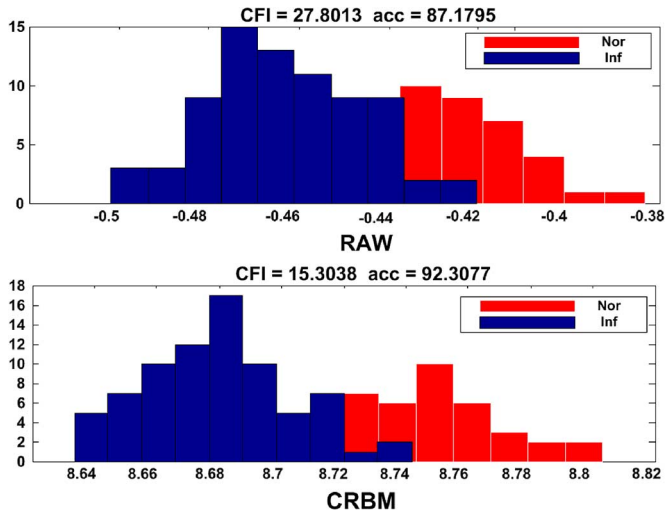


Fig. 14. Results of VAP identification with/without CRBM: normal and infected patients (Klebsiella, Pseudomonas aeruginosa, Staphylococcus aureus, Candida).

studies for disease identification [35]–[38]. The raw data acquired from the sensor array can be used as a standard in the proposed system. Breath samples from each patient were collected using a 1000 mL gas sampling bag before they were inserted into the device through a gas pumper at 10 mL/s. The readout data containing $\mathrm{R_S} - \mathrm{R_0}/\mathrm{R_0}$, as shown in (4), serves as the odor data for further analysis.

The functionality of VAP identification was verified through the clinical data. Among the clinical data, 76 samples infected with pneumonia (19 Klebsiella, 25 Pseudomonas aeruginosa, 16 Staphylococcus aureus, and 16 Candida) and 41 uninfected samples were categorized into the experimental group and control group, respectively. The classification was performed in two steps: 1) recognizing whether the patient was infected, and 2) if infected, identifying which microorganism was the source. The classification method was as follows: First, the CRBM was trained to model the raw data. Second, the linear discriminant analysis (LDA) was adopted to examine and visualize the linear separability of (i) the raw data and (ii) the projection of data to the hidden space of the trained CRBM. Finally, a linear classifier was used to compute the accuracy of the classifier.

Fig. 14 and Fig. 15 compare the LDA projections of the raw data and the corresponding hidden-neuron responses of the trained CRBM. Clustering Fisher index (CFI) [39] is applied to estimate the clustering performance. A larger CFI indicates that two clusters are more overlapped. Although the raw data of normal and infected patients (Klebsiella, Pseudomonas aeruginosa, Staphylococcus aureus, Candida) overlapped with each other, the CRBM improved the detection accuracy from 87.18% to 92.31% by reducing the CFI from 27.80 to 15.30 (Fig. 14). In the task of distinguishing Klebsiella from the other three types of infected patients (Pseudomonas aeruginosa, Staphylococcus aureus, Candida), the CRBM improved the accuracy from 94.74% to 100% by reducing the CFI from 6.71 to 2.89 [Fig. 15(a)]. In the task of distinguishing Pseudomonas aeruginosa from the other three types of infected patients (Klebsiella, Staphylococcus aureus, Candida), the CRBM improved the accuracy from 93.42% to 100% by reducing the CFI from 8.53 to 4.81 [Fig. 15(b)]. In the task of distinguishing Staphylococcus aureus from the other three types of infected patients (Klebsiella, Pseudomonas aeruginosa, Candida), the CRBM improved the accuracy from 92.11% to 100% by reducing the CFI from 9.92 to 5.43 [Fig. 15(c)]. Finally, in the task of distinguishing Candida from the other three types of infected patients (Klebsiella, Pseudomonas aeruginosa, Staphylococcus aureus), the CRBM improved the accuracy from 96.05% to 100% by reducing the CFI from 5.09 to 3.07 [Fig. 15(d)]. In this clinical verification, CRBM has shown powerful ability to identify the patents with VAP.

VI. Chip Measurement Results

The proposed nose-on-a-chip was fabricated in a TSMC 90 nm 1P9M CMOS technology. Fig. 16 shows the chip micrograph. The chip area is 3254 μm $\times$ 3223 μm. This chip has eight integrated on-chip sensors, an eight-channel adaptive sensor interface, a 10-bit SAR ADC, and a 32b RISC-core with a low-voltage L7T 8K $\times$ 32b SRAM, along with a robust dCRBM kernel for higher-dimensional signal processing. A summary of the chip and sub-blocks is provided in Table I.

In the on-chip sensor array, the resistance is controlled between several kΩ and several tens of kΩ. A sample sensor array response to ethanol was measured, as shown in Fig. 17(a). An eight-channel adaptive interface reads the sensor signals. The adaptive resistance and the preset adaptive voltage range between 5 kΩ–100 kΩ and between 0.15 V–0.25 V, respectively. The voltage-to-resistive change curve [Fig. 17(b)] shows a resistive change ratio $(\Delta\mathrm{R}/\mathrm{R})$ readout ranges between 0% and 76% with a regression coefficient (R^2) of 0.9993. This eight-channel adaptive interface consumes 215 μW from a 0.5 V supply voltage. The implemented CAS SAR-ADC achieves a constant resolution of 10 bit for a variable sampling rate (0.5 to 4 MS/s), at an adequately scaled supply (0.4 to 0.7 V). It occupies only a core area of 0.0418 mm^2, and consumes 1.15 μW at 0.5 V.

The measured read-waveform of PBV-L7T-SRAM, probed through the SRAM-Flash interface (SFIF), is shown in Fig. 18. At VDD $= 0.5$ V, this 256-row 256 Kb SRAM achieves a read access time of 20.8 ns, including the path delay caused by the SFIF, level-shifter, digital-IO-pad, and interconnect.

To verify the dCRBM, seven samples infected with pneumonia and 10 samples were categorized into the experimental group and the control group, respectively. The learning rate for $\{w_j\}$ is 0.25, and the learning rate for $\{a_i\}$ and $\{a_j\}$ are 0.5. After 5,000 learning cycles, the parameters can converge. One of the clustering results is shown in Fig. 19. Compared with the MATLAB simulation, the measurement result shows the dCRBM has a similar pattern distribution.

This nose-on-a-chip operates at 0.5 V, and consumes only 1.27 mW at an operating frequency of 8 MHz. This chip is the first demonstration of a fully integrated SoC for rapid diagnosis of VAP. Table II lists a comparison of the proposed nose-on-a-chip versus prior arts. This nose-on-a-chip achieves the highest level of integration and the highest computation capability with the lowest power dissipation among state-of-the-art nose-on-a-chip systems.

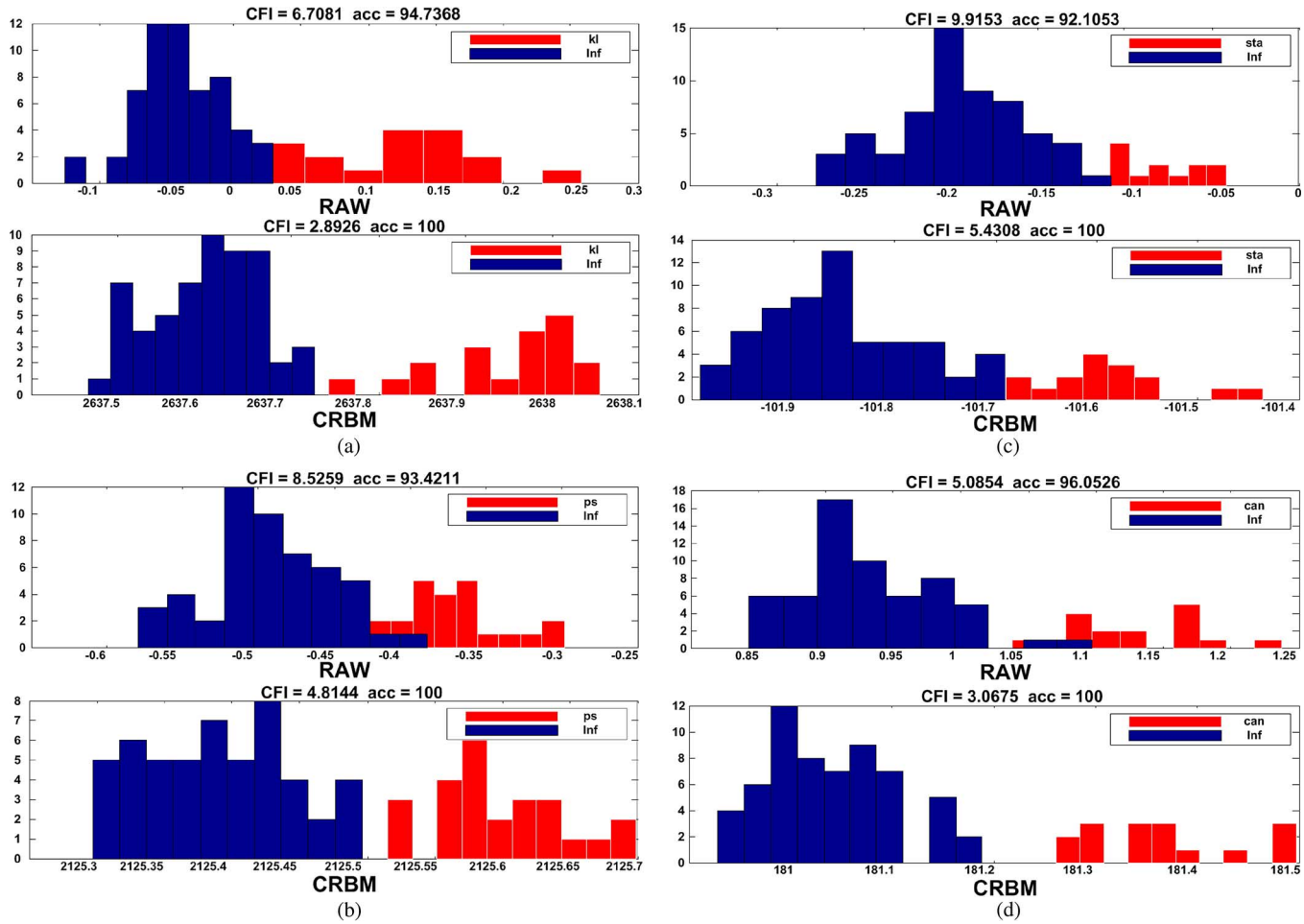


Fig. 15. Results of VAP identification with/without CRBM. (a) Klebsiella versus other infected patients (Pseudomonas aeruginosa, Staphylococcus aureus, Candida). (b) Pseudomonas aeruginosa versus other infected patients (Klebsiella, Staphylococcus aureus, Candida). (c) Staphylococcus aureus versus other infected patients (Klebsiella, Pseudomonas aeruginos, Candida). (d) Candida versus other infected patients (Klebsiella, Pseudomonas aeruginosa, Staphylococcus aureus).

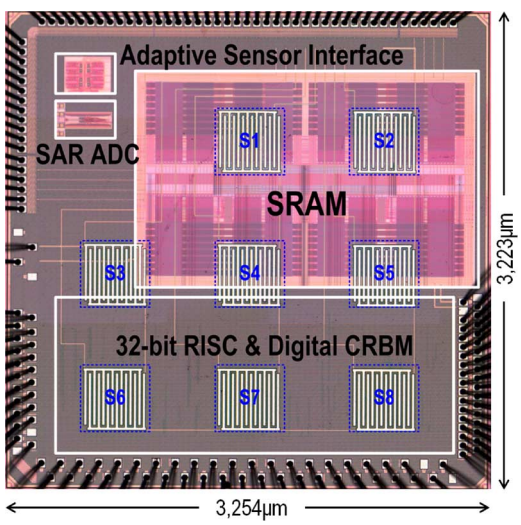


Fig. 16. Chip micrograph of the proposed nose-on-a-chip.

TABLE I
SUMMARY OF THE NOSE-ON-A-CHIP AND ITS SUB-BLOCKS

Chip Summary	
Technology	1P9M 90nm CMOS
Die Size	3,254μm × 3,223μm
Supply Voltage	0.5V
Power Dissipation	1.27mW
Operation Frequency	8MHz
Sub-Blocks	
On-Chip Sensors	8 Polymer-Carbon Composites
Adaptive Interface	8 Channels, Range: 5k-100kΩ
SAR-ADC	10b
Processor	32b RISC
SRAM	L7T, 8Kx32b
Learning Kernel	CRBM

VII. CONCLUSION

In this paper, a fully integrated nose-on-a-chip is proposed for VAP diagnosis. The chip occupies 10.49 mm^2 in 90 nm and

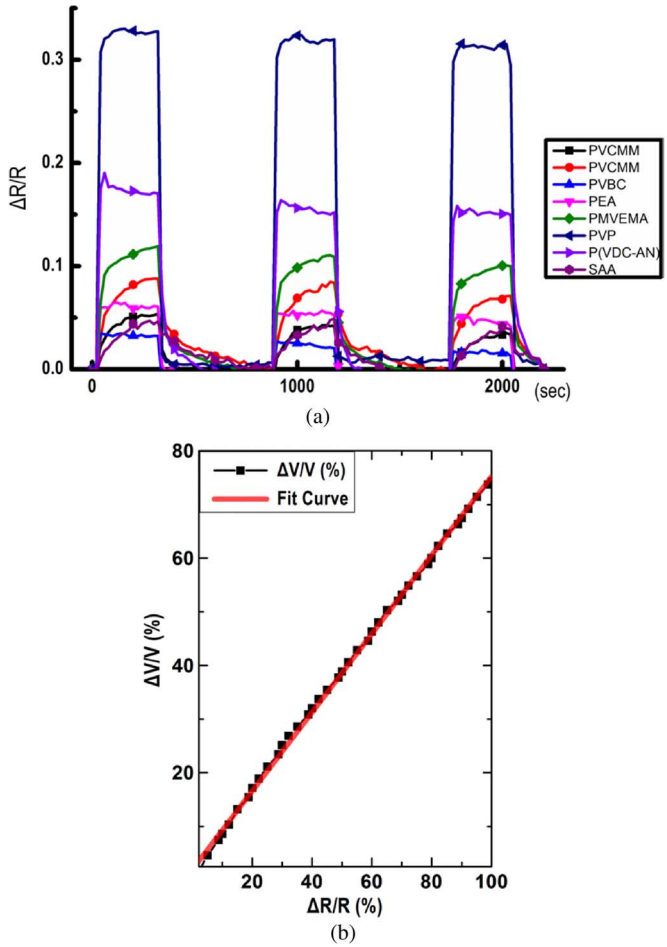


Fig. 17. (a) A sample gas response of the on-chip sensor array. (b) Vvoltage-to-resistive change curve of the interface circuit.

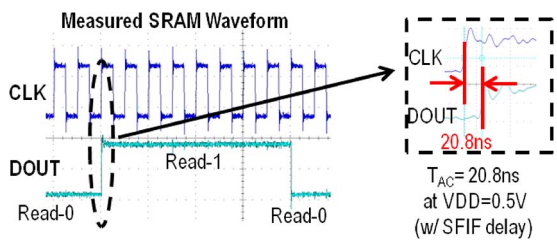


Fig. 18. The measured read-waveform of PBV-L7T-SRAM.

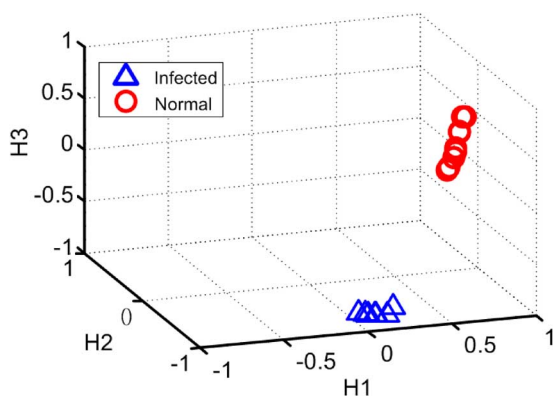


Fig. 19. Results of VAP identification with dCRBM.

TABLE II
COMPARISON TABLE WITH PRIOR ARTS

	JSSC'02 [40]	TBCAS'11 [41]	ISSCC'12 [42]	This Work
CMOS Technology	0.8μm	0.18μm	0.25μm	90nm
Supply Voltage (V)	>5	1.8	3.3	0.5
Sensor Type	Capacitive/Calorimetric/Mass-Sensitive	Resistive	Frequency	Resistive
Channels	3	8	1	8
Power Dissipation (mW)	>7.25	2.81	1.35	1.27
On-Chip Sensor	Post-MEMS	-	-	Standard CMOS
Sensor Interface	Not Adaptive	Self Adaptive	Not Adaptive	Self Adaptive
Embedded Processor	-	8b 8051	-	32b RISC
On-Chip Memory	-	6T, 16Kx8b	-	L7T, 8Kx32b
Learning Kernel	-	-	-	CRBM
Scalability	-	-	-	YES
Automatic Gain Control	NO	NO	YES	NO

consumes only 1.27 mW at a 0.5 V supply voltage. The functionality of VAP identification is verified by clinical data. The experimental results show a very high VAP identification rate of 92.31% for identifying healthy and infected patients and a 100% accuracy to identify the microorganisms of Klebsiella, Pseudomonas aeruginosa, Staphylococcus aureus, and Candida from VAP-infected patients. Consequently, this work provides a promising solution for a long-time unresolved issue—real-time monitoring and rapid diagnosis of VAP.

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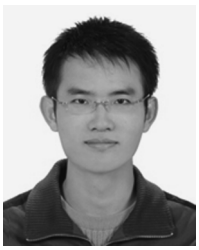

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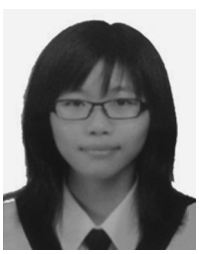

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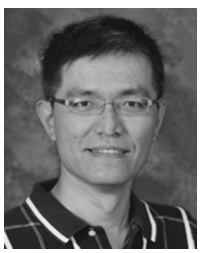
Li-Chun Wang received the B.S. degree from the Department of Chemistry, National Cheng Kung University, Tainan, Taiwan, the M.S. degree from the Department of Chemistry, National Sun Yat-sen University, Kaohsiung, Taiwan, and the Ph.D. degree from the Department of Materials and Engineering, National Chiao Tung University, Hsinchu, Taiwan.

Currently, he is with the Chemical System Research Division of the National Chung-Shan Institute of Science and Technology, Longtan Township, Taoyuan County, Taiwan. His main fields of research are the application of carbon nanomaterials and chemical sensors.

Hsin Chen (M'04) received the Ph.D. degree in electronics from Edinburgh University, Edinburgh, U.K., in 2004.

He joined the Electrical Engineering Department of National Tsing Hua University, Hsinchu, Taiwan, and was appointed as an Associate Professor. He has led the Neuro-Engineering Lab, looking to explore neuro-inspired computation and its hardware implememtation. The "neural hardware" includes stochastic neuromorphic systems that mimic biological neurons to compute with noise, neuro-electronic interfaces for neural prostheses and brain research, and neuro-engineered integrated circuits that could "communicate" with real biological neurons. The research findings in these areas have been applied to several clinical applications such as the eNose for smelling out pneumonia and the batteryless, implantable microsystem for studying the mechanisms of the deep-brain stimulation.

Dr. Chen received the Outstanding Young Researcher Award from the Taiwan Integrated Circuit Design (TICD) Society in 2013. He was an Invited Researcher at the University of Bordeaux, France, in 2009, Université d'Évry Val-d'Essonne, France, in 2011, and the Institute of Neuroinformatics, UZH/ETH, Switzerland, in 2014. He is a member of the IEEE EMB, the IEEE CaS, and TICD societies.



Chih-Cheng Hsieh (M'07) received the B.S., M.S., and Ph.D. degrees from the Institute of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, in 1990, 1991, and 1997, respectively.

He served with the Army of Taiwan as a Second Lieutenant from 1997–1999. From 1999–2007, he worked with a IC design house, Pixart Imaging Inc., Taiwan., and was involved in the development of CMOS image sensor ICs for PC, consumer, and mobile phone applications. He led the Mixed-Mode IC Department as a Senior Manager and helped the company become an IPO successfully in 2007. He has proposed many inventions to improve the function and quality of CMOS image sensor ICs, and has been granted 12 U.S. patents and 23 R.O.C. (Taiwan) patents. In 2007, he joined the Department of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan, where he is currently an Assistant Professor. His research interests include CMOS image sensor IC development for biomedical, space, robot, and customized applications; smart sensor IC with array level pre-processing; and low power analog and mixed-mode IC design.

Meng-Fan Chang (S'03–M'05) received the M.S. degree from The Pennsylvania State University, State College, PA, USA, and the Ph.D. degree from National Chiao Tung University, Hsinchu City, Taiwan, respectively.

In 2006, he joined the Department of Electrical Engineering at National Tsing Hua University (NTHU), Hsinchu, Taiwan. Currently, he is a Professor at NTHU. Before 2006, he worked in industry for more than 10 years. From 1996 to 1997, he designed memory compilers at Mentor Graphics, Warren, NJ, USA. From 1997 to 2001, he designed embedded SRAMs and Flash in the Design Service Division (DSD) at the Taiwan Semiconductor Manufacturing Company. From 2001–2006, he was a Director at the IPLib Company, where he developed embedded SRAM and ROM compilers, Flash macros, and flat-cell ROM products. His research interests include circuit designs for volatile and nonvolatile memory, ultra-low-voltage circuits, emerging memories, 3D-memory, memristor logics, and circuit designs for nano-devices.

Dr. Chang is the corresponding author of numerous ISSCC and VLSI Symposia papers. He received the Junior Research Investigators Award of Academia Sinica in 2012, Outstanding Industrial Collaboration Award of NTHU in 2012, and the Ta-You Wu Memorial Award of National Science Council (NSC-Taiwan) in 2011. He has also received numerous awards from the Taiwan National Chip Implementation Center (CIC), MXIC Golden Silicon Awards, and ITRI. He currently serves on the technical program committee for IEEE CAS (ISCAS), A-SSCC, VLSI-DAT, and numerous conferences. Since 2011, he has served as the Associate Executive Director for Taiwan's 5-year National Program of Intelligent Electronics (NPIE).

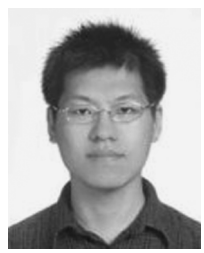
Yi-Wen Liu received the B.S. degree from National Taiwan University, Taipei City, Taiwan, and the M.S. and Ph.D. degrees from Stanford University, Stanford, CA, USA, in 1996, 2000, and 2006, respectively, all in electrical engineering.

From 2006–2010, he performed postdoctoral work at Boys Town National Research Hospital (BTNRH), Omaha, NE, USA. In 2010, he joined National Tsing Hua University, Hsinchu, Taiwan, where he is currently an Associate Professor. His research interests include signal processing and dynamic system modeling, with a focus on sounds and hearing.

Dr. Liu is a member of the Acoustical Society of America and the Association for Research in Otolaryngology.

Tsan-Jieh Chen (M'11) received the B.S. degree in electrical engineering from the Ming Chi University of Technology, New Taipei City, Taiwan, and the Ph.D. degree in communication engineering from National Chiao Tung University, Hsinchu City, Taiwan, in 2007 and 2012, respectively.

He was a Postdoctoral Research Fellow in 2012 and Assistant Research Fellow in 2013 at Biomedical Electronics Translational Research Center (BETRC), National Chiao Tung University. Currently, he is working on a bio-signal processing algorithm at MediaTek. His research interests include a bio-signal processing algorithm, hardware software co-design and optimization, and low-power design methodology for biomedical applications.



Chia-Hsiang Yang (S'07–M'10) received the B.S. and M.S. degrees from the National Taiwan University, Taipei City, Taiwan, and the Ph.D. degree from the University of California, Los Angeles (UCLA), Los Angeles, CA, USA, in 2002, 2004, and 2010, respectively, all in electrical engineering.

He then joined the faculty of the Electronics Engineering Department at the National Chiao Tung University, Hsinchu City Taiwan, as an Assistant Professor. His research interests focus on energy-efficient integrated circuits and architectures for biomedical and communication signal processing.

Dr. Yang was a winner of the DAC/ISSCC Student Design Contest in 2010. He received the 2010–2011 Distinguished Ph.D. Dissertation in Circuits & Embedded Systems Award from the Department of Electrical Engineering at UCLA. In 2013, he was a corecipient of the ISSCC Distinguished Technical Paper Award.

Herming Chiueh (M'90) received the B.S. degree in electrophysics from National Chiao Tung University (NCTU), Hsinchu, Taiwan, and the M.S. and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles, CA, USA.

From 1996 to 2002, he was with the Information Sciences Institute, University of Southern California, Marina del Rey, CA, USA. He has participated in the VLSI effort on several large projects at USC/ISI, which includes the development of a 55-million transistor processing-in-memory (PIM) chip. From 2009 to 2012, he gave more than 20 invited talks regarding his recent research on closed-loop epileptic seizure detection and low-power sigma-delta data converters at conferences and workshops as well as at various campuses and research institutes. He currently serves as an Associate Professor in the Department of Electrical and Computer Engineering at NCTU. His research interests include system-on-chip design methodology, low-power integrated circuits, neural interface circuits, and biomimetic systems.

Dr. Chiueh was the co-recipient of ISSCC 2013 Distinguished Technical Paper Award to recognize his research in "closed-loop neural-prosthetic SoC."

Jyuo-Min Shyu (S'85–M'88–SM'05–F'08) received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei City, Taiwan, and the Ph.D. degree in electrical engineering and computer science from the University of California, Berkeley, Berkeley, CA, USA, in 1977, 1979, and 1988, respectively.

In 1988, he joined the Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, and has been involved in various R&D and technology transfer projects for the development and advancement of microelectronics and flat-panel display industries in Taiwan. He was K. T. Li Chair Professor and Dean of the College of Electrical Engineering and Computer Science, National Tsing Hua University, Hsinchu, Taiwan (2007–2010), Executive Vice President of ITRI (2003–2007), Executive Director of Taiwan's National Nanotechnology Science and Technology Program (2004–2006), and is currently the President of ITRI. His research interests include microelectronic systems design and design automation for integrated circuits.

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From 2001–2006, he was a Senior Electrical Engineer with Second Sight Medical Products Inc., Sylmar, CA, USA. He designed mixed signal ASIC for retina prosthetic devices. In 2006, he joined the Electrical Engineering Faculty at National Tsing Hua University, Hsinchu, Taiwan, and is currently an Associate Professor. His research interests include biochemical sensing systems, analog and mixed signal IC design, neuromorphic SoC design, and biomedical SoC design.