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Electrical characteristic fluctuation of 16-nm-gate high-κ/metal gate bulk FinFET devices in the presence of random interface traps

Sheng-Chia Hsu[1,2] and Yiming Li[1,2,3*]

Abstract

In this work, we study the impact of random interface traps (RITs) at the interface of SiO_x/Si on the electrical characteristic of 16-nm-gate high-κ/metal gate (HKMG) bulk fin-type field effect transistor (FinFET) devices. Under the same threshold voltage, the effects of RIT position and number on the degradation of electrical characteristics are clarified with respect to different levels of RIT density of state (D_{it}). The variability of the off-state current (I_{off}) and drain-induced barrier lowering (DIBL) will be severely affected by RITs with high D_{it} varying from 5×10^{12} to 5×10^{13} eV^{-1} cm^{-2} owing to significant threshold voltage (V_{th}) fluctuation. The results of this study indicate that if the level of D_{it} is lower than 1×10^{12} eV^{-1} cm^{-2}, the normalized variability of the on-state current, I_{off}, V_{th}, DIBL, and subthreshold swing is within 5%.

Keywords: Density of interface traps; Random interface traps; Bulk FinFETs; Interface trap fluctuation; Electrical characteristic fluctuation; Statistical device simulation

Background

For the last decades, the technology of silicon-based CMOS devices suffered significant fabrication challenges and sizeable characteristic variability [1-5]. Characteristics could be affected by various traps in high-κ/metal gate (HKMG) devices [6]. For emerging ultra-scaled transistors, the characteristic degradation induced by interface traps at the interface of SiO_x/Si is severe for giga-scale circuit designs [7]. Furthermore, random interface traps (RITs) appearing at the interface of SiO_x/Si depend on different fabrication processes of HKMG [8-13]. Except planar MOSFETs, fin-type field effect transistors (FinFETs) with HKMG play a key role in sub-22-nm technology nodes to boost electrical performance [14-16] and suppress various fluctuations. Recent studies reported the density of interface traps (D_{it}) resulting from the orientations of the vertical fin channel of FinFETs [6,17]. The effects of RITs on sub-22-nm FinFETs have also been reported and compared between different device structures [18,19]. Unfortunately, the impact of RITs on 16-nm-gate HKMG bulk FinFET devices has not been clearly discussed yet.

In this work, we study the DC characteristic fluctuation induced by RITs at the SiO_x/Si interface of 16-nm TiN/HfSiON gate stack bulk FinFET devices by using experimentally calibrated three-dimensional (3D) device simulation. Under the same threshold voltage, more than 50% suppressions on the standard deviation of threshold voltage and subthreshold swing (SS) are achieved, benefiting from the nature of the vertical channel, compared with the planar MOSFET devices. By considering different levels of D_{it}, the effects of RIT position and number on the degradation of electrical characteristics are also examined. This paper is organized as follows: In the 'Methods' section, we illustrate the RIT simulation flow. In the 'Results and discussion' section, we report the results and discuss the characteristic fluctuation resulting from RITs on 16-nm-gate bulk FinFET devices. Finally, the conclusions are drawn.

Methods

RIT simulation method for FinFET devices

We study Si-based 16-nm-gate HKMG bulk FinFETs and planar MOSFET with amorphous-based titanium nitride/

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hafnium oxide/silicon oxide ($TiN/HfO_2/SiO_x$) stacks of gate dielectric and an effective oxide thickness (EOT) of around 0.95 nm (EOT = $T_o + T_h \times \varepsilon_{SiO2}/\varepsilon_{HfO2} = 0.6 + 2 \times 3.9/22 = 0.95$ nm), where T_o is the thickness of SiO_x, T_h is the thickness of HfO_2, and the dielectric constant of HfO_2 is assumed to be 22. An aspect ratio of 4 (i.e., $H_f/W_f = 32$ nm/8 nm = 4), a 30-nm-long source/drain (S/D), and an 8-nm-long S/D extension for the explored FinFET are considered, as shown in Figure 1 (a). The doping applied to the channel (N_{ch}), source/drain ($N_{S/D}$), substrate (N_B), and source/drain extension regions is 4×10^{18} cm^{-3}, 5×10^{20} cm^{-3}, 10^{15} cm^{-3}, and 6×10^{18} cm^{-3} for the n-type 16-nm-gate HKMG bulk FinFET devices, respectively. First, we calibrate the nominal DC characteristic of the studied devices according to the International Technology Roadmap for Semiconductor (ITRS) roadmap for low-power applications, which was experimentally quantified in our recent study, and fix the threshold voltage at 300 mV. To estimate device characteristics, a set of 3D drift-diffusion equations coupled with the density gradient equation for quantum correction is performed [20-23]. The mobility model used in the 3D device simulation involves fin channel surface roughness, high-field saturation, and impurity scattering. The mobility model was quantified with our device measurements for the best accuracy, and the characteristic fluctuation was validated with the experimentally measured DC baseband data from 15/20-nm CMOS and FinFET devices in our earlier work [24].

To perform 3D device simulation with two-dimensional (2D) interface trap fluctuation (ITF) for each randomly

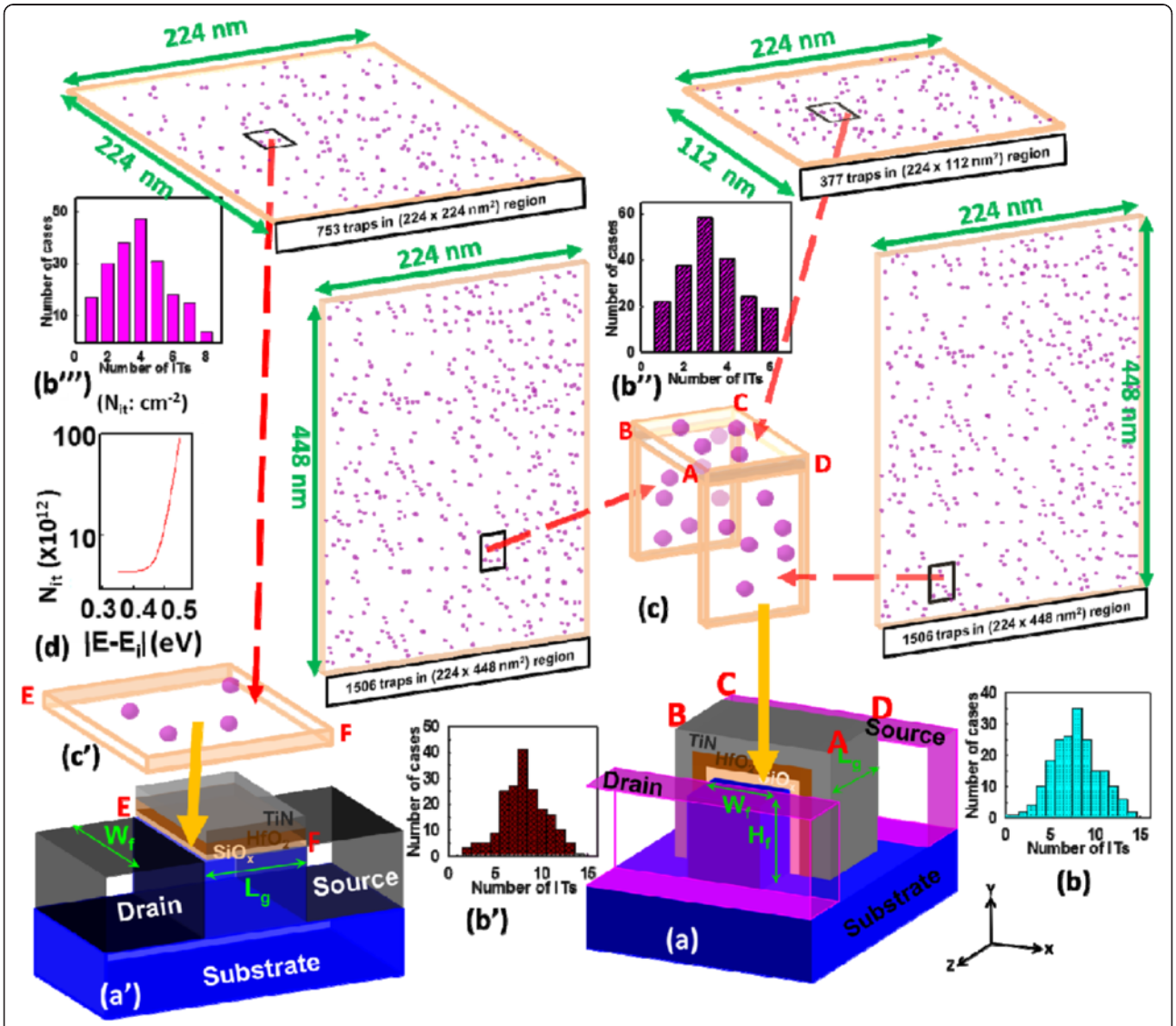

Figure 1 The RIT simulation technique for the bulk FinFET devices. (a) and (a') are the device structures. (b)-(b''') are the distribution of ITs. (c) and (c') illustrate the IT planes. (d) shows the individual trap's density versus the trap's energy.

generated device sample, we assume that the size of each RIT (S_{RIT}) is equal to 2 nm × 2 nm at the interface of SiO_x/Si. Notably, the value of S_{RIT} is numerically set for the simulation of ITF [2,25]. To generate RITs for the statistical device simulation of ITF, we first generate 3,389 acceptor-like traps marked as pink color in the three large 2D planes for the n-type FinFET device, as shown in Figure 1, and the corresponding concentration of RITs is around 1.5×10^{12} cm^{-2} [26,27]. The total number of generated acceptor-like traps follows the Poisson distribution, as shown in Figure 1 (b)-(b"). Then, we partition the large planes into many subplanes and map them to form a surface of RITs, as shown in Figure 1(c), where the number of traps in the subplanes varies from 0 to 6 at the top side and from 0 to 14 at the lateral sides, and the average number of interface traps is 3, 8, and 8, respectively. The concentration of each RIT (N_{it}) on a subplane is randomly assigned according to the RIT's energy following the relationship, as shown in Figure 1 (d). Then, the level of D_{it} is the total product of ($N_{it} \times S_{RIT}$) divided by the total area of the SiO_x/Si interface. Ultimately, we repeat this process until all subplanes are assigned. Notably, each subplane with RITs is numerically solved with the quantum mechanically corrected device model, where the RITs appear at the right-hand side of the Poisson equation.

Notably, the D_{it} varies with respect to the different process treatments on the TiN/HfSiON gate stacks [9,11,13], so we also consider the impact of three different D_{it} levels on device performance degradation. The ranges of high, typical, and low D_{it} vary from 5×10^{12} to 5×10^{13} eV^{-1} cm^{-2}, 1×10^{12} to 1×10^{13} eV^{-1} cm^{-2}, and 5×10^{11} to 5×10^{12} eV^{-1} cm^{-2}, respectively. For the p-type devices, we have a similar simulation setting with modification of the acceptor-like traps to donor-like traps. For the planar MOSFET ITF simulation, it follows

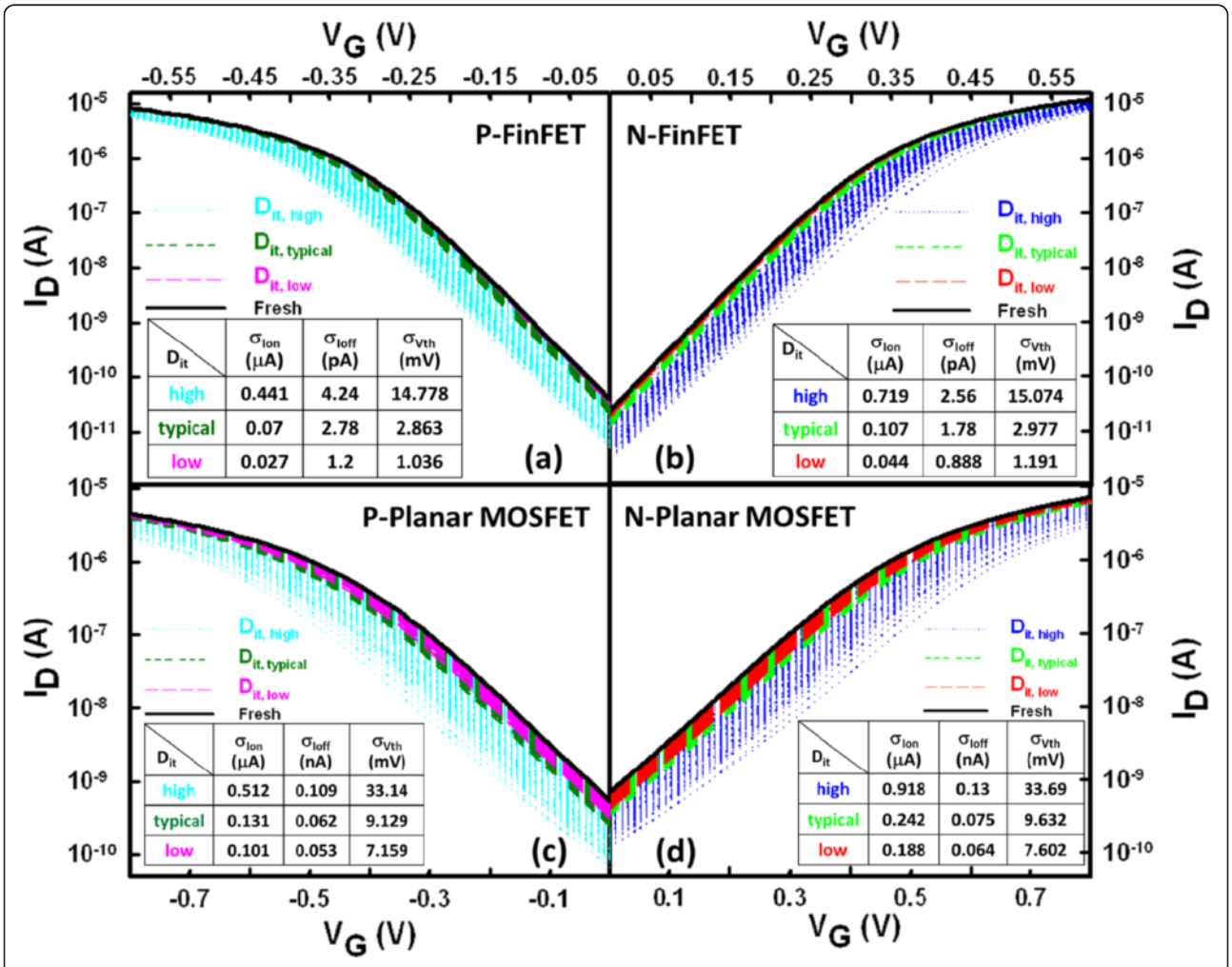

Figure 2 I_D-V_G curves of the studied devices with different D_{it} levels. The line indicates the I_D-V_G of a fresh sample. **(a, b)** n-/p-type bulk FinFET and **(c, d)** n-/p-type planar MOSFET devices.

our recent work, as shown in Figure 1 (a'), (b'''), and (c'), and the details could be found in [7,28].

Results and discussion

The nominal V_{th} for the fresh device (i.e., device with ultra-low D_{it}) is calibrated to 300 mV using a constant-current method. To meet the ITRS roadmap for low-power applications, the voltages applied for the 16-nm-gate HKMG bulk FinFET and planar MOSFET devices were 0.6 and 0.8 V, respectively. As shown in Figure 2, we firstly simulate the RIT-fluctuated I_D-V_G curves for the n-/p-type bulk FinFET (Figure 2a,b) and n-/p-type planar MOSFET (Figure 2c,d) devices with different levels of D_{it}, respectively. For all devices, the magnitude of ITF becomes smaller as the level of D_{it} decreases. The inset tables list the estimated fluctuation of I_{on} (σI_{on}), I_{off} (σI_{off}), and V_{th} (σV_{th}) for devices with different levels of D_{it}. As shown in Figure 3, we compare the ITs-fluctuated V_{th} under different levels of D_{it}, where the normalized standard deviation (σ/μ) of V_{th} is calculated, and σ and μ are the standard deviation and average of the fluctuated cases, respectively. The V_{th} shifts and its normalized standard deviation becomes larger when the level of D_{it} is increased. Both the n- and p-type FinFET devices, as shown in Figure 3a,c, have comparable magnitudes of σ/μ which are smaller than that of the planar MOSFET devices (about 50% reduction), as shown in Figure 3b,d. Nevertheless, the ITs-fluctuated V_{th} is strongly governed by high D_{it} varying from 5×10^{12} to 5×10^{13} eV^{-1} cm^{-2}. In Figure 4, we show the I_{on} versus I_{off} for all devices with different levels of D_{it}. The results of the normalized standard deviation of I_{on} and I_{off} imply that the advantage of the vertical channel in the suppression of ITF will be weakened when the level of D_{it} is increased; for example, the ellipsoid-shape distribution of I_{on} and I_{off} is broadened as the D_{it} increases. For the cases of low D_{it}, as shown in Figure 4a,c, the FinFET σ/μ of I_{on} and I_{off} is about three times smaller than that of

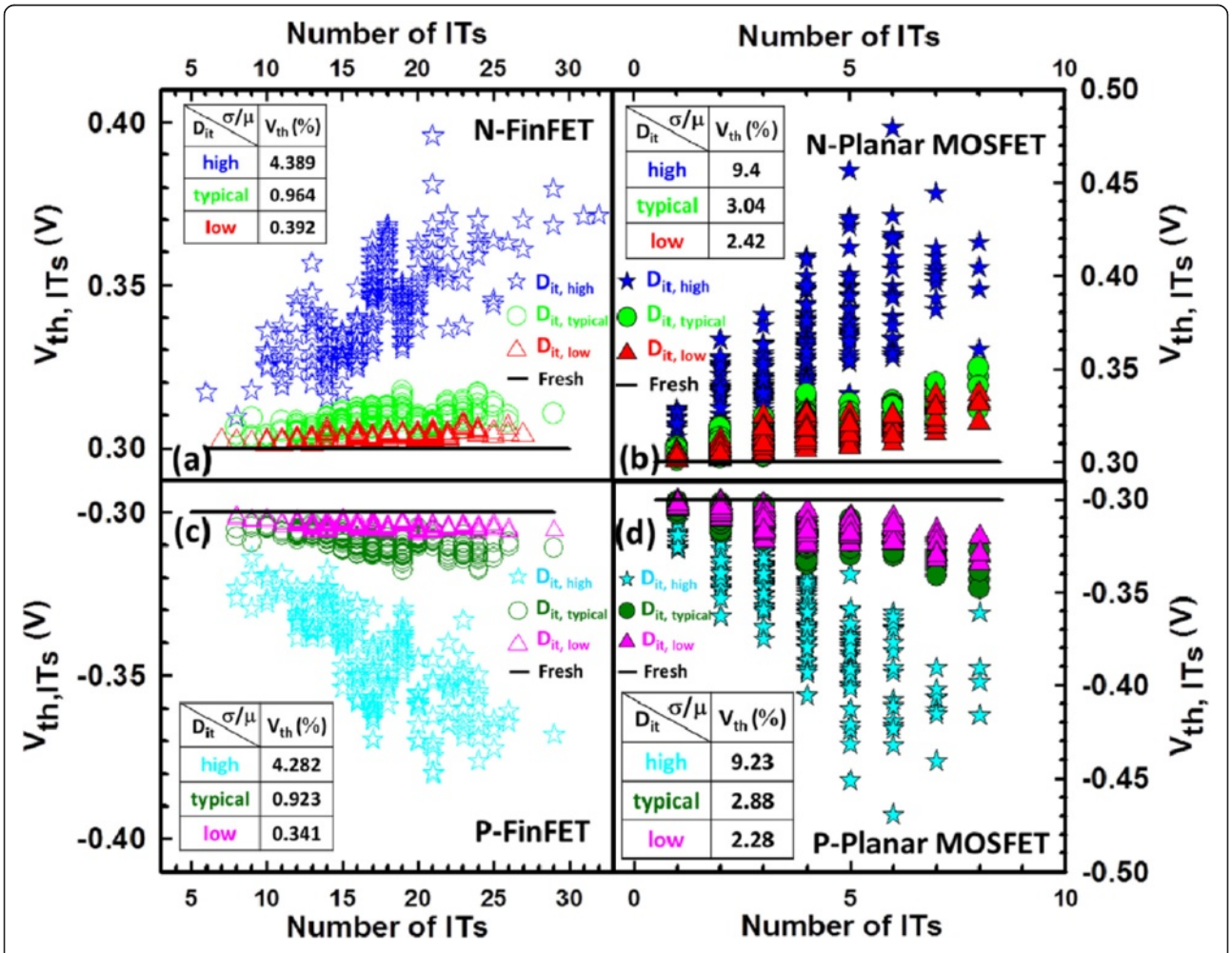

Figure 3 Fluctuated V_{th} for the studied devices with different D_{it} levels. The line indicates the threshold voltage of a fresh sample. **(a, c)** n-/p-type bulk FinFET and **(b, d)** n-/p-type planar MOSFET devices.

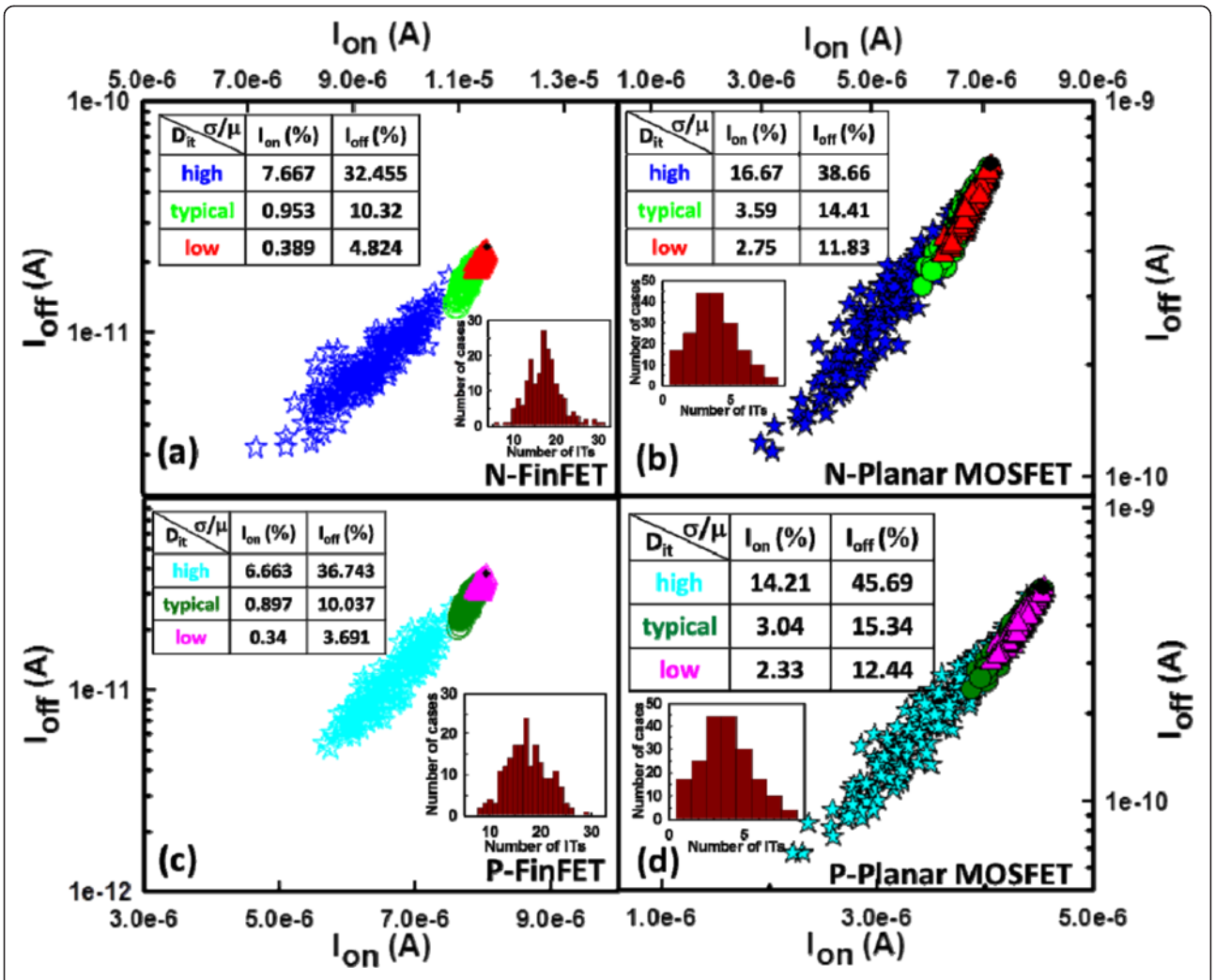

Figure 4 I_{off} versus I_{on} for the studied devices with different D_{it} levels. The black dot is the result of a free device. **(a, c)** n-/p-type bulk FinFET and **(b, d)** n-/p-type planar MOSFET devices.

the planar device, owing to their significant structural dominance. However, such strength is destroyed with the increasing level of D_{it}; as listed in the inset tables, the normalized standard deviations are considerable and comparable between the two devices for the cases of high D_{it}, in particular, the σ/μ of I_{off}.

The degradation of SS becomes more critical when the level of D_{it} increases. Owing to large gate capacitance (C_g) coupling in FinFETs, the dependence relationship of ITs-fluctuated SS versus drain-induced barrier lowering (DIBL) is reduced, as shown in Figure 5a,c; however, the distribution of SS versus DIBL exhibits a negative dependency in the planar MOSFETs, as shown in Figure 5b,d. The significant dependence relationship of ITs-fluctuated SS versus DIBL indicates that the characteristic degradation was caused by an even stronger short-channel effect [29]. To maximize V_{DD} scaling for logical application, the fluctuations of transconductance (g_m) and subthreshold swing must be minimized. As shown in Figure 6, the ITs-fluctuated transconductances are calculated for the studied devices with different levels of D_{it}. The flatter normalized standard deviations (within 2%) of the maximum transconductance ($g_{m,max}$) listed in the inset tables are found for the FinFET devices with high D_{it}, as shown in Figure 6a,c.

To go deep into the physics of the results reported above, as shown in Figure 7, we now examine the advantage of the vertical structure and the effect of random distribution (i.e., the random position) and the random number of ITs on the surface potential profiles of the ITs-fluctuated devices. As shown in the inset of Figure 7a, along the channel direction (Z-direction) from the source (S) to the drain (D) at the interface of SiO_x/Si on the top gate, the two profiles of conduction band are extracted

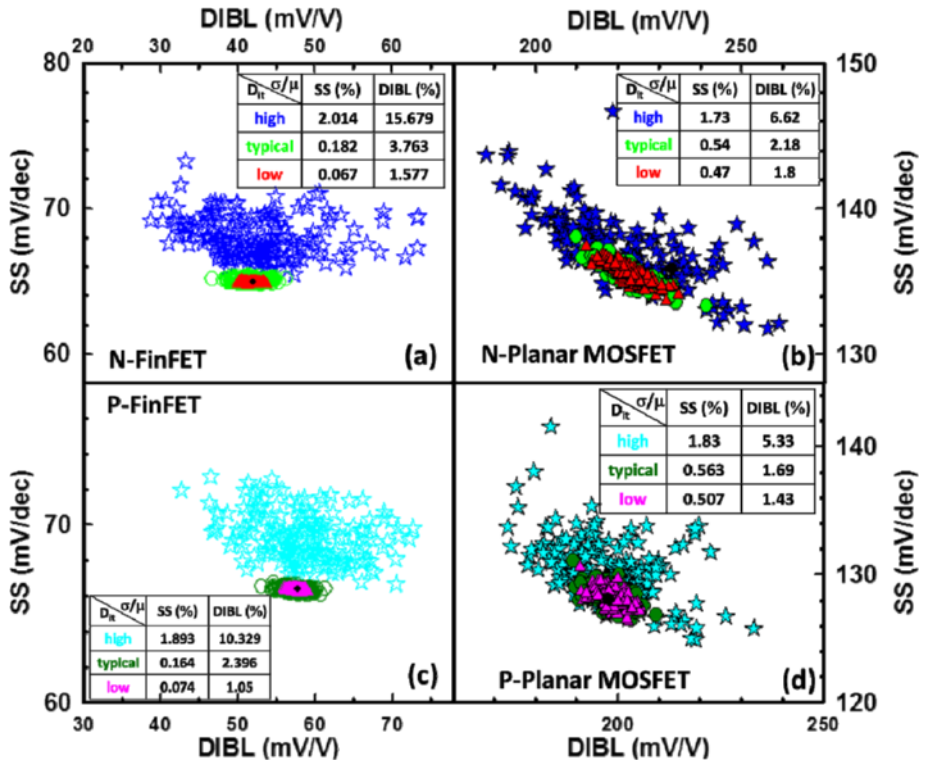

Figure 5 SS versus DIBL for the studied devices with different D_{it} levels. (a, c) n-/p-type bulk FinFET and **(b, d)** n-/p-type planar MOSFET devices.

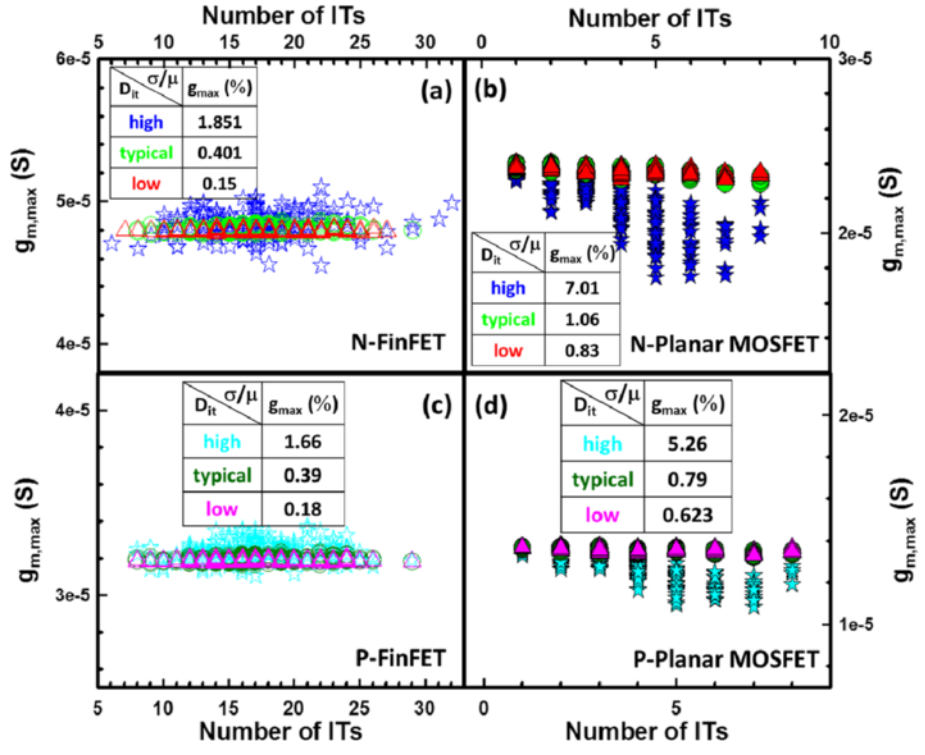

Figure 6 ITs-fluctuated $g_{m,\ max}$ for the studied devices with different D_{it} levels. (a, c) n-/p-type bulk FinFET and **(b, d)** n-/p-type planar MOSFET devices.

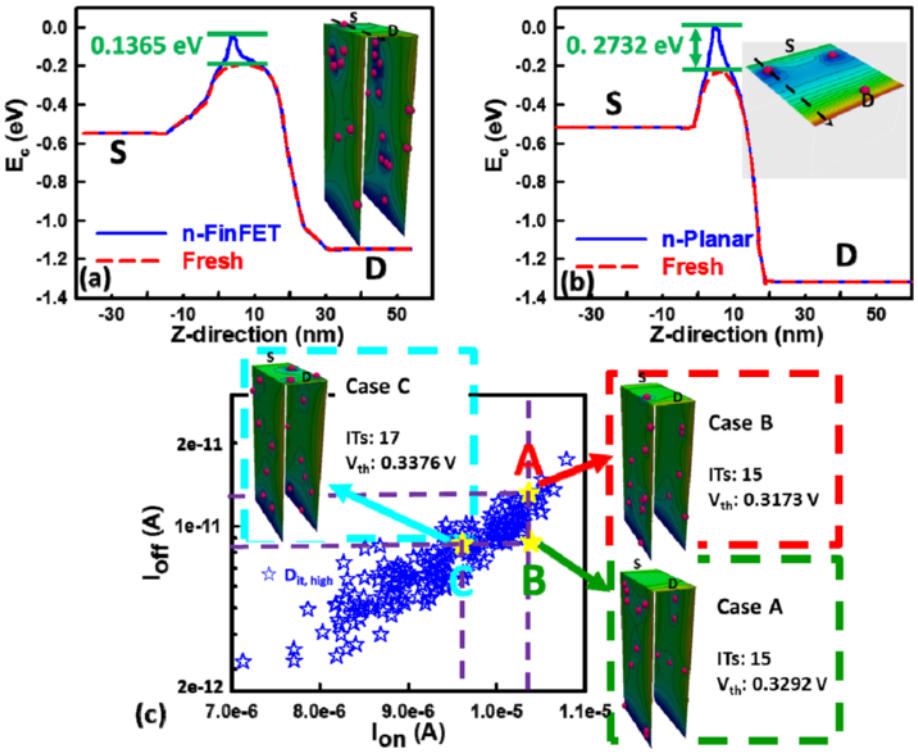

Figure 7 Barrier height fluctuation induced by RITs for the studied devices with high D_{it}. n-type HKMG **(a)** bulk FinFET and **(b)** planar MOSFET devices. The devices are under off-state condition, where $V_G = V_s = V_B = 0$ V and $V_D = 0.6$ V for the FinFET and $V_G = V_s = V_B = 0$ V and $V_D = 0.8$ V for the planar MOSFET. **(c)** The I_{off}-I_{on} plot used to explain the position and number effects of RITs.

and compared for the fresh FinFET device and the FinFET device with high D_{it} under off-state condition, where the barrier difference induced by a single interface trap is about 0.1365 eV. Similarly, as shown in Figure 7b, for the planar MOSFET device, the barrier difference is about 0.2732 eV. Comparison between Figure 7a and 7b indicates the significant structural effect; the planar MOSFET device severely suffers from the impact of RIT compared to the FinFET one. The coupling of gate electrodes from both the lateral sides to the top gate enhances the C_g, and thus, it effectively reduces the impact of RITs on the energy band. The findings of this comparison confirm the superiority of a 3D channel structure and the aforementioned results. The random position effect of RITs is further examined for the FinFET device. For similar I_{on} and different I_{off}, the two illustration cases (case A and case B) shown in Figure 7c have the same number of ITs (15 ITs) but different V_{th} owing to the different positions of RITs. For similar I_{off} and different I_{on}, the numbers of ITs for the two illustration cases (case A and case C) shown Figure 7c are 15 and 17. Therefore, according to the random number effect, they have different V_{th} because the effective D_{it} of case C is higher than that of case A. Thus, the device has similar I_{off} and different I_{on}.

Conclusions

In this work, we have investigated the impact of RITs on n-/p-type 16-nm-gate HKMG bulk FinFETs using an experimentally validated device simulation technique. We examined the ITs-fluctuated short-channel effect (SCE) parameters for the bulk FinFET and planar MOSFET devices. Benefiting from the improved gate controllability and stronger gate coupling capability, the estimated normalized standard deviation indicates that the 16-nm-gate HKMG bulk FinFET devices can effectively suppress the DC characteristic and SCE parameter fluctuations induced by RITs with respect to different levels of D_{it}. The insets of Figures 3, 4, 5, 6 listed the fluctuation magnitudes of I_{off} and DIBL which are severely governed by RITs with high D_{it} level ranging from 5×10^{12} to 5×10^{13} eV^{-1} cm^{-2}. Due to the strong screening effect for devices under high gate bias, the fluctuation magnitudes of SS and g_m induced by different levels of RITs are minimized. To effectively control the magnitude of normalized fluctuation within 5% for the V_{th}, I_{off}, I_{on}, SS, and DIBL, the D_{it} should be lower than 1×10^{12} eV^{-1} cm^{-2}. We are currently designing a proper experiment to measure the characteristic fluctuation induced by RITs and study the random bulk traps' influence together with RITs on device characteristic variability.

Abbreviations

σI_{off}: Standard deviation of I_{off}; σI_{on}: Standard deviation of I_{on}; σV_{th}: Standard deviation of V_{th}; 2D: Two-dimensional; 3D: Three-dimensional; C_g: Gate capacitance; DIBL: Drain-induced barrier lowering; D_{it}: Density of interface traps; EOT: Effective oxide thickness; FinFET: Fin-type field effect transistor; g_m: Transconductance; $g_{m,max}$: Maximum transconductance; HKMG: High-κ/metal gate; ITs: Interface traps; I_{off}: Off-state current; I_{on}: On-state current; N_{ch}: Channel doping; N_B: Substrate doping; N_{it}: RIT concentration; $N_{S/D}$: Source/drain doping; RITs: Random interface traps; SCE: Short-channel effect; S_{RIT}: RIT size; SS: Subthreshold swing; V_{th}: Threshold voltage.

Competing interests

The authors declare that they have no competing interests.

Authors' contributions

S-CH performed the numerical simulation and data analysis. YL conducted the entire study including manuscript preparation. Both authors read and approved the final manuscript.

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