An Efficient Method for Characterizing Time-Evolutional Interface State and Its Correlation with the Device Degradation in LDD n-MOSFET's

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***Abstract*—A new characterization method is proposed to study the relationship between the hot-carrier-induced interface state $N_{it}(x)$ and the device drain current degradation of submicron LDD n-MOSFET's. In this method, by making use of the conventional charge pumping measurement in combination with the power-law dependence of interface damages on stress time, the spatial distribution $N_{it}(x)$ and the effective damaged length L_{dam} can be easily extracted. The time evolution of the interface state generation and its correlation with the device degradation can then be well explained. It is worthwhile to note that this newly-developed method requires no repetitive charge pumping measurements, and hence avoids he likely imposition of re-stress on tested devices. By combining the characterized L_{dam} and N_{it} quantitatively, the results show that the damage at $V_{GS} \approx V_{DS}/2$ is most highly localized among various stress biases, which can explain why the generated interface states will dominate the device drain current degradation at this bias after long-term operating conditions.**

NOMENCLATURE

C	Proportional constant in the power-law model.
$E_{1/2}$	Lateral surface electric field at the position where the amount of induced interface states is $\Delta N_{it,1/2}$ (V/cm).
E_{lat}	Lateral surface electric field distribution (V/cm).
E_m	Maximum lateral surface electric field (V/cm).
f	Frequency of the applied gate pulse (Hz).
I_{cp}	Charge pumping current (A).
$I_{cp,max}$	The maximum charge pumping current after stress (A).
I_{DS}	Drain current (A).
L_{dam}	Effective damaged length of the induced interface state in terms of FWHM (cm).
$n(t)$	Time-dependent power-law factor.
q	Magnitude of electronic charge (C).
t	Stress time (sec).
$V_{fb}(x)$	Local flatband voltage distribution (V).
V_{gh}	High level of applied gate pulse string in charge pumping measurement (V).
V_{gl}	Base level of applied gate pulse string in charge pumping measurement (V).
V_{rev}	Reverse bias applied to source and drain electrodes in charge pumping measurement (V).
V_{DS}	Applied drain-source bias (V).
V_{GS}	Applied gate bias (V).
$V_T(x)$	Local threshold voltage distribution (V).
W	Effective channel width (cm).
λ_e, λ_h	Mean-free path for electron (hole) (Å).
$\phi_{it,e}, \phi_{it,h}$	Critical energy that an electron (hole) must have to create interface states (eV).
$\Delta I_{cp,max}$	Increase in the maximum charge pumping current after the stress (A).
$\Delta N_{it,1/2}$	Half of the maximum interface state density (1/cm^2).
ΔN_{it}	Interface state density (1/cm^2).
$\Delta N_{it,m}$	Maximum interface state density (1/cm^2).

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I. INTRODUCTION

ONE of the key reliability issues imposed by the continued shrinking of MOSFET dimensions is the hot-carrier-induced oxide damages which result in the device degradations such as the threshold voltage shift, transconductance reduction, drain current degradation, etc. These damages are due to the generation of both trapped charges Q_{ox} in the oxide and interface states (N_{it}) at the Si-SiO_2 interface [1]–[3]. Moreover, since the probabilities for the injection and creation depend sharply upon the hot-carrier energy, provided by the high accelerating electric field to overcome the critical barrier, the majority of the oxide traps and interface states are highly localized near the drain junction. This highly localized character of the hot-carrier injection and the resultant damage present a considerable challenge to both experimental and modeling efforts.

One widely used experimental method for quantitatively characterizing oxide damages in MOSFET's is the so-called charge-pumping (CP) technique [4], [5], which can be employed to investigate the interface properties in MOS devices. In particular, this technique is capable of providing the information of interface traps generated during the injection and the charges that have been trapped in the gate dielectric, even for the case of localized injection.

In spite of its excellent characterizing capability, the charge pumping technique has not yet been satisfactorily combined with an efficient method to quantitatively establish the relationship between the characterized oxide damages and the

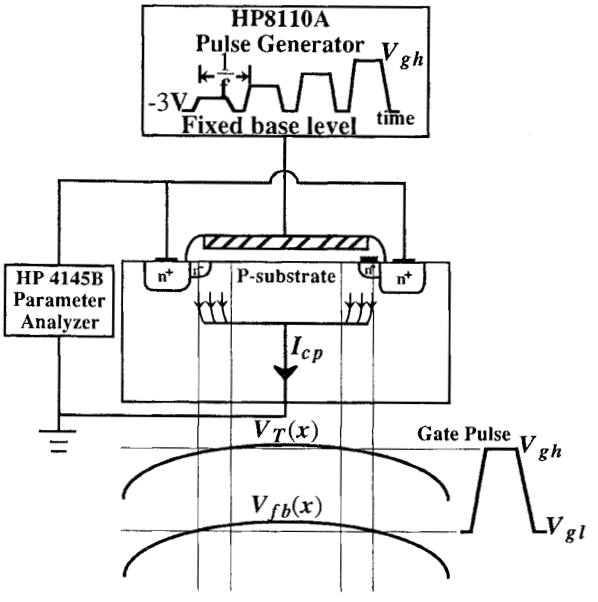

Fig. 1. Basic experimental set-up for charge pumping measurement.

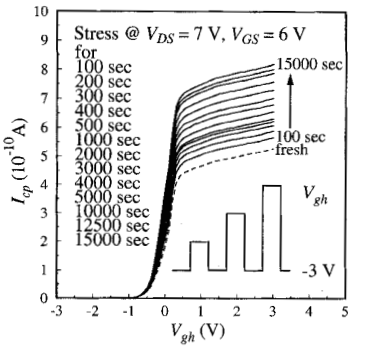

Fig. 2. Measured $I_{\rm cp}$ versus $V_{\rm gh}$ curves before and after various time stress. The applied gate frequency is 1 MHz.

aforementioned device degradation effect. In the past, most of the studies are concentrated on the individual study of $N_{\rm it}$ characterization [2]–[4] and its correlation with the degradations [5] qualitatively. Only a few [6] are focused on the correlation between $N_{\rm it}$, damaged region, $L_{\rm dam}$ and drain current degradation.

In this paper, we will develop a new characterization method to extract the spatial distribution of interface states using charge pumping measurement and the time-dependent power law relationship. Unlike other existing methods by adjusting the reversed drain bias $V_{\rm rev}$, this method can directly profile the highly localized interface states as well as the effective time-dependent damaged length. For demonstration, this paper begins with the implementing details of this technique, along with some illustrative results. Next, this newly-developed method is applied to LDD n-MOSFET's stressed at different biases so as to further investigate the device drain current degradation under long-term operating conditions.

II. Device Fabrication and Charge-Pumping Measurement

The LDD n-MOSFET's used in this work were fabricated using a poly-Si gate twin-well CMOS process. The tested samples were 0.72-μm mask gate length (metallurgical junction was 0.044-μm offset from gate edge), 20-μm channel width LDD transistors, 140-Å oxide thickness, and 0.15-μm conventional vapor-deposited sidewall oxide spacer. The channel was implanted with boron and followed by a diffusion process to adjust the channel to a surface concentration $N_A = 1.5 \times 10^{17}$ cm^{-3}. After the conventional gate etching process, implantation with phosphorus dosage of 2×10^{13} cm^{-2} and energy 80 keV was performed in n^- regions. Then, source and drain were arsenic-implanted with a junction depth of 0.22 μm. The required source/drain and channel doping profiles for device simulations were generated using process simulator—SUPREM IV [7]. They were calibrated against SRP or SIMS data. In this work, we use PISCES IIB device simulator to simulate the majority-carrier distribution to define the effective channel length [8] that contributes to the measured charge-pumping currents.

The basic setup for charge pumping measurement is shown schematically in Fig. 1. We use a fixed base level CP measurement, i.e., the gate of an LDD n-MOS device under test is connected to a pulse generator (HP8110A), and the source/drain are grounded, while the substrate current is measured. Note that the drain and source biases are held constant at zero to avoid the stress on devices during the measurement. A series of 1-MHz square pulse strings with rising/falling gradient of 25 ns/V are used in our CP measurements. By fixing the base level $V_{\rm gl}$ at -3 V, we vary high level voltage $V_{\rm gh}$ to measure CP currents for fresh and stressed LDD n-MOSFET's. Fig. 2 shows the measured $I_{\rm cp}$ versus $V_{\rm gh}$ curves with both source and drain grounded before and after various periods of channel-hot-carrier stress at $V_{\rm DS}$ =7 V and $V_{\rm GS}$ =6 V for the tested sample. The dashed curve is the measured charge pumping current for a fresh device while the other solid curves are those for the device after different time stress. We can see that the CP currents rise abruptly when the applied high level gate voltages are larger than the local threshold voltage $V_T(x)$ [4], [9]–[11], as shown in Fig. 1. With the increasing stress time, more interface states are generated and so are the CP currents. From this set of experimental data, we may further find a way to investigate the oxide damages associated with this hot-carrier-induced stress as described below.

III. A New Method to Determine the Interface State and the Damaged Region

Although the charge pumping technique can be served as a good tool for characterizing the amount of interface states, it still has to be equipped with an appropriate method to enhance the characterizing capability. For this reason, here we will propose a new method to characterize the interface state distribution by combining the power-law model and the charge pumping measurement data. A general power-law formula for describing the time-dependent interface damages can be

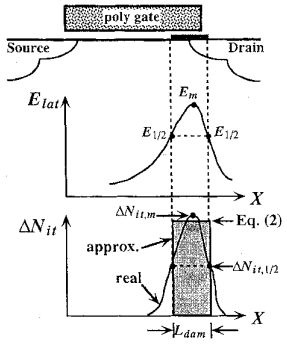

Fig. 3. Schematic diagram of the new characterization technique. The oxide damaged region along with the lateral surface electric field, is also shown.

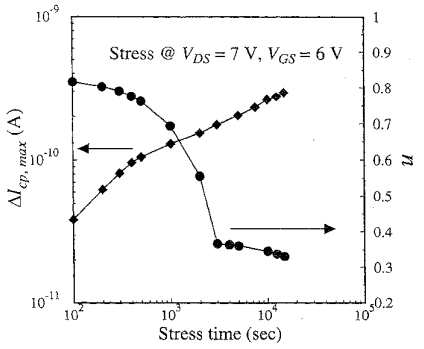

Fig. 4. $\Delta I_{\mathrm{cp,max}}$ versus stress time from Fig. 2. The time-dependent power law factor n is shown on the right.

expressed as [12]

$$\Delta I_{\mathrm{cp,max}}(t) = C\left[t\frac{I_{\mathrm{DS}}}{W}e^{-\phi_{\mathrm{it}}/q\lambda E_m}\right]^{n(t)}. \tag{1}$$

In this equation, $\Delta I_{\mathrm{cp,max}}$ is the increase of the maximum CP current (i.e., a signal of the overall increase of the interface state density). q is the electron charge. λ (λ_e and λ_h represent the mean-free paths for electrons and holes, respectively,) is the mean-free path of the hot carrier. E_m is the maximum lateral surface electric field. I_{DS} is the device drain current. W is the gate width. C is a proportional constant. The power-law factor $n(t)$ indicates the power-law dependence on the stress time t, and ϕ_{it} is a critical energy that a carrier must have in order to create interface traps. Let $\phi_{\mathrm{it},e}$ and $\phi_{\mathrm{it},h}$ be the critical energies for electrons and holes, respectively. Here, it should be noted that n has been modified to be a function of stress time (no longer assumed to be constant) and can be determined from experiment. Experimentally determined values for these parameters are $\phi_{\mathrm{it},e} = 3.7$ eV and $\phi_{\mathrm{it},h} = 4.2$ eV. Also, the values of the electron and hole mean-free paths are $\lambda_e = 67$ Å and $\lambda_h = 49$ Å [13], respectively.

As described by Ancona *et al.* [14], in MOS devices with very thin gate oxides, the hot-carrier-induced interface state generation occurs in a relatively narrow zone (i.e., highly localized) and the peak is found to be well correlated with the location, where the lateral electric field reaches its maximum value. With this in mind and for simplicity, this highly localized interface trap $\Delta N_{\mathrm{it}}(x)$ can be approximated by a rectangular distribution as shown in Fig. 3. Also, the approximate ΔN_{it} profile has the nonzero value

$$\Delta N_{\mathrm{it}}(t) = \frac{\Delta I_{\mathrm{cp,max}}(t)}{qWfL_{\mathrm{dam}}(t)} \tag{2}$$

only in the effective damaged region. In the above equation, f is the applied gate pulse frequency in CP measurement. The effective time-dependent damaged length $L_{\mathrm{dam}}(t)$ is defined as the full width at half-maximum (FWHM) of the ΔN_{it} profile and can be regarded as an important index of the damage during hot-carrier stress. Here, it should be emphasized that our definition of $L_{\mathrm{dam}}(t)$ and the derivation of $\Delta N_{\mathrm{it}}(x)$ are just based on the general feature of charge pumping method with an aim to reduce the repetitive CP measurements and complicated data manipulation as much as possible by making appropriate approximations.

Now, $L_{\mathrm{dam}}(t)$ for (2) can be derived as follows. First, keeping the definition of FWHM in mind and referring again to the power-law expression, we get

$$\frac{\Delta N_{\mathrm{it},1/2}(t)}{\Delta N_{\mathrm{it},m}(t)} = \exp\left[\frac{n(t)\phi_{\mathrm{it}}}{q\lambda}\left(-\frac{1}{E_{1/2}(t)}+\frac{1}{E_m}\right)\right] = \frac{1}{2}. \tag{3}$$

Here, $\Delta N_{\mathrm{it},1/2}$ is defined as one half of the maximum interface state generation $\Delta N_{\mathrm{it},m}$ in tested device, and $E_{1/2}$ is the lateral surface electric field at a location, where the induced amount of interface states is $\Delta N_{\mathrm{it},1/2}$.

Next, we can rearrange (3) to solve $E_{1/2}$ which yields

$$E_{1/2}(t) = \left(\frac{1}{E_m}+\frac{q\lambda}{n(t)\phi_{\mathrm{it}}}\ln 2\right)^{-1}. \tag{4}$$

The lateral surface electric field under the stress condition was simulated with a 2-D device simulator PISCES IIB [15]. To make sure that the simulation results are more convincing, the calibration procedure should be performed beforehand. Thus, the $E_{1/2}$ positions can be easily located from the simulated lateral surface electric field. As a consequence, the effective damaged length L_{dam} of the ΔN_{it} profile can be obtained by calculating the distance between the two $E_{1/2}$ locations as illustrated in Fig. 3.

IV. Results and Discussions

In Fig. 4, we show the increase (denoted by $\Delta I_{\mathrm{cp,max}}$) of a sequence of the maxima in I_{cp} (from Fig. 2) with stress time (in diamonds), which are plotted as a function of the stress time in log-log scale. They can be regarded as the changes of the induced interface states for the stressed and fresh devices. Initially, $\Delta I_{\mathrm{cp,max}}$ increases largely with the increasing stress time and then *gradually saturates*. According to the power-law model, the power-law factor $n(t)$ can be extracted from the slope of the $\log(\Delta I_{\mathrm{cp,max}})$ versus $\log(t)$ curve by (1) as shown also in Fig. 4 with solid circles. It can be seen that n decreases largely with the increasing stress time, and then approaches to a saturated value, which is approximately 0.32 in this case. It has been reported that under the stress condition of the *maximum substrate current bias* ($V_{\mathrm{GS}} \approx V_{\mathrm{DS}}/2$), the value of n is stress-bias dependent and is about 0.5, as in

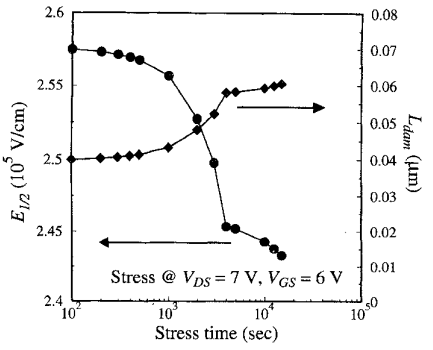

Fig. 5. $E_{1/2}$ and the effective damaged length $L_{\rm dam}$ versus time, in terms of FWHM.

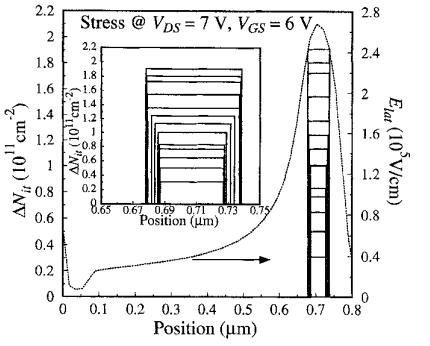

Fig. 6. Time evolution of lateral distributions of $\Delta N_{\rm it}(x)$ and the corresponding lateral surface electric field distribution at the stress condition.

[12]. However, *when the device is stressed at other biases*, n is less than 0.5 as concluded in this work.

Before determining the effective damaged length $L_{\rm dam}$, the corresponding lateral surface electric field distribution should be calculated first. Now, with this distribution being calculated by the 2-D device simulator, we can calculate $E_{1/2}$ (denoted in Fig. 3) straightforwardly from (4). The results are shown in Fig. 5. Values of $E_{1/2}$ decrease with the increasing stress time (i.e., with the decreasing power-law factor). Furthermore, with $E_{1/2}$ just obtained, we can find the two $E_{1/2}$ positions from the simulated lateral surface electric field distribution. Thus, The effective damaged length $L_{\rm dam}$ of the $\Delta N_{\rm it}$ profile with a full width at half-maximum (FWHM) can be obtained from the difference between the two $E_{1/2}$ locations. The results are again shown in Fig. 5.

Given $\Delta I_{\rm cp,max}$ and $L_{\rm dam}$, the induced $\Delta N_{\rm it}$ distribution can then be calculated from (2) as shown in Fig. 6. The simulated lateral surface electric field distribution $E_{\rm lat}$ is also shown here. The insert shows the magnified box approximation with the magnitude $\Delta N_{\rm it}$, damaged region and damaged length $L_{\rm dam}$ near gate edge. From this figure, we can see that both the magnitude and damaged range of $\Delta N_{\rm it}$ increase with stress time while the damaged length tends to saturate gradually with stress time. It should be noted that if we keep the power-law factor n constant as one usually assumes, the effective damaged length is a constant at around 400 Å in this case. This gives rise to a deviation of 200 Å by comparing with our calculations.

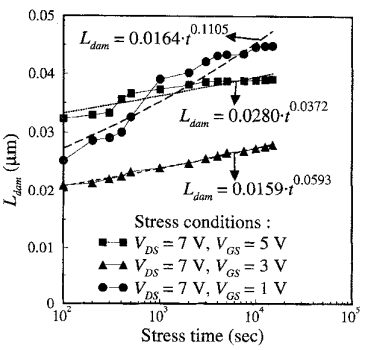

Fig. 7. Time evolution of the damaged region length at various stress biases.

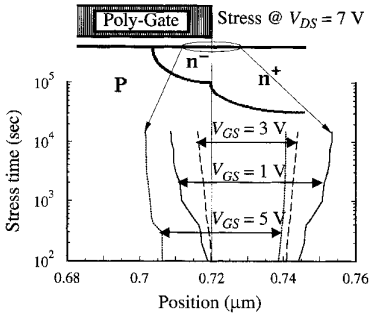

Fig. 8. Comparison of damaged regions for devices at different stress biases.

In order to further investigate the degradation in LDD n-MOSFET's, we also applied this method to tested devices under three different stress bias conditions (including $V_{\rm GS}$ = 1, 3, 5 V, and $V_{\rm DS}$ = 7 V). From Figs. 7 and 8, on one hand, we can see that the effective damaged length (most of which is located in the spacer region) is the shortest at $V_{\rm DS}$ = 7 V and $V_{\rm GS}$ = 3 V (or $V_{\rm GS} \approx V_{\rm DS}/2$) among all the bias conditions, and initially $L_{\rm dam}$ at $V_{\rm DS}$ = 7 V and $V_{\rm GS}$ = 5 V is the largest. However, it turns out that $L_{\rm dam}$ at $V_{\rm DS}$ = 7 V and $V_{\rm GS}$ = 1 V is the largest in the long run. On the other hand, the smaller the gate voltage bias, the closer to drain side the damaged region. Although, at first the amount of interface states at $V_{\rm DS}$ = 7 V and $V_{\rm GS}$ = 3 V is not the largest, due to the shortest $L_{\rm dam}$ it in turn leads to the rapid increase of interface states with stress time (shown in Figs. 9 and 10) and so enhances the degradation of drain current after a long time stress (shown in Fig. 11). In other words, for the devices stressed at the maximum substrate current ($V_{\rm GS} \approx V_{\rm DS}/2$), the oxide damage can be mainly attributed to interface trap generation through carriers [3]. For the comparison of growth rates in damaged length and magnitude of interface trap, Fig. 12 shows the fitting parameters in $L_{\rm dam}$ and $\Delta N_{\rm it}$ with a power form at different bias conditions. It reveals that with increasing stress time, the quantity of $\Delta N_{\rm it}$ at stress bias of $V_{\rm GS}$ = 3 V is the largest finally. However, from the beginning of the stress (Fig. 9), the quantity of $\Delta N_{\rm it}$ is not the largest. It means that in judging the current degradation in n-MOS devices, the criteria should consider both the combined effects of $\Delta N_{\rm it}$ and oxide damaged region length $L_{\rm dam}$. Based on the lateral surface electric field distributions and the time evolution of

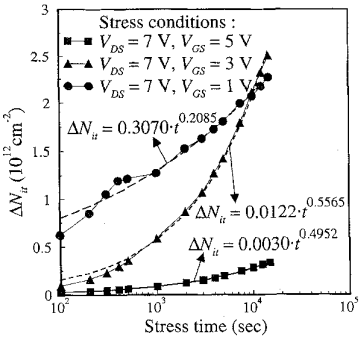

Fig. 9. Time evolution of $\Delta N_{\rm it}(x)$ at various stress biases.

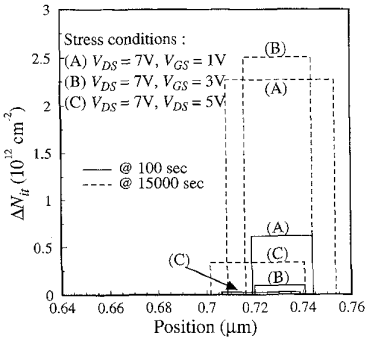

Fig. 10. Lateral distributions of $\Delta N_{\rm it}(x)$ at various stress biases for 100 and 15 000 s.

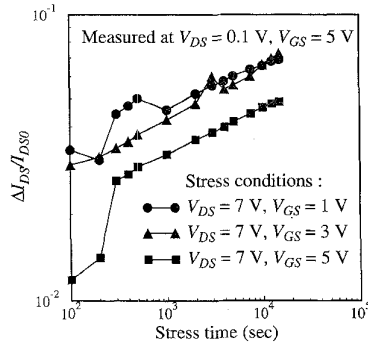

Fig. 11. Drain current degradations $\Delta I_{\rm DS}/I_{\rm DS0}$ versus time at various stress biases for comparison.

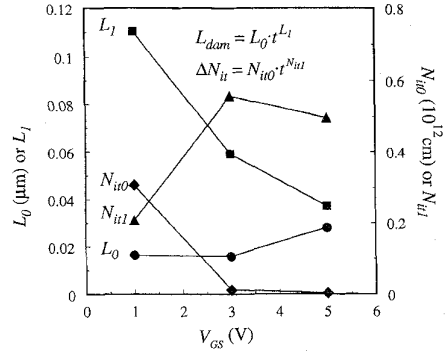

Fig. 12. Extracted parameters versus stress gate biases for Figs. 7 and 9.

power factors, it can be inferred that the effective damaged length in terms of FWHM will not necessarily increase with the increasing gate voltage bias.

To summarize, the advantages of the present method are listed below.

1) In this experiment, we can easily obtain the lateral distribution of the induced $\Delta N_{\rm it}$ along the channel *merely* from one time-evolutional CP current $I_{\rm cp} - V_{\rm gh}$, measured at 0-V drain/source bias. On one hand, because the drain and source are held constant at zero, this method can avoid changes of $V_T(x)$ and $V_{\rm fb}(x)$ during the inversion and accumulation half cycles. On the other hand, it requires no repetitive CP measurements, and hence avoids the likely imposition of re-stress on tested devices.
2) It can extract $\Delta N_{\rm it}$ distribution directly from CP measurement without taking $Q_{\rm ox}$ into account, even if it exists.
3) It can even extract $\Delta N_{\rm it}$ distribution outside of the contributed region that CP method can not detect.
4) This method can be generalized to calculate the local $\Delta N_{\rm it}$ distribution along the whole channel region (including the source side).

V. Summary and Conclusion

In this work, a new method has been developed for characterizing the lateral distributions of interface states and the effective time-dependent damaged lengths. The correlation between the generated interface states with the stress time and the device drain current degradation can then be well described.

In this new method, by combining the power law as a function of stress time and the charge pumping measurement data, we can directly calculate the time-dependent effective damaged length and the spatial distribution of interface states with a rectangular approximation. To further investigate the device drain current degradation in terms of $L_{\rm dam}$ and $\Delta N_{\rm it}$, the damages of devices at different stress biases are analyzed in detail. It shows that for the devices stressed at the maximum substrate current ($V_{\rm GS} \approx V_{\rm DS}/2$), the effective damaged length is the shortest. Moreover, device drain current degradation at this bias is the largest after a long period of stress since the generated interface state is most highly localized by comparing with the other stress biases.

Owing to its simplicity, the developed method is expected to be useful for investigating the structure dependence of the hot carrier reliability in the drain engineering of submicron or deep-submicron VLSI/ULSI design. Moreover, this method can be used as a good and precise monitor of the hot carrier reliability in the state-of-the-art VLSI/ULSI device design.

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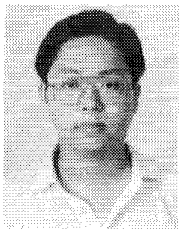

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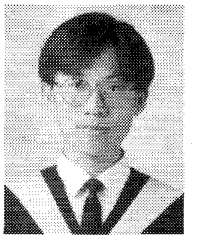

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Dr. Chung has served on various technical program committees of IEEE ASIC Conference (U.S.), International Electron Devices and Materials Symposium (IEDMS, Taiwan), and HPC (High Performance Computing)-ASIA'95.