A Novel Operation Method to Avoid Overerasure in a Scaled Trapping-Nitride Localized Charge Storage Flash Memory Cell and Its Application for Multilevel Programming

Wen-Jer Tsai, Nian-Kai Zous, Tahui Wang, *Senior Member, IEEE*,
Yen-Hui Joseph Ku, and Chih-Yuan Lu, *Fellow, IEEE*

***Abstract*—By using the charge pumping technique, it was found that the injected-hole occupied percentage increases with respect to the whole channel, and overerasure thus happens in a scaled trapping-nitride storage Flash memory cell. Such overerasure can be avoided or can be recovered if the cell is suitably biased during the erase operation. Moreover, the erase threshold voltage can be well controlled by the applied erase gate voltage. The reason is that both the channel-hot electrons and the band-to-band tunneling-induced hot holes would inject at the same time and are in balance as a specific surface potential is achieved. Based on this study, a self-limited soft program, as well as a self-saturated erase scheme, is proposed. Applications of this concept to multilevel programming are also demonstrated.**

***Index Terms*—Band-to-band-tunneling (BTBT)-induced hot-hole (HH) injection, channel-hot electron (CHE) injection, Flash electrically erasable programmable read-only memory (EEPROM), multilevel programming, multiplex virtual ground AND (MXVAND), NBit, nitride read-only memory (NROM), overerasure, programming by hot-hole injection nitride electron storage (PHINES), self-convergent, silicon–oxide–nitride–oxide–silicon (SONOS), soft program, trapped charge storage, trapping nitride.**

I. Introduction

The "BLOCK" erase is performed in a Flash memory to achieve high erase speed [1]. Inasmuch as a huge number of cells are erased simultaneously, good control of the threshold voltage ($\mathrm{V_t}$) of these cells is one of the key techniques to maintain high performance and reliability [2]. Many efforts have been devoted to reduce or to recover the overerased bits by optimizing process conditions and erase waveforms in conventional floating-gate Flash memories [2]–[6]. On the other hand, nitride-based localized charge storage Flash memories (Fig. 1) [7], [8], which use channel-hot electron (CHE) injection for program and band-to-band tunneling-induced hot-hole (BTBT HH) injection for erase, are thought to be free of overerasure [9] because the injected holes

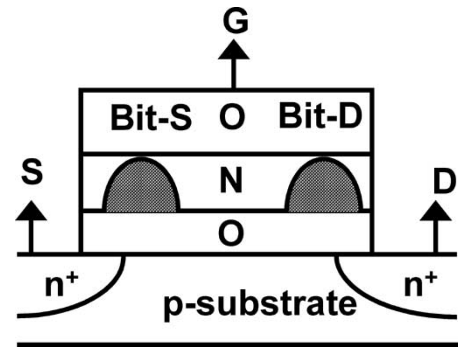


Fig. 1. Schematic representation of a trapping-nitride localized charge storage Flash memory cell. Each cell can store two bits of information (bit-D and bit-S).

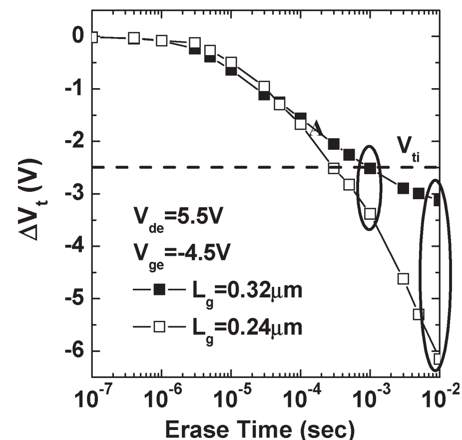


Fig. 2. Erase characteristics of two cells with $L_g = 0.24$ and $L_g = 0.32\ \mu$m, respectively. The erase bias $V_d/V_g = 5.5\ \mathrm{V}/-4.5\ \mathrm{V}$.

are locally trapped in the nitride layer. This is shown in Fig. 2, where the erase ($\mathrm{V_t}$) (V_{te}) of the cell with $L_g = 0.32\ \mu$m is almost saturated to its intrinsic value (V_{ti}) even when the erase time is much longer than 1 ms. For the cell with $L_g = 0.24\ \mu$m, however, overerasure occurs, and its V_{te} is much lower than its V_{ti} as the erase time increases. A charge pumping (CP) technique is used to analyze the lateral charge distributions [10]. In Fig. 3, $I_{\mathrm{cp}}/I_{\mathrm{cp,max}}$ is plotted against V_{gh}. Here, $I_{\mathrm{cp}}/I_{\mathrm{cp,max}}$ implies the percentage of the trapped hole region (with respect to the whole channel) with a local ($\mathrm{V_t}$) below V_{gh}. For the cell with $L_g = 0.24\ \mu$m, around 40% of the channel is

Manuscript received October 21, 2005; revised January 19, 2006. The review of this paper was arranged by Editor S.-I. Kimura.

W.-J. Tsai, N.-K. Zous, Y.-H. J. Ku, and C.-Y. Lu are with Macronix International Company Ltd., Hsinchu 300, Taiwan, R.O.C. (e-mail: vincenttsai@mxic.com.tw).

T. Wang is with Macronix International Company Ltd., Hsinchu 300, Taiwan, R.O.C., and also with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

Digital Object Identifier 10.1109/TED.2006.871198

0018-9383/$20.00 © 2006 IEEE

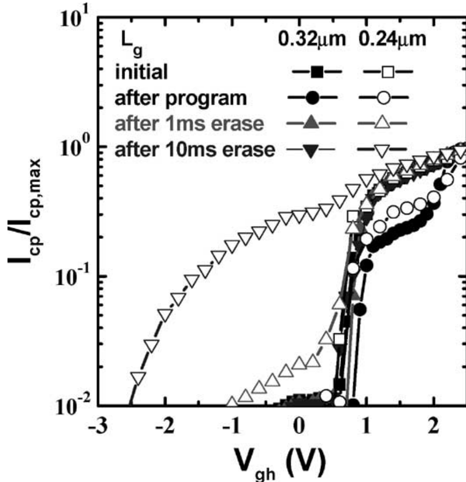


Fig. 3. Normalized CP characteristics corresponding to those of Fig. 2. With a similar hole injection, the hole-occupied percentage with respect to L_g is much higher for the cell with $L_g = 0.24\ \mu$m.

with a local $(\mathrm{V_t})$ lower than its V_{ti} as the erase time increases to 10 ms. It reduces the main channel potential and then causes a serious channel-shortening effect. For the cell with $L_g = 0.32\ \mu$m, however, $(\mathrm{V_t})$ is dominated by its V_{ti} inasmuch as the main channel is much less occupied by the injected holes ($\ll$ 10%). From the aforementioned, we find that the injection width of BTBT HH is controlled by a lateral field (the applied V_d during erase) and is not scaled with L_g proportionally [2]. As the device scales, overerasure would be a detrimental issue even in a localized charge storage cell. In this paper, we would like to explore the methods to suppress such overerasure in a scaled trapping-nitride storage Flash memory cell.

II. Unique V_g Dependence During the Erase Operation

Sometimes, a V_g stepping method is used to control the erase current or the erase speed [11]. However, we find some interesting phenomena in our case. Fig. 4 shows that V_{te} has a unique erase V_g (V_{ge}) dependence. Two cells are first programmed until their $(\mathrm{V_t})$s reach 5 V (A, A′). One of the cells is erased with $V_{\mathrm{ge}} = -0.5$ V for 10 ms (open square, A to B) and then with $V_{\mathrm{ge}} = -4.5$ V for another 10 ms (open circle, B to C). The other one is erased via a reverse sequence. In both cases, $V_d/V_s = 5.5\ \mathrm{V}/0\ \mathrm{V}$. Regardless of the sequence, overerasure results if $V_{\mathrm{ge}} = -4.5$ V (C and B′). Meanwhile, two characteristics are unusual. First, a saturated V_{te} (~ 2 V) is observed as $V_{\mathrm{ge}} = -0.5$ V (B and C′) even if the erase time is extended to 100 ms. What is more surprising is the evolution of $(\mathrm{V_t})$ from B′ to C′. Though the cell has been overerased ($V_{\mathrm{te}} = -1$ V at B′), it could still be recovered (to a higher $(\mathrm{V_t})$ value), and V_{te} is also converging to 2 V (C′). The increase of V_{te} means that electrons may be injected as well. The corresponding CP characteristics of these two cells at their various statuses (A, B, C, A′, B′, and C′ in Fig. 4) are measured to study the injected charge distributions (Fig. 5). I_{cp} is found to be the same if V_{ge} is the same regardless of the sequence of V_{ge} applied. It also shows that for B′ and C, 40% of the channel

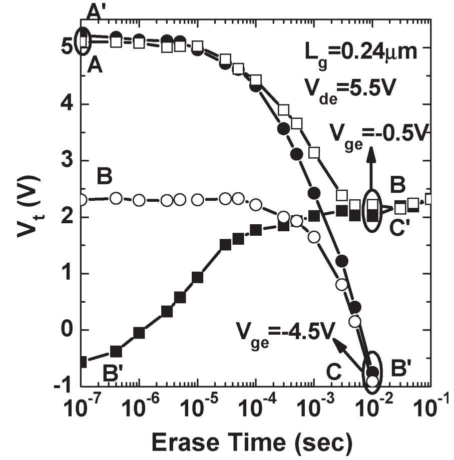


Fig. 4. Erase characteristics of two cells $(L_g = 0.24\ \mu\mathrm{m})$ with various V_{ge} sequences. One of the cells (A, open symbols) is erased with $V_{\mathrm{ge}} = -0.5$ V for 10 ms (open square, A to B) and then with $V_{\mathrm{ge}} = -4.5$ V for another 10 ms (open circle, B to C). The other cell (A′, solid symbols) is erased with $V_{\mathrm{ge}} = -4.5$ V for 10 ms (solid circle A′ to B′) and then with $V_{\mathrm{ge}} = -0.5$ V for another 10 ms (solid square, B′ to C′).

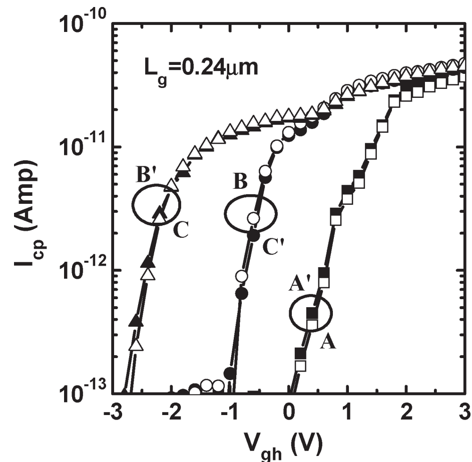


Fig. 5. I_{cp} curves corresponding to those of Fig. 4. The three cell states including programmed (A and A′), self-limited erased (B and C′), and overerased (C and B′) are clearly identified.

is with a local $(\mathrm{V_t}) < -0.5$ V, which means that the cell is at ON-state even when $V_{\mathrm{gp}} = -0.5$ V. In addition, the turn-around feature of I_{cp} from B′ to C′ also implies an increase of negatively trapped charges.

III. Results and Discussions

Typically, a self-convergent process can be achieved via two mechanisms. The first one is achieved by injecting holes and electrons simultaneously [5], [12]. These two injection processes will balance when a specific surface potential is achieved. The second one utilizes a vertical field-controlled Fowler–Nordheim (FN) injection [13] or a BTBT HH injection [14]. The final $(\mathrm{V_t})$ is independent of the initially stored charges once the applied program/erase time is long enough. In Figs. 6–10, the erase bias effects are characterized to clarify which mechanism is the dominant one.

In Fig. 6, under a fixed erase V_d (V_{de}), we found that the saturated V_{te} is strongly dependent on V_{ge}, and ΔV_{te} is equal

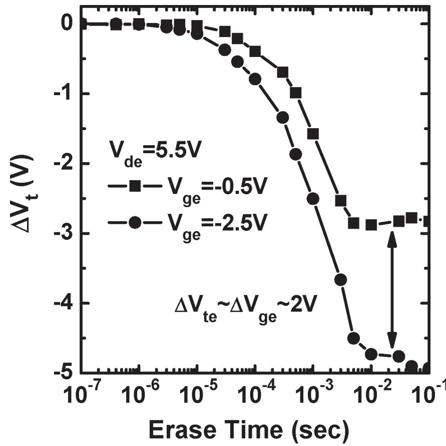


Fig. 6. Erase characteristics with the same V_{de} (5.5 V) and various values of V_{ge} (-0.5 and -2.5 V). ΔV_{te} is equal to ΔV_{ge} (2 V).

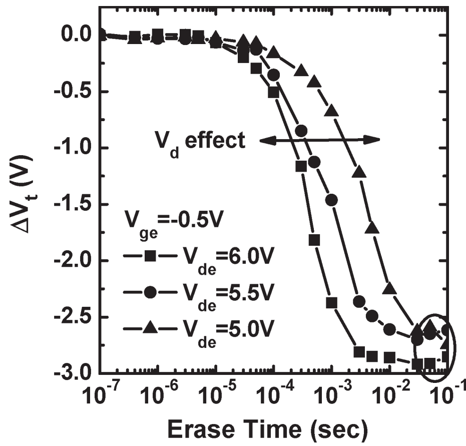


Fig. 7. Erase characteristics with the same V_{ge} (-0.5 V) and various values of V_{de} (5, 5.5, and 6 V). V_{te} is almost the same for each case.

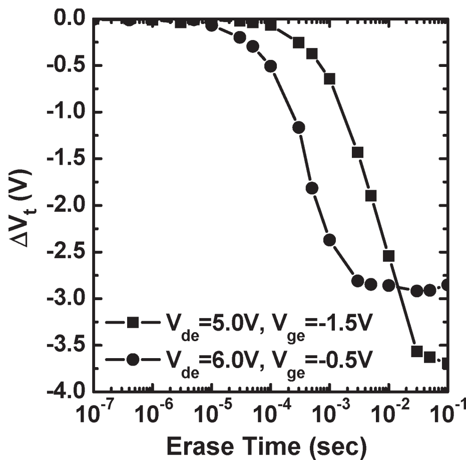


Fig. 8. Erase characteristics with the same V_{dg} (6.5 V). V_{de} affects the erase speed, whereas V_{ge} determines the saturated V_{te} level.

to ΔV_{ge}. A minor speed enhancement, which is due to a higher vertical field, is also observed. On the other hand, with the same V_{ge}, V_{de} only affects the erase speed, whereas V_{te} is quite close as shown in Fig. 7. To have a more fair comparison, the erase V_{dg} is kept constant as shown in Fig. 8. Although a faster erase speed is observed at $V_{\mathrm{de}}/V_{\mathrm{ge}} = 6\ \mathrm{V}/-0.5\ \mathrm{V}$, a

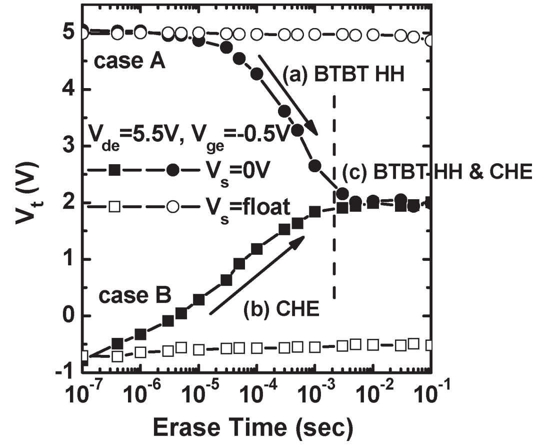


Fig. 9. V_s effect is studied in two cases. In case A, the cell is initially at a higher ($\mathrm{V_t}$) state (5 V). In case B, the cell is initially at a lower ($\mathrm{V_t}$) (-0.5 V) state. A self-saturated erase and a self-limited program for case A and case B, respectively, only occur as $V_s = 0$ V.

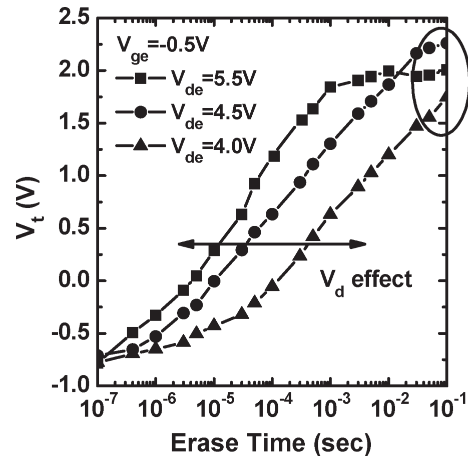


Fig. 10. Recovering speed of the overerased cells depends on the applied V_{de}. However, they are all converging to the same ($\mathrm{V_t}$), which is controlled by the same applied V_{ge}.

lower saturated V_{te} is found at $V_{\mathrm{de}}/V_{\mathrm{ge}} = 5\ \mathrm{V}/-1.5\ \mathrm{V}$. Once again, ΔV_{te} (1 V) matches ΔV_{ge} (-0.5 V vs. -1.5 V). This excludes the vertical field-related convergent process. From these characteristics, we may conclude that the decrease of V_{te} is dominant by the BTBT HH injection before it reaches the saturated value. The source bias (V_s) effect is shown in Fig. 9. The self-saturated erase (case A) and self-limited program (case B) only happen when $V_s = 0$ V. As the source is floating, the erase is inhibited for the cell initially at a higher ($\mathrm{V_t}$) state (e.g., 5 V). It is due to the adjacent junction (floating source) bias effect that is suppressing the BTBT HH injection efficiency [15]. Meanwhile, the program of the cell initially at a low ($\mathrm{V_t}$) state (e.g., -0.5 V) is stopped. It is due to the elimination of CHEs originating from the $\mathrm{n^+}$ source. In Fig. 10, the V_d effect on the further increase of ($\mathrm{V_t}$) demonstrates that the injected electrons are accelerated by the lateral field. Similarly, the ($\mathrm{V_t}$) evolution is dominated by such CHE injection before it saturates.

In summary, we can explain all the characteristics through Fig. 11. If the cell is at a high ($\mathrm{V_t}$) state and V_{ge} is low enough, BTBT HH dominates, and ($\mathrm{V_t}$) will decrease first (case A in

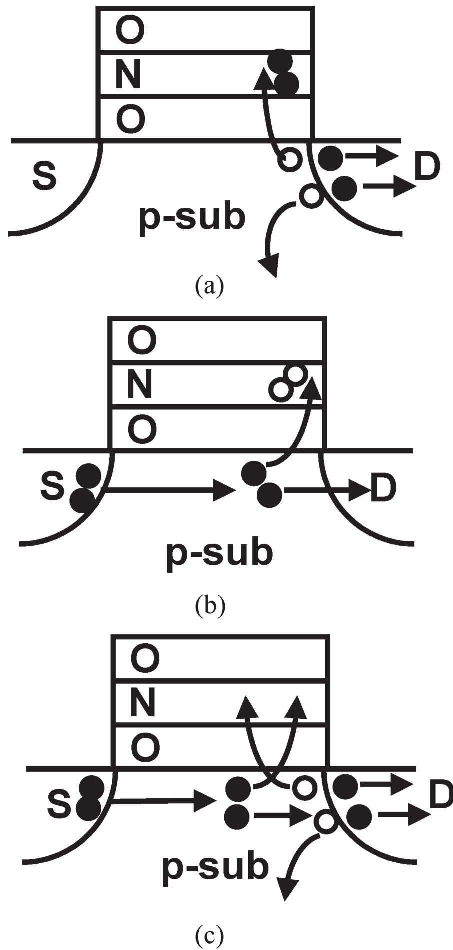


Fig. 11. Schematics of the related mechanisms. Though we just show the carrier injections near the drain side, both the drain and source are injected in all experiments (inasmuch as it is a $2b/c$ operation). They correspond to the (V_t) evolution as shown in Fig. 9. (a) If many electrons are stored in nitride or the applied V_g is more negative, the cell is at OFF-state. The BTBT HH injection will dominate and cause (V_t) to decrease. (b) If many holes are stored in nitride or the applied V_g is less negative, the cell is at ON-state. The CHE injection will dominate and cause (V_t) to increase. (c) Both the BTBT HH and CHE injections occur at the same time, as the stored charges and the applied V_g happen to result in a "balanced" surface potential.

Fig. 9). As the injected holes accumulated, the surface potential increases, and eventually, an inversion layer is formed. CHE injection then takes over. (V_t) is thus kept unchanged inasmuch as both the holes and electrons are injected into the trapping nitride simultaneously. Case B in Fig. 9 is similar but with a reverse sequence. V_{de} dominates the field heating effect and affects the erase speed, whereas V_{ge} modulates the surface potential and thus determines whether these two injection mechanisms occur at the same time as well as the convergent (V_t) level.

IV. Applications

A. Suppressing Overerasure

If a cell is overerased, it would conduct an undesirable leakage current during programming or reading the cells belonging to the same bit line, which may cause malfunctions in programming or reading the bit state. Repairing or suppressing the overerased bit is of great importance. Based on the characteristics shown, a self-limited soft program and a self-saturated erase scheme, which are similar to [5], are proposed. A designed V_g bias, which corresponds to a predetermined V_{te} level, is applied on the soft program (phase II in Fig. 12) following the erase operation (phase I in Fig. 12). The result is shown in Fig. 13. Though the V_{te} distribution after the erase may be as large as 2.5 V, it becomes as narrow as 0.3 V after the soft program. Alternatively, we may skip phase I and apply

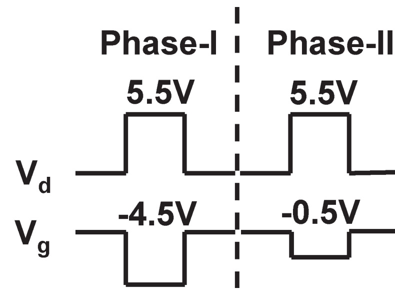


Fig. 12. Proposed operation methods to suppress overerasure. Phase II can act as a self-limited soft programming (see Fig. 13) right after a block erase operation (phase I). We may also skip phase I and use only phase II to achieve a self-saturated erase (see Fig. 14).

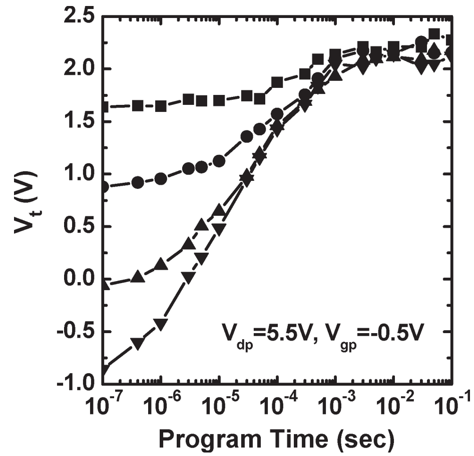


Fig. 13. Erase (V_t) distribution reduces from 2.5 to 0.3 V after the self-limited soft programming (phase II in Fig. 12) for 10 ms. It also implies the precise (V_t) control by the applied gate bias when programming an NBit cell.

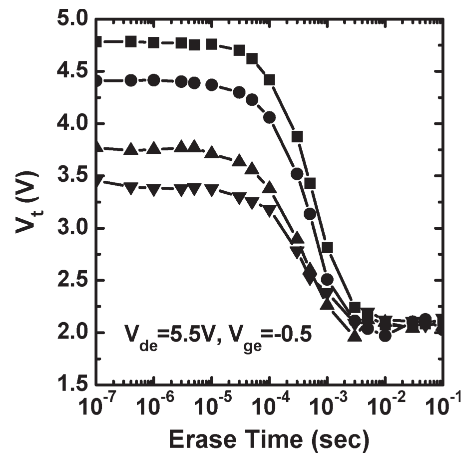
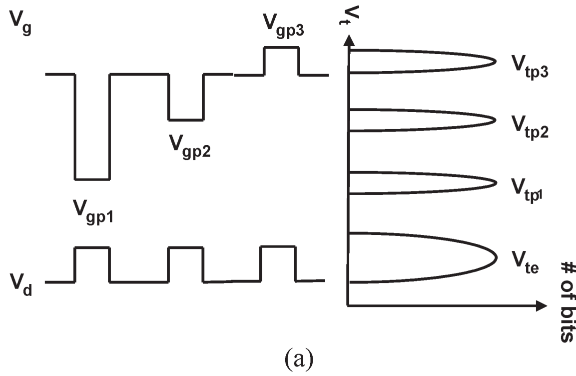
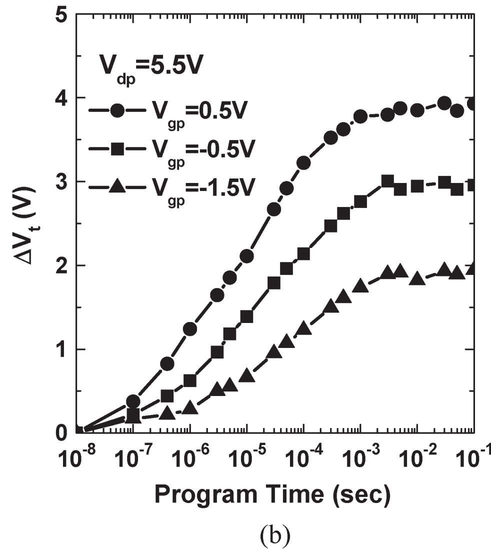


Fig. 14. Self-saturated erase (only applying phase II in Fig. 12) is achieved regardless of a wide range of programmed (V_t) distributions. It also implies the precise (V_t) control by the applied gate bias when programming a PHINES cell.

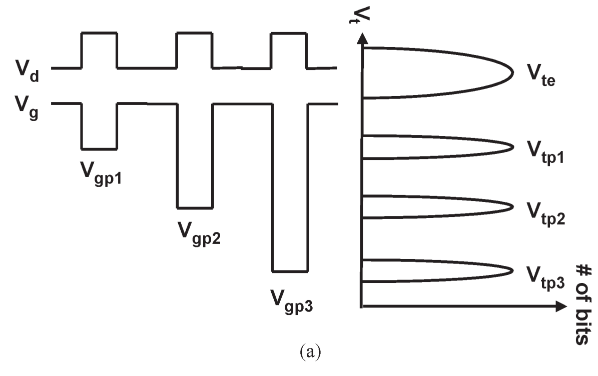


(a)

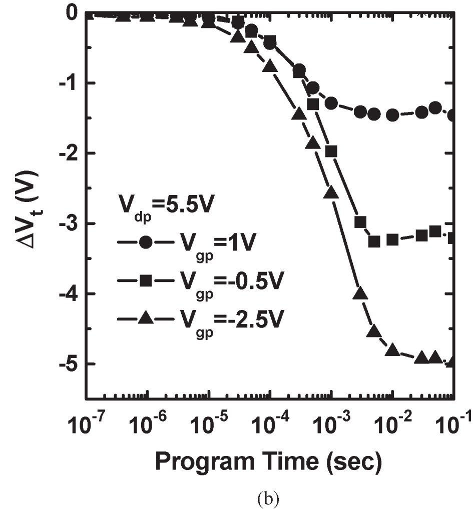


(b)

Fig. 15. (a) Bias scheme for a multilevel NBit cell operation. (b) Different $(\mathrm{V_t})$ states can be precisely achieved by varying V_{gp}.



(a)



(b)

Fig. 16. (a) Bias scheme for a multilevel PHINES cell operation. (b) Different $(\mathrm{V_t})$ states can be precisely achieved by varying V_{gp}.

phase II only. The result in Fig. 14 shows that a self-saturated erase can be achieved regardless of a wide range of program $(\mathrm{V_t})$ distributions.

B. Multilevel Programming

Though two-bit-per-cell storage has been realized in the trapping-nitride cell, it is found that the bit state may be influenced by the neighboring bit [16]. This is called the second-bit effect, which is getting worse as the cell is scaled [17]. Alternatively, conventional floating-gate Flash memories adopt the multilevel-cell (MLC) concept [18] to increase its density based on the same process technology. One of the key techniques to realize MLC is to precisely control the $(\mathrm{V_t})$ distributions. For example, a 0.5-V bandwidth for each bit state is required [18]. Based on the characteristics aforementioned, a self-limited program scheme similar to [5] is proposed by controlling the program gate voltage (V_{gp}). A designed V_{gp1} bias, which corresponds to the bit state of V_{tp1}, is applied in the first phase that is followed by applying V_{gp2} and V_{gp3} for the bit states of V_{tp2} and V_{tp3}, respectively [Figs. 15(a) and 16(a)]. Let us see the results in an NBit cell [8] that utilizes CHE and BTBT HH as the program (to a high $(\mathrm{V_t})$ state) and erase (to a low $(\mathrm{V_t})$ state) mechanisms, respectively. Fig. 13 can also represent the program characteristics. It means that though a 2.5-V bandwidth may exist for the erase state, its V_{tp} is convergent to the same $(\mathrm{V_t})$ level, which is determined by V_{gp}. Fig. 15(b) shows that V_{tp} is well controlled by the designed V_{gp}. Such scheme also works for a programming by hot-hole injection nitride electron storage (PHINES) cell [19] in which a negative-gate FN tunnel erase and a BTBT HH program are used. Similar results are shown in Figs. 14 and 16(b).

V. Conclusion

A self-limited carrier injection phenomenon is found in a scaled trapping-nitride localized charge storage Flash memory cell. A convergent $(\mathrm{V_t})$ state is due to the balance between CHE and BTBT HH as a specified surface potential is achieved. In this way, the gate bias can precisely control the convergent $(\mathrm{V_t})$ value, which suggests a way to avoid overerasure or to recover the overerased bits. It also provides a promising technique to realize the MLC concept and is applicable for both NBit and PHINES cell operations.

References

[1] W. D. Brown and J. E. Brewer, *Nonvolatile Semiconductor Memory Technology*. Piscataway, NJ: IEEE Press, 1997, pp. 193–194.

[2] K. Yoshikawa, S. Yamada, J. Miyamoto, T. Suzuki, M. Oshikiri, E. Obi, Y. Hiura, K. Yamada, Y. Ohshima, and S. Atsumi, "Comparison of current Flash EEPROM erasing methods: Stability and how to control," in *IEDM Tech. Dig.*, 1992, pp. 595–598.

[3] W. D. Brown and J. E. Brewer, *Nonvolatile Semiconductor Memory Technology*. Piscataway, NJ: IEEE Press, 1997, pp. 206–207.

[4] W. H. Lee, D. K. Lee, Y. H. Na, K. S. Kim, K. O. Ahn, K. D. Suh, and Y. Roh, "Impact of floating gate dry etching on erase characteristics in NOR flash memory," *IEEE Electron Device Lett.*, vol. 23, no. 8, pp. 476–478, Aug. 2002.

[5] S. Yamada, T. Suzuki, E. Obi, M. Oshikiri, K. Naruke, and M. Wada, "A self-convergence erasing scheme for a simple stacked gate Flash EEPROM," in *IEDM Tech. Dig.*, 1991, pp. 307–310.

[6] M. Ushiyama, Y. Ohji, T. Nishimoto, K. Komori, H. Murakoshi, H. Kume, and S. Tachi, "Two dimensionally inhomogeneous structure at gate electrode/gate insulator interface causing Fowler–Nordheim current deviation in nonvolatile memory," in *Proc. Int. Reliability Physics Symp.*, 1991, pp. 331–336.

[7] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: A novel localized trapping, 2-bit nonvolatile memory cell," *IEEE Electron Device Lett.*, vol. 21, no. 11, pp. 543–545, Nov. 2000.

[8] W. J. Tsai, C. C. Yeh, C. C. Liu, C. J. Hwang, Y. C. Chen, T. Liang, A. Liu, R. B. Chang, N. K. Zous, M. I. Liu, T. Wang, W. Ting, K. Ku, and C. Y. Lu, "Novel PHINES Flash EEPROM with 0.046 μm^2 bit size for giga-bit era application," in *Proc. IEEE Non-Volatile Semiconductor Memory Workshop*, 2004, pp. 79–82.

[9] M. K. Cho and D. K. Kim, "High performance SONOS memory cells free of drain turn-on and over-erase: Compatibility issue with current Flash technology," *IEEE Electron Device Lett.*, vol. 21, no. 8, pp. 399–401, Aug. 2000.

[10] S. H. Gu, M. T. Wang, C. T. Chan, N. K. Zous, C. C. Yeh, W. J. Tsai, T. C. Lu, T. Wang, J. Ku, and C. Y. Lu, "Investigation of programmed charge lateral spread in a two-bit storage nitride Flash memory cell by using a charge pumping technique," in *Proc. Int. Reliability Physics Symp.*, 2004, pp. 639–640.

[11] A. Chimenton, P. Pellati, and P. Olivo, "Constant charge erasing scheme for Flash memories," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 613–618, Apr. 2002.

[12] W. D. Brown and J. E. Brewer, *Nonvolatile Semiconductor Memory Technology*. Piscataway, NJ: IEEE Press, 1997, pp. 255–258.

[13] P. Candelier, F. Mondon, B. Guillaumot, G. Reimbold, H. Achard, F. Martin, and J. Hartmann, "Hot carrier self convergent programming method for multi-level Flash cell memory," in *Proc. Int. Reliability Physics Symp.*, 1997, pp. 104–109.

[14] W. D. Brown and J. E. Brewer, *Nonvolatile Semiconductor Memory Technology*. Piscataway, NJ: IEEE Press, 1997, pp. 261–263.

[15] W. J. Tsai, N. K. Zous, M. H. Chou, S. Huang, H. Y. Chen, Y. H. Yeh, M. Y. Liu, C. C. Yeh, T. Wang, J. Ku, and C. Y. Lu, "Cause of erase speed degradation during two-bit per cell operation of a trapping nitride storage Flash memory cell," in *Proc. Int. Reliability Physics Symp.*, 2004, pp. 522–526.

[16] C. C. Yeh, W. J. Tsai, T. C. Lu, S. K. Cho, T. Wang, S. Pan, and C. Y. Lu, "A modified read scheme to improve read disturb and second bit effect in a scaled MXVAND Flash memory," in *Proc. IEEE Non-Volatile Semiconductor Memory Workshop*, 2003, pp. 44–45.

[17] T. Mikolajick, S. Decker, J.-M. Fischer, R. Haberkern, R. Hagenbeck, P. Haibach, M. Isler, F. Lau, C. Ludwig, S. Riedel, M. Straburg, G. Tempel, and J. Willer, "Optimisation of a multi-bit charge trapping memory cell using process and device simulation," in *Proc. IEEE Non-Volatile Semiconductor Memory Workshop*, 2004, pp. 98–99.

[18] M. Bauer, R. Alexis, G. Atwood, B. Baltar, A. Fazio, K. Frary, M. Hensel, M. Ishac, J. Javanifard, M. Landgraf, D. Leak, K. Loe, D. Mills, P. Ruby, R. Rozman, S. Sweha, S. Talreja, and K. Wojciechowski, "A multilevel-cell 32 Mb Flash memory," in *Proc. IEEE ISSCC*, 1995, pp. 132–133.

[19] C. C. Yeh, W. J. Tsai, M. I. Liu, T. C. Lu, S. K. Cho, C. J. Lin, T. Wang, S. Pan, and C. Y. Lu, "PHINES: A novel low power program/erase, small pitch, 2-bit per cell Flash memory," in *IEDM Tech. Dig.*, 2002, pp. 931–934.

Wen-Jer Tsai was born in Hualien, Taiwan, R.O.C., on April 23, 1969. He received the B.S., M.S., and Ph.D. degrees in electronics engineering from the National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1991, 1993, and 2005, respectively.

In 1995, he was a Device Engineer at Macronix International Company, Ltd., Hsinchu, Taiwan, R.O.C. From 1995 to 2000, he has worked on the simulation, modeling, and design of nonvolatile memory devices. Since 2000, he has been engaged in the development of device and reliability physics of nitride-based NBit technology. His research interests include device characterization and reliability physics of nonvolatile memory devices.

Nian-Kai Zous received the Ph.D. degree in electronics engineering from the National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2002.

In 2003, he joined the advanced device group of the Device Technology Division, Macronix International Company, Ltd. (MXIC), Hsinchu, Taiwan, R.O.C. His research activities include the study of reliability and scaling issues in nitride-based NBit devices. Since 2005, he has been with the NBit Flash Technology Department, MXIC, and is responsible for the reliability issue on NBit product.

Tahui Wang (S'85–M'86–SM'94) was born in Taoyuan, Taiwan, R.O.C., on May 3, 1958. He received the B.S.E.E. degree from National Taiwan University, Taipei, Taiwan, R.O.C., in 1980 and the Ph.D. degree in electrical engineering from the University of Illinois, Urbana-Champaign, in 1985.

From 1985 to 1987, he was with Hewlett-Packard Laboratories, Palo Alto, CA, where he was engaged in the development of GaAs HEMT devices and circuits. Since 1987, he has been with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., where he is currently a Professor. His research interests include hot carrier phenomena characterization and reliability physics in very large scale integration (VLSI) devices, RF CMOS devices, and nonvolatile semiconductor devices.

Dr. Wang served as a technical committee member of many international conferences, among them IEDM, IRPS, and VLSI-TSA. He received the Best Teacher Award from the Ministry of Education, Taiwan, R.O.C.

Yen-Hui Joseph Ku received the B.S. degree in electrical engineering from the National Cheng-Kung University, Tainan, Taiwan, R.O.C., in 1979, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Texas at Austin in 1983 and 1988, respectively. His research was on the self-aligned silicide and shallow junction formation for deep submicrometer device application.

In 1987, he was the Co-Founder of Rapro Technology, Fremont, CA, with responsibility on RTPCVD reactor design and process development. From 1991 to 1992, he was with Paradigm Technology, San Jose, CA, where he worked on 0.35-μm 4-MB SRAM technology development. In 1992, he joined LSI Logic, Santa Clara, CA, where he worked on advanced logic technology development and served as Integration Manager of the R&D Division until 1997. He later joined the Technology Development Division of the Macronix International Co., Ltd., Hsinchu, Taiwan, R.O.C. He currently leads the Technology Development Center and is responsible for the development of advanced nonvolatile memory and embedded SOC technologies. He has published more than 30 papers in technical journals and conferences.

Chih-Yuan Lu (M'78–SM'84–F'95) received the B.S. degree from National Taiwan University, Taipei, Taiwan, R.O.C., in 1972 and the Ph.D. degree in physics from Columbia University, New York, NY, in 1977.

He was a Professor at the National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. and was with AT&T Bell Labs from 1984 to 1989. In 1989, he was a Deputy General Director at ERSO/ITRI, responsible for the MOEA Grand Submicron Project. This project successfully developed Taiwan's first 8-in manufacturing technology with high density DRAM/SRAM. In 1994, he was the Co-Founder of Vanguard International Semiconductor Corporation, which is a spin-off memory IC company from ITRI's Submicron Project. He was the VP of Operation, VP of R&D, and later President from 1994 to 1999. He is currently the Chairman and CEO of Ardentec Corporation, a very large scale integration (VLSI) testing service company, and also serves as a Senior VP/CTO at Macronix International Co., Ltd. (MXIC), Hsinchu, Taiwan, R.O.C. He led MXIC's technology development team to successfully achieve the state-of-the-art nonvolatile memory technology and now responsible for MXIC's overall memory operation. He has published more than 100 papers and has been granted 123 international patents.

Dr. Lu is a Fellow of the American Physical Society. He received the IEEE Millennium Medal and the most prestige semiconductor R&D Award in Taiwan from Pan Wen Yuan Foundation. He was granted the National Science and Technology Achievement Award by the Prime Minister of Taiwan, R.O.C. due to his leadership and achievement in the MOEA Grand Submicron Project.